

Process development and material characterization of Cu-Cu thermo-compression bonding (TCB) for high-conductivity electrical interconnects.

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Abstract

In this work, we focus on metal-metal Thermo-Compression Bonding (TCB) for realizing assembly of dielets to a silicon interconnect fabric (IF). The popular metal choices include bare Cu, Cu plated with Au and Au. Our approach simplifies the metallurgies used in classic chip-to-package assemblies by avoiding the use of solder and the concomitant issues of intermetallic formation such as electrical resistance and brittleness. In this paper, we address TCB parameter optimization and material characteristics of these metal-metal TCB joints. The roles of two physical mechanisms on Cu-Cu interface voiding i.e. surface roughness prior to TCB, oxide presence at bonding interface are evaluated in detail.

Key words

Thermo-compression bonding (TCB), Cu-Cu interface voiding, CMP process, SEM/FIB analysis,

I. Motivation

Die-to-package interconnects have not been scaled in the last several decades and are generally in the 100 – 200 μm pitch range, while in 3D integration die-to-die connections have been achieved at 40 μm pitch with some layout restrictions [1] [2]. These interconnections are usually realized by use of either lead-based or lead-free eutectic solders i.e. PnSn, SnAgCu, in the form of controlled collapse chip connection (C4) bumps, or solder-capped copper pillars. Using the classical approach, the reduction of chip-to-substrate interconnect pitch (50 μm) to fine pitch range (2 – 10 μm) remains a challenge [2]. During the solder reflow process, the solder material is squeezed out and therefore restricts the possibility of placing interconnects at the finer pitches i.e. < 50 μm . Moreover, the solder joints face the issue of brittle intermetallic formation [3] and joint fatigue over the life time of interconnection. In order to achieve finer chip-to-substrate pitches, we are proposing a metal-metal interconnection approach which utilizes a Thermal Compression Bonding (TCB) process and avoids use of classic solder materials. In

this study, we will investigate the bonding techniques and materials issues.

II. Materials and test samples

In this work, we focus on Copper-Copper (Cu-Cu) interconnects made using Thermal Compression Bonding (TCB) for realizing die-to-substrate interconnection. The test vehicles for both die and substrate were based on silicon which was metallized with copper using dc-electroplating process. The details of the test vehicles are described in table 1.

Table I: Details of test vehicles

Si-based test vehicle		
Material	Thickness (μm)	Purpose
Si	525	Die/Substrate material
SiO ₂	0.50	Insulation layer
Ti-sputtered	0.05	Barrier layer
Cu-sputtered	0.30	Seed layer

Cu-electroplated	5	Contact layer
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The metallized silicon wafers (12-inch) were diced into various coupon sizes. The smaller coupons with edge sizes of 1-4 mm were regarded as dielets and those with 5-10 mm length were regarded as substrates. The samples were provided by GlobalFoundries.

III. Thermal compression bonding

A thermal compression bonding (TCB) process was used to produce blank Cu-to-Cu interconnection by mounting test dies on test substrates. The process was carried out in a Karl Suss SB6 substrate bonder. The schematic of the experimental setup is shown in Fig. 1. The chip-substrate stack shown was loaded into a process chamber equipped with two heating plates (top and bottom) and could be loaded up to a defined bonding pressure. During TCB bonding, the chamber was initially evacuated to a base pressure in the range of $1\text{-}2 \times 10^{-2}$ mbar using a turbo molecular pump. Once the base pressure was reached, the stack was heated from both sides at a relatively high heating rate ($35\text{ }^{\circ}\text{C}/\text{min}$) to a temperature range of $250\text{-}300\text{ }^{\circ}\text{C}$. Afterwards, the stack was brought into intimate contact with a bonding pressure of 10 MPa, which was normalized to the contact size. Both temperature and pressure were maintained for a certain period of time, during which solid state diffusion of copper atoms across the chip/substrate interface is expected. Thereafter, the pressure was removed and the assembly was allowed to cool at a slow rate ($2.5\text{-}5\text{ }^{\circ}\text{C}/\text{min}$). The bonded device was then taken out of the chamber and optionally annealed at $400\text{ }^{\circ}\text{C}$ in an oven to achieve a clean bonded interface.

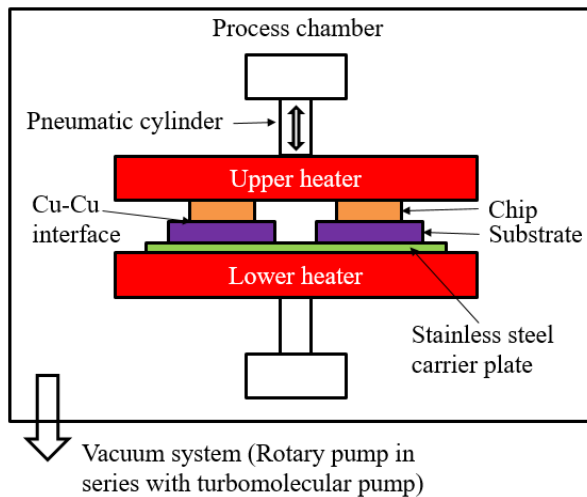


Fig. 1: Schematic of thermal compression bonding.

Various process parameters such as temperature, pressure, bonding environment and surface roughness and

surface preparation were optimized during the TCB process development. At this stage, the optimization criterion is the shear strength of the die on the substrate. A systematic DOE approach was used to determine the optimized process parameters, which are listed in table 2. Surface preparation is key and is discussed in detail below.

Table II: Optimized process parameters

Process parameters for TCB	Values
Temperature, T	250 $^{\circ}\text{C}$
Heating rate, dT/dt	35 $^{\circ}\text{C}/\text{min}$
Pressure, P	10 MPa
Bonding time, t	30 min
Ambient pressure, P	1.5×10^{-2} mbar
Annealing time and environment	2 h in vacuum
Surface roughness and planarization	< 20 nm

IV. Factors affecting Cu-Cu TCB

The Cu-Cu thermo-compression bonding process is a solid state diffusion process, which is driven by temperature and external pressure. The original bonding interface usually disappears due to diffusion and grain growth. The Cu layers merge and a homogeneous layer is obtained. For Cu-Cu TCB joints, the diffusion coefficients and activation energies of Cu strongly depend on the surface crystallographic orientation as well as the environment in which the bonding is performed [4]. Another factor that can affect the copper bonding process such as oxidation. Two kinds of oxides, namely cuprous Oxide (Cu_2O) and Cupric Oxide (CuO), are usually formed on the copper surface [5]. These interfacial oxides inhibit the Cu inter-diffusion and grain growth needed to initiate the bond. Wet etching techniques such as acetic acid dipping has been used to minimize the oxides. Other oxide removing techniques such as in-situ formic acid vapor application and forming gas (N_2/H_2 : 80/20 %) also are common practices for Cu-Cu direct bonding [6]. In a classic solder-based reflow process, the solder usually accommodates any topographic irregularities. In the absence of solder, surface planarization to the atomic level is an important requirement that we have addressed. We have used Chemical Mechanical Planarization (CMP) for surface flatness and have made a comparative study for the as dc-electrodeposited and planarized copper surfaces.

V. Characterizations for dc-plated Cu surface and Cu-Cu bonds

A. X-ray diffractometry

The crystallographic orientation of the copper can greatly affect the Cu-Cu solid state diffusion process. It is a known fact that (111)-oriented copper surfaces have higher diffusion rates compared to other crystallographic orientations [7]. The X-ray diffractometer revealed the presence of polycrystalline phases on dc-electroplated Cu used for direct Cu-Cu bonding. The XRD 2θ - ω scans in Fig. 2 show multiple peaks indicating the deposition of polycrystalline copper. (111)-orientation Cu surface would be preferred due to fast solid state diffusion, the dc-plated Cu surface having polycrystalline phases with relatively planar and smooth surface texture (roughness < 16 nm) could achieve good bonding at the interface region using optimized process parameters.

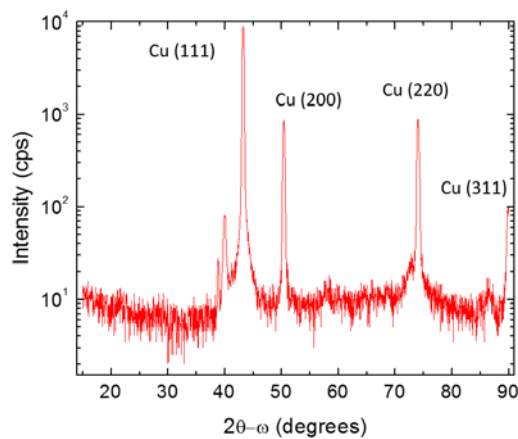


Fig. 2: XRD 2θ - ω scan showing polycrystalline phases on dc-plated copper surface

B. Surface roughness using AFM scans

The surface roughness plays a key role during Cu-Cu direct bonding. A smoother surface is always desired to make intimate contact during TCB. The surface roughness was measured using AFM over the dc-plated Cu surface.

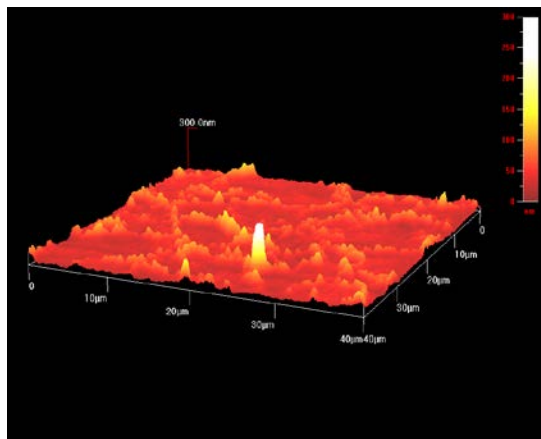


Fig. 3: AFM scan on Cu surface over 40 X 40 μm .

Fig. 3 shows that over a scan length of 40 micron and at a scan rate of 1 Hz, the RMS deviation of the surface roughness is about 16 nm. A promising interfacial bonding at the Cu-Cu interface was found with less than this magnitude of surface roughness. The average surface roughness was well below 16 nm on the measured samples from GlobalFoundries. However, other plating techniques produce higher surface roughness of a few hundred nanometers. These samples were subjected to a CMP process to get a surface planarization and an average surface roughness below 10 nm.

C. SEM/FIB images of Cu-Cu interface

In order to see the quality of bonds, the metallographic cross sections of the Cu-Cu bonded joints were made, which were bonded under optimized bonding conditions (10 MPa, 250 °C, 30 min, 1.5×10^{-2} mbar ambient). These samples had an average surface roughness of < 16 nm on both chip and substrate sides. These samples were subjected to a pre-bonding surface treatment of an acetic acid (99.6 %) dip for about 30 seconds and thereafter the samples were transferred to the bonding chamber within 3 minutes of acid treatment. Both chips and substrate were not subjected to any DI water cleaning. The copper surface was flushed with dry nitrogen gas to remove any remaining acid traces. The SEM image in Fig. 4 shows no apparent voids on the polished cross section of the bonded joint. Further FIB cross sections, shown in Fig. 5, were made along the interface in perpendicular direction of the original cross section. A closer examination of the FIB cross section in Fig. 6 reveals the presence of a few voids in the range of 100 to 250 nm. These samples were not annealed after the bonding process at all.

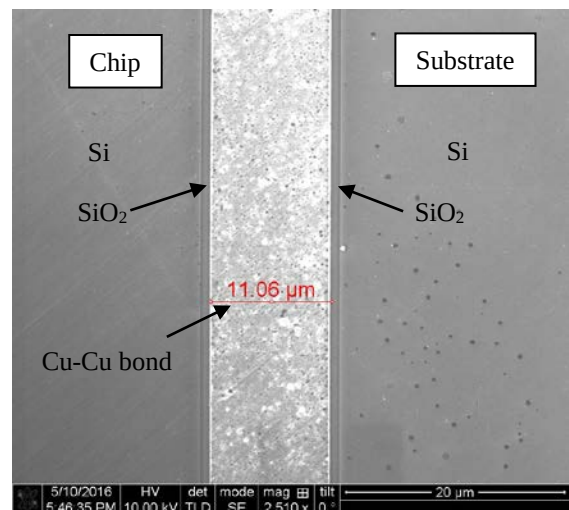


Fig. 4: SEM image of a bonded Cu-Cu interface.

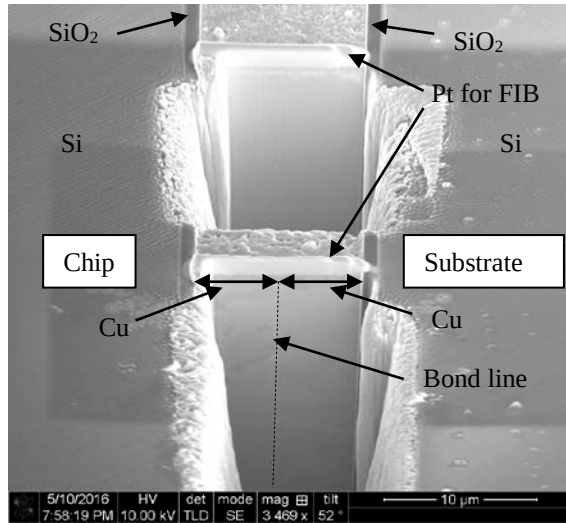


Fig. 5: FIB cross sections on a bonded Cu-Cu interface.

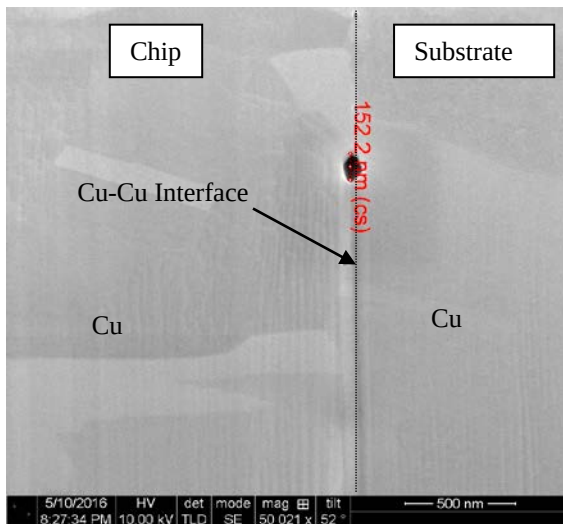


Fig. 6: FIB cross section of a bonded Cu-Cu interface without annealing step.

The annealing of the bonded samples at 400 °C under vacuum for two hours resulted in a more uniform Cu-Cu interface. The voids tend to reduce in size but were not completely eliminated. The interface looked better than the unannealed bonded samples in FIB cross-sections. Moreover, the grains on both chip and substrate started to grow across the interface and the bond line in the interface seemed to disappear as shown in Fig. 7. The time delay between the acetic acid treatment and the sample transfer to the processing chamber was very critical. If this time exceeds 3 minutes, a layer of oxide began to build up at the interface, which hindered the bonding of two copper

surfaces as shown in Fig. 8. This sample was exposed to ambient conditions for approximately 15 min after acetic acid treatment, which led to the oxidation of copper at the surface.

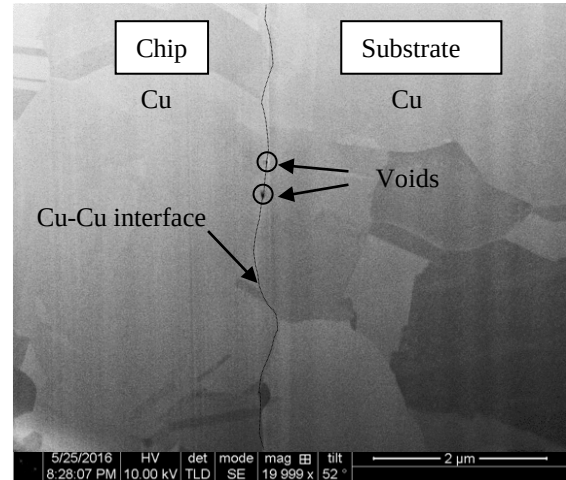


Fig. 7: FIB cross section of bonded Cu-Cu interface after annealing at 400 °C for two hours.

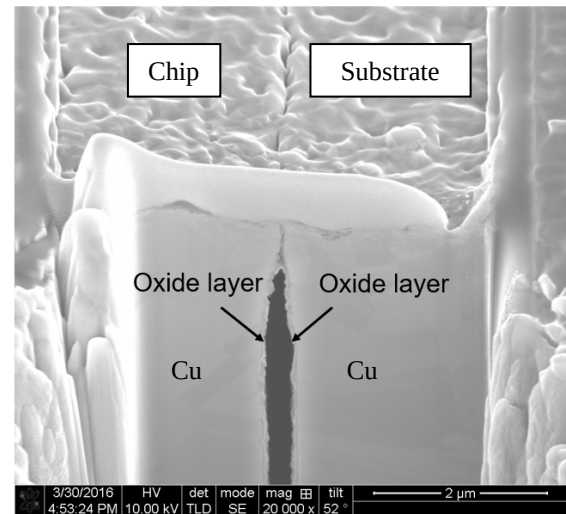


Fig. 8: FIB cross section of Cu-Cu interface with large transfer time (15 min) between acetic acid treatment and processing chamber transfer.

The effect of surface planarization on the bonding of copper surfaces was also studied. The samples had a surface roughness of few hundred nanometers. The TCB of these samples results in poor or no bonding at all. The FIB cross section in Fig. 9 reveals that non planarity of the surfaces result in no bonding at all.

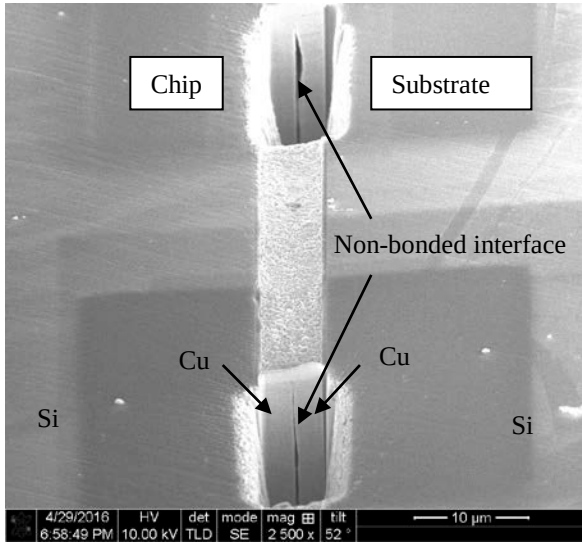


Fig. 9: FIB cross section of a non-planarized Cu-Cu bonding interface.

The chemical mechanical planarization (CMP) process was employed in our laboratory facility for the Cu samples before TCB process. The polished samples exhibit excellent bonding under optimized bonding conditions after the planarization process. The FIB cross section of the CMP treated samples is shown in Fig. 10. These samples were not subjected to the annealing step.

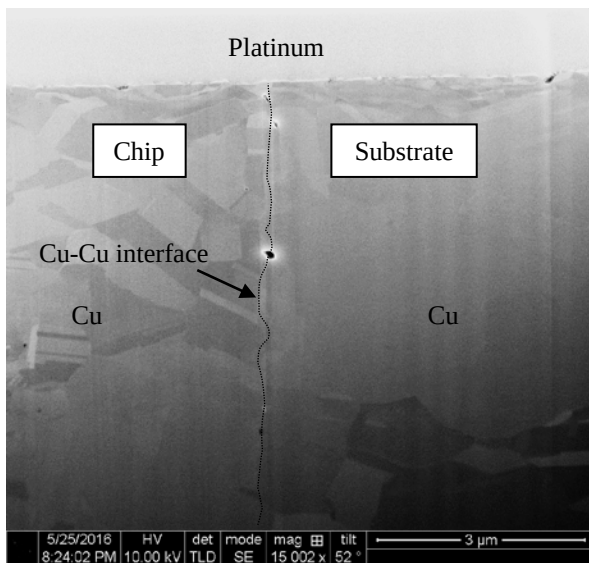


Fig. 10: FIB cross section of CMP planarized Cu-Cu bonding interface.

V. Discussion and conclusions

We performed a thorough investigation of the Cu-Cu

thermal compression bonded samples. Two factors are very important: i.e. “surface oxide” and “surface roughness and planarity” and have a profound effect on direct Cu-Cu TCB. It is essential to remove any surface oxide layer prior to the bonding, which in our case was performed using an acetic acid dip for 30 seconds. Moreover, during the TCB process it is essential to minimize the copper surface oxidation which can be achieved by a lower ambient pressure i.e. 1.5×10^{-2} mbar (rough vacuum range) inside the chamber. The smoother and planarized Cu surfaces achieve good interfacial bonding. The chemical mechanical planarization (CMP) process is essential for the preparation of copper surfaces for TCB bonding. Though fairly uniform bonding interface was achieved after the TCB process using optimized parameters (10 MPa, 250 °C, 30 min, 1.5×10^{-2} mbar ambient), the annealing at 400 °C for 2 hours helps to minimize the interface voids while at the same time accelerates the copper grains on both chip and substrate sides to grow across the bond line. The bonded joint consists of copper grains as found in a single copper layer.

Direct Cu-Cu bonding avoids use of any solder material which comes with the disadvantages of squeezing the solder material between the Cu-stamps during the bonding process and formation of brittle intermetallic compounds. The former prevents the placing of interconnects at finer pitch with the possibility of electrical shorts between the adjacent interconnects while the latter poses reduced joint life-time under cyclic temperature cycles. Moreover, copper has very high electrical and thermal conductivity in comparison with solder materials which makes it an excellent choice for interconnect material.

VI. Future work

For performance comparison with classic solder materials, the reliability tests such as passive temperature cycling and active power cycling for Cu-Cu contacts will be performed. Furthermore, the mechanical and electrical characterization of these contacts will be performed to measure the shear strength and electrical resistance respectively.

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References

- [1] S. S. Iyer, "Heterogeneous Integration for Performance and Scaling," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. PP, no.99, pp.1-10 doi: 10.1109/TCPMT.2015.2511626

- [2] S. S. Iyer, "Three-dimensional Integration: A Tutorial for Designer," in *Solid-State Circuits Magazine IEEE*, vol. 7, no. 4, pp. 63-74. doi:10.1109/MSSC.2015.2474235
- [3] Y. Wang, I. M. De Rosa, K. N. Tu, "Size effect on ductile-to-brittle transition in Cu-solder-Cu micro-joints," in *Proc. 2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, pp 632 - 639, doi: 10.1109/ECTC.2015.7159658
- [4] D. B. Butrymowicz, J. R. Manning, and M. E. Read, "Diffusion in Copper and Copper Alloys," *Journal of Physical and Chemical Reference Data*, vol. 2, no. 3. pp. 643-656, 1973.
- [5] L. Peng, L. Zhang, J. Fan, H. Y. Li, D. F. Lim, and C. S. Tan, "Ultrafine pitch (67 μm) of recessed and bonded Cu-Cu interconnects by three-dimensional wafer stacking," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1747-1749, 2012.
- [6] J. Fan and C. Tan (2012), " Low temperature wafer-level metal thermo-compression bonding technology for 3-d integration" in *Metallurgy- Advances in Materials and Process*, Dr. Yogiraj Pardhi (Ed.), InTech. doi: 10.5772/48216
- [7] D. B. Butrymowicz, J. R. Manning, M. E. Read, "Diffusion in Copper and Copper Alloys," in *Journal of Physical and Chemical Reference Data*, vol. 2, no. 3, pp. 643-656. doi: 10.1063/1.3253129