Impact of Reprocessing Technique on First Level Interconnects of Pb-Free to SnPb Reballed Area Array Flip Chip Devices

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Abstract

The risk of damage caused by reballing SnPb eutectic solder balls onto a commercial off-the-shelf (COTS) active flip chip with a ball grid array (BGA) of SAC305 was studied. The effects of reballing performed by five different reballers were examined and compared. The active flip chip device selected included manufacturer specified resistance between eight (8) differential port pairs. The path resistance between these pins following reballing, as compared to an unreballed device, was used to assess damage accumulation in the package. 2-dimensional x-ray microscopy, acoustic microscopy, and x-ray computer tomography were also used to characterize the effects of reballing. These studies indicated that no measureable damage was incurred by the reballing process, implying that reballed devices should function as well as non-reballed devices in the same application.

Key words

Audit, flip chip, Pb-free to SnPb, process control, reballing

I. Introduction

The electronics assembly market has experienced a material shift from lead (Pb) based solders to Pb-free solders as a result of the widespread adoption of Reduction of Hazardous Substances (RoHS) legislation and practices in commercial industry. An impact of this shift is it increasingly difficult to procure commercial off-the-shelf (COTS) components with tin-lead (SnPb) solder balls or finish for high reliability applications.

There are three responses to the scarcity of acceptable SnPb parts: custom order, reprocess or adapt. Reprocessing parts saves money because the parts are COTS, but expends money and resources by performing post processing on them. Additionally, the added labor and handling increases the risk of damaging the part.

This work is part of a larger study focused on reliability repercussions of reprocessing ball grid array (BGA) parts by reballing them from tin-silver-copper (SAC305) solder to SnPb eutectic solder.

Reballing is a processing technique that completely replaces existing solder balls with new ones on ball grid array (BGA) packages. Reliability concerns with reballing are focused on the second level interconnects, but there is interest in possible damage to the first level interconnects as a result of the process.

The two major procedures that comprise a reballing process are ball removal and ball attachment. Ball removal melts off the pre-existing solder balls and prepares the solder pads for new solder balls. There are two types of procedures for removal of solder spheres: one melts the lead-free spheres with a hot implement to remove the liquid solder by wick absorption, Figure 1, top. The other procedure dissolves the lead-free spheres by touching them to a tin-lead molten solution, Figure 1, bottom. The second major procedure, ball attachment, is the placement of new solder spheres on the pads and reflowing them to form an intermetallic bond. All reballers used comparable methods for ball attach.

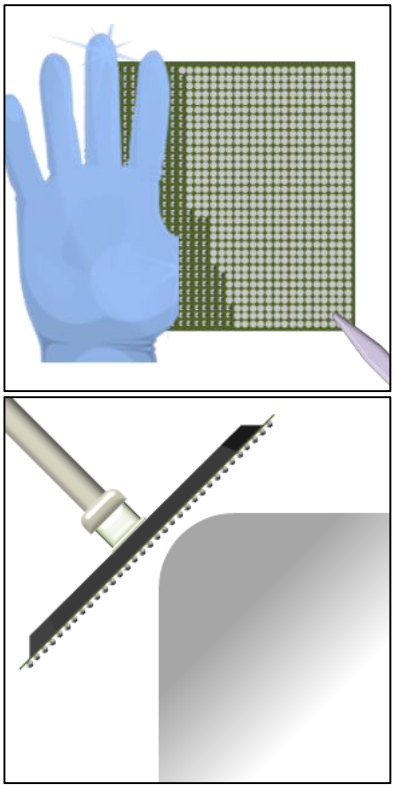


Figure 1: Methods of ball removal: solder balls are melted manually with an iron and wicked away by copper braid (not shown) (top). Alternately, the component is mechanically touched to molten solder, melting and dissolving existing solder balls into the bath (bottom).

II. Approach

Test vehicles that allowed for electrical measurement of damage induced in the first level interconnects as a result of reballing were selected. Thermal measurements in the package were taken during ball removal and ball attachment of other, dummy components, to identify stresses distinguishing different processes and reballers.

A. Test Vehicle Selection

A Vitesse VSC3312 asynchronous crosspoint switch was chosen for this study. Figure 2 displays top and bottom views of this component. It has 196 solder balls of 0.64mm diameter and 1.00mm pitch, and 139 solder bumps of ~0.125mm diameter and 0.25mm pitch.

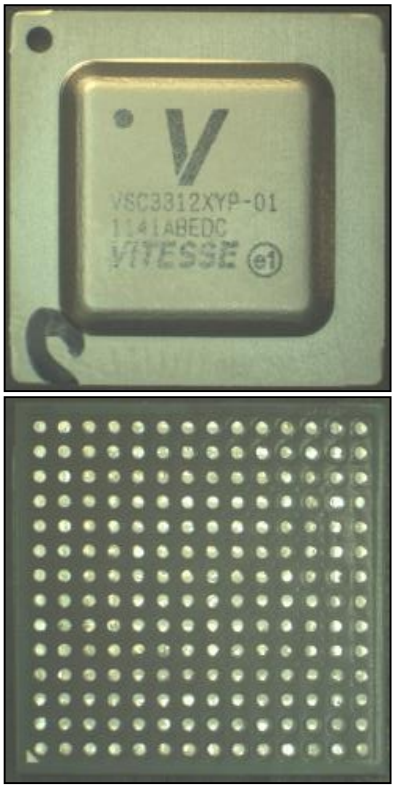


Figure 2: VSC3312 crosspoint switch, top (top) and bottom (bottom) views. This part has been marked with a C (for control) and prepared for testing by removing the external solder balls.

The technical datasheet indicates that for the eight (8) input pair circuits, pictured in Figure 3, two 50Ω pull-up resistors exist between the true and complement. The manufacturer specifies a resistance of 85Ω to 125Ω for these pairs.

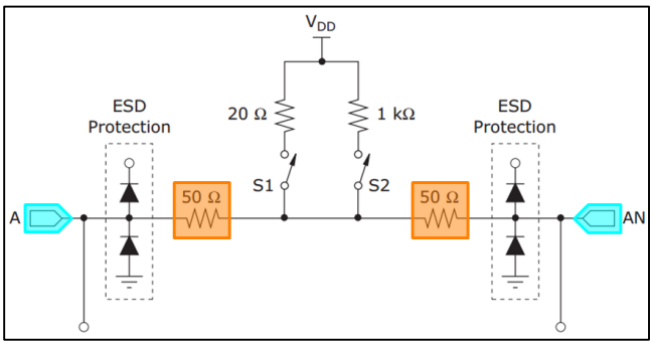


Figure 3: High speed input buffer equivalent circuit demonstrating 100Ω between "A" and "AN" differential port and complement.

B. Sample Preparation

Ten (10) VSC3312 flip chips were sent to each reballer. Reballers were instructed to remove the SAC305 solder spheres and clean and dress the pads with flux as they normally would for ball attach. Without placing SnPb solder spheres or solder paste on the dressed pads, they were asked

to reflow the parts and clean and bake out the components to simulate the ball attach process.

Reballers are identified as A, B, C, D, and E. Reballers B and D manually remove solder balls, shown on the top in Figure 1, which tends to inflict the least thermal shock. Reballers C and E employ the automated molten solder technique, on the bottom in Figure 1, which inflicted more thermal shock on the parts than manual processing. Reballer A also uses a molten solder ball removal technique that is distinct from the procedure used by C and E. The technique used by Reballer A exposes the devices to thermal shock on par with, or in excess of, that of Reballers C and E [1].

Upon receipt, nine (9) parts from each reballer were reflowed to mimic assembly. Reflow profile is displayed in Figure 4.

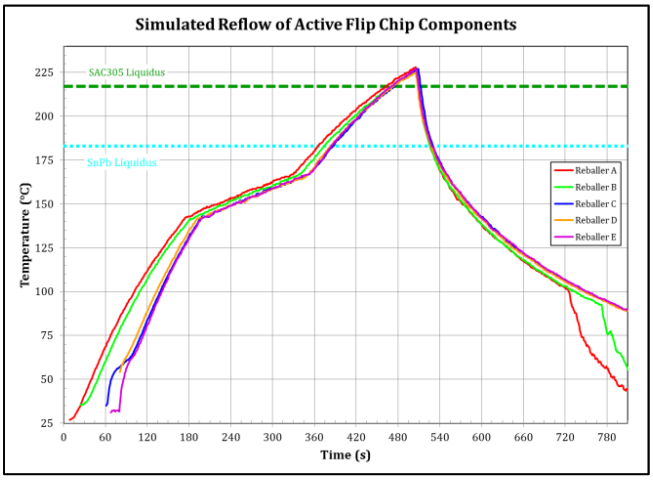


Figure 4: Simulated assembly profile applied to active flip chip components following ball removal and simulated ball attach.

C. Control

As an unprocessed control, ten (10) test components were not exposed to any modification or thermal excursions. Ball removal was performed with low speed shear with the XYZTEC Condor Classic Bond Tester. This process removed the bulk of each solder sphere while leaving the pads intact.

III. Inspection and Characterization

Electrical characterization, acoustic microscopy, and 3-D x-ray microscopy, were performed on flip chip assemblies to assess the potential reliability concerns of the first level interconnect solder bumps after undergoing reballing.

A. Electrical Characterization

Five (5) reprocessed components were probed per population, all measurements for all components fell within the 85Ω and 125Ω range defined by the manufacturer specification. Average resistance for each pair by reballer is summarized in Figure 5. Minor deviations between particular bond pad pairs and reballers are evident, however, no statistically significant changes in measured resistance were observed as the result of reballing.

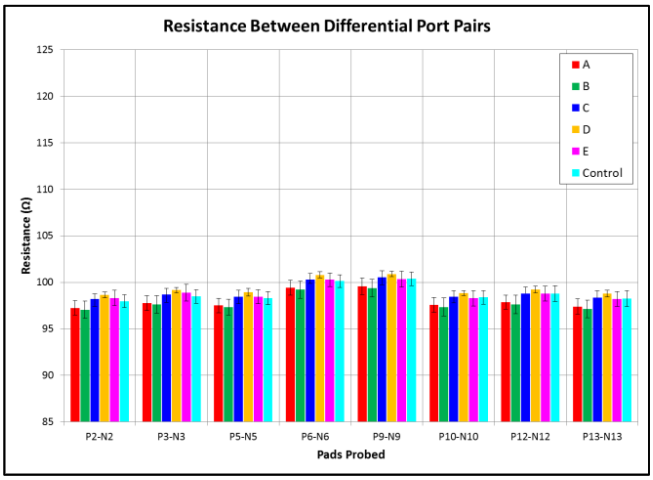
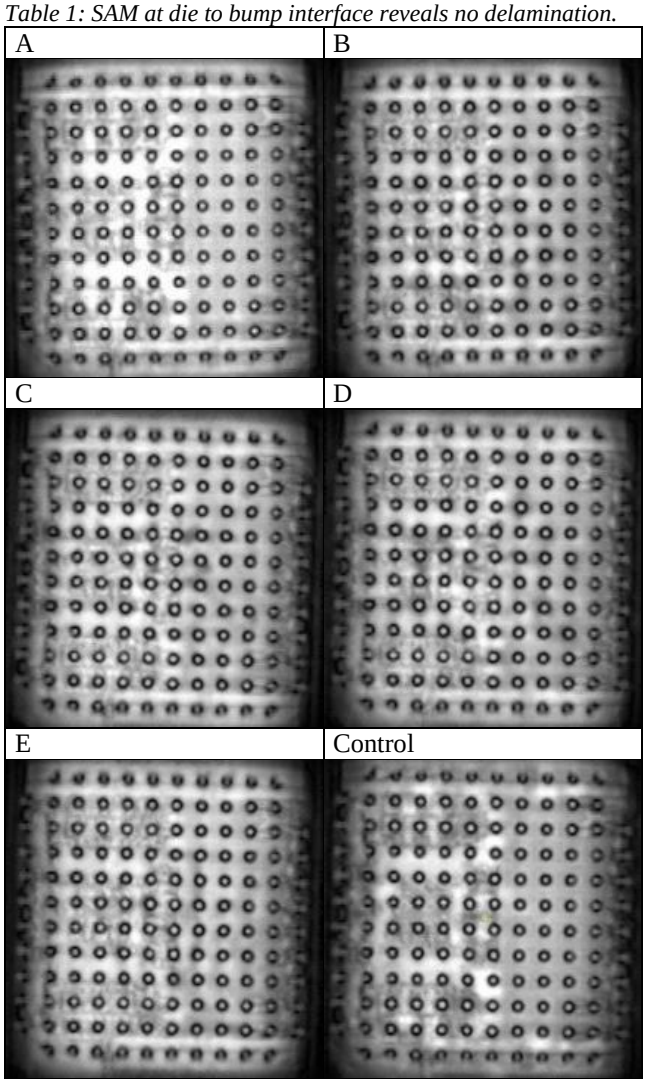


Figure 5: Average resistance between pads by differential port pair and reballer. Error bars indicate standard deviation. N=5.

B. Scanning Acoustic Microscopy

Tomographic acoustic micro-imaging (TAMI), a type of scanning acoustic microscopy (SAM), was performed on one flip chip processed by each reballer and a control. Imaging was focused at the interface where the solder bumps adhere to the pads on the die, visible in Table 1; and to the substrate, not shown. If observed, gaps, voids or delamination would be superimposed in red and yellow over black and white x-ray images; these defects were not observed on reballed or control components.

Table 1: SAM at die to bump interface reveals no delamination.

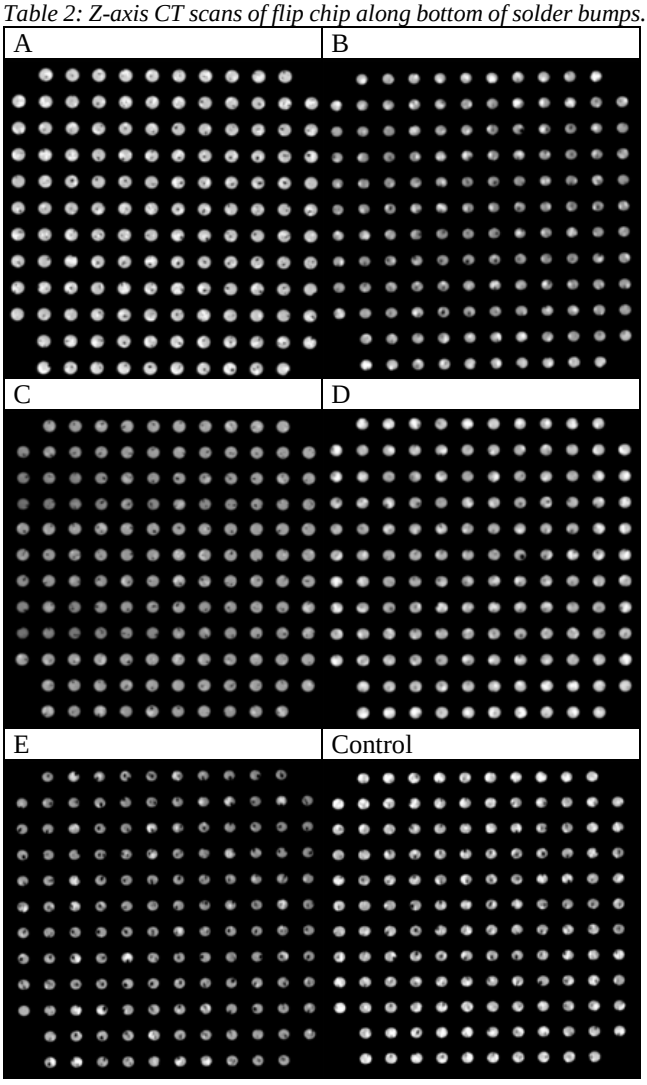


C. X-Ray Computed Tomography

Computed tomography (CT) x-ray imaging generates a 3-D model from a series of x-ray slices. CT scans were used to assess the percent voiding and to look for evidence of cracking in the first level interconnects of reball-simulated VSC3312 flip chips and an unprocessed SAC305 control.

In an X-Y plane scan, such as those shown in Table 2, a cracked joint would appear circular with jagged edges, while a good joint would appear circular with smooth edges. In an X-Z plane or a Y-Z plane scan, an example of which is shown in Figure 6, a crack would be visible through a slice of the solder joint, whereas a good joint would have no cracks [2]. The CT employed has a 6µm spot size and can detect features as small as 1.5µm. As each solder bump is ~0.65mm in diameter, fine cracks and defects would not be detected. No evidence of cracking of the solder bumps was seen in the X-Y scans, examples of which are shown Table 2, or the X-Z and Y-Z scans (not shown).

Table 2: Z-axis CT scans of flip chip along bottom of solder bumps.



CT results indicated voiding in the solder bumps of the VSC3312 flip chips from all reballers, as seen by dark spots in the bottom slice images presented Table 2. There is more voiding in the bottom of the solder bumps than the top, as can be seen in the sample Y-Z plane cut, shown in Figure 6.

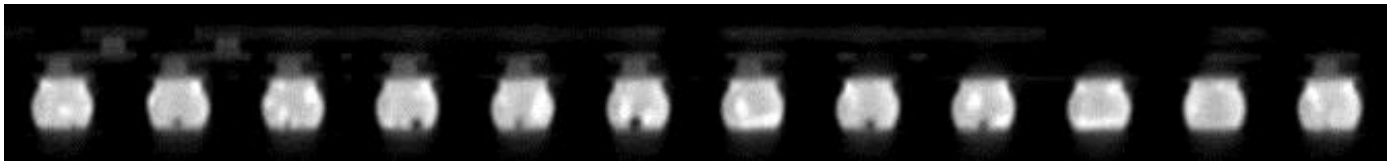


Figure 6: Example of a CT Y-Z plane cut through a row of solder bumps

The bottom slice images were threshold corrected in ImageJ to allow for estimation of percent voiding. An example of a threshold and filter processed image used to calculate percent voiding can be seen in Figure 7.

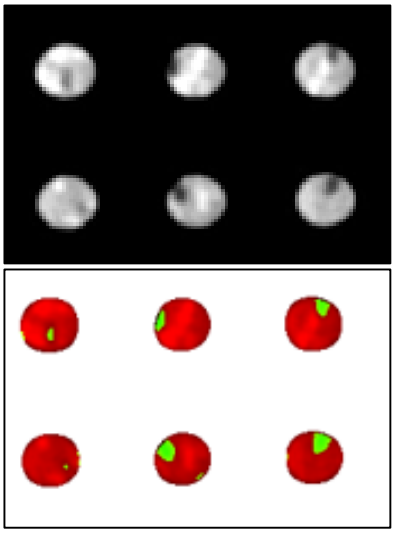


Figure 7: Detail of Z-axis CT scan at bottom of solder bumps in control (top), and processed for void measurement (bottom).

No specification exists for the amount of voiding deemed acceptable in first level interconnect solder bumps. IPC-A-610E states it is acceptable to have less than 25% voiding in a solder ball x-ray image. Despite the size and metallurgical differences between solder balls and bumps, the same mechanical principles should apply to both, and this metric is an acceptable guideline to indicate whether the voiding present in the solder bumps is a concern. After the simulated thermal events the VSC3312 flip chip experienced during reballing, the amount of voiding in the solder bumps was well below the 25% threshold and remained within two standard deviations of the mean, as displayed in Figure 8.

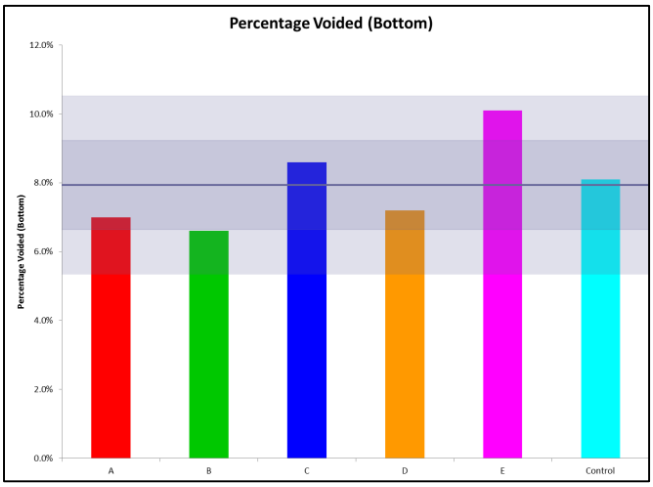


Figure 8: Percentage of cross sectional area voided, by reballer, with average voiding and two standard deviations indicated.

Bump voiding does not appear to correlate to reballing thermal stresses. Further study with thermal monitoring of the flip chips during reballing, and a larger sample size, would be necessary to confirm these findings.

IV. Conclusions

Damage was not observed to the first level interconnects as the result of reballing:

Resistance across solder bump connected input differential ports did not reveal any statistically significant changes in the conductivity of the paths. These measurements would be expected to change dramatically if cracking occurred in the bump joints.

Acoustic microscopy indicated that no delamination occurred within the packages during the reballing process.

No evidence of gross void formation or coalescence within the solder bumps was detected by CT. The control unit, which had not undergone reballing procedures, demonstrated voiding approximately equivalent to the average voiding observed for all samples scanned. CT inspection did not reveal any changes to the appearance of the solder bumps that would indicate cracking or damage accumulation in the 1st level interconnects.

Acknowledgment

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References

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