A Novel Thin Wafer Handling Technology to Enable Cost-Effective Fabrication of Through-Glass Via Interposers

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Abstract

Thin wafer handling technologies to fabricate silicon interposers have been widely discussed at conferences. Despite tremendous efforts to overcome several technical hurdles such as wafer chipping, cracking, and warpage, high manufacturing costs resulting from the complexity of the processes used to make silicon interposers remains a major concern.

Fabricating a through-glass via (TGV) interposer using novel thin wafer handling (TWH) technology will be presented here as an example of a simple and cost-effective solution for realizing 2.5-D IC integration. Utilizing a simplified TWH technology, a TGV interposer with 30-µm-diameter vias to eliminate the isolation layer is combined with polymer-based polybenzoxazole (PBO) as passivation to build one to two redistribution layers (RDLs) with 20-µm line width on both sides after thinning to 100 µm. The simplified TWH requires only a release layer on the glass carrier and another layer of bonding material on the TGV wafer to enable fabrication of a TGV interposer.

A process flow for fabricating a TGV interposer utilizing a simplified TWH technology will be presented in detail, including carrier treatment, bonding material, bonding, titanium/copper seed layer deposition, copper plating, RDL deposition, under-bump material (UBM) formation, debonding, and silicon chip stacking on a TGV interposer. The combination of TGV interposer and novel TWH technology will pave the way for cost-effective fabrication in 2.5-D IC.

Key words

Through-glass via (TGV), interposer, temporary bonding and debonding, thin wafer handling, 2.5-D IC integration

I. Introduction

Many papers and publications have documented the capabilities of silicon interposers to achieve 2.5-D stacking integration to minimize the mismatch in coefficient of thermal expansion (CTE) with silicon integrated circuits (ICs) [1]. Mature infrastructure in terms of equipment, process, and supply chain suggests silicon interposers are ideal for high-pin-count IC applications. However, cost-related issues such as size limitations of silicon substrates and the need for electrical insulation around via sidewalls for silicon semiconductor material are considered to be important issues for future high-volume manufacturing (HVM) production [2]. Thus, through-glass via (TGV) interposers are being introduced to answer cost concerns based upon several advantages, including their inherent insulating property, excellent insertion loss in high-frequency RF applications, and ability to extend to panel fabrication [3]. Several papers have already reported creating TGV interposers without copper through-silicon via (TSV) insulator through a 300-mm wafer process [4]. This paper focuses on demonstrating a simple temporary bonding and debonding technology with a TGV interposer wafer as a step toward realizing 2.5-D IC integration in panel-size fabrication.

II. Process Integration

A. Temporary bonding and debonding flow

Fig. 1 depicts a schematic process flow for achieving room temperature debonding where the thinned TGV interposer is protected at all times during debonding.

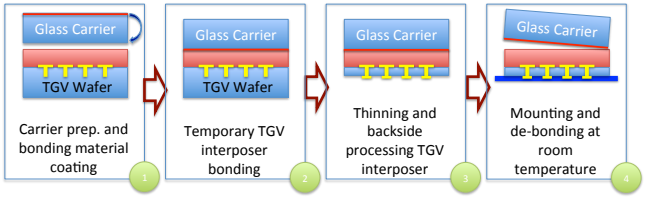

Fig. 1: Process flow for TGV interposer wafer thinning and processing.

First the bonding material is coated on a 300-mm TGV interposer wafer, which is then bonded, in a thermal compression bonder, to a glass carrier treated with a release layer beforehand [6]. The release layer, an organic polymer, is the only material required to treat the surface of glass carrier to enable lift-off debonding at room temperature. The carrier preparation process requires only spin coating and hot plate baking. The bonding material used in this study is designed to match the surface requirements of the release layer and to be compatible with metal pads, passivation materials, and topography to obtain void-free bonding. Moreover, the bonded pair experiences low warpage and has low total thickness variation (TTV) before backside processes (fig. 2). Most importantly, both the bonding material and the release layer remain stable in high-temperature thermal processes (fig. 3) and inert in harsh chemical environments. Finally, the treated glass carrier adhered on the surface of the bonding material is lifted off using a mechanical debonding tool while the thin TGV interposer wafer is protected by a film frame.

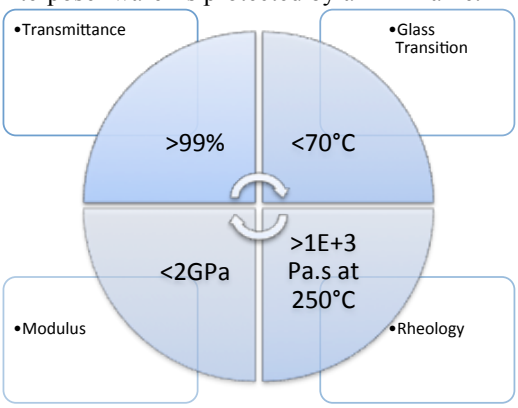

Fig. 2: Characteristics important to maintaining a good bonding stack and controlling warpage.

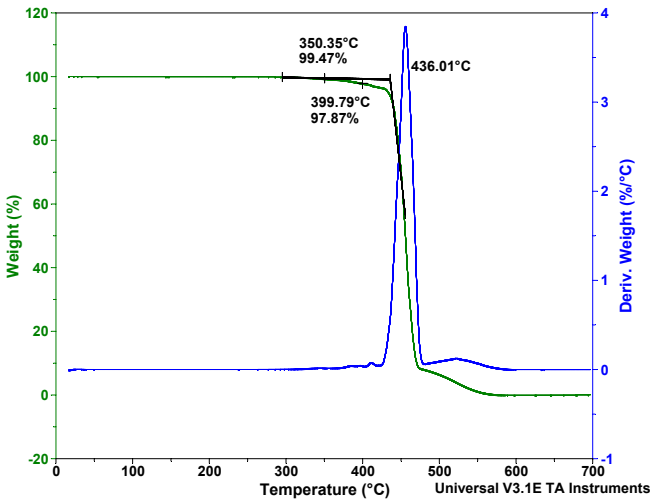

Fig. 3: Thermal gravity analysis of the bonding material indicates its thermal decomposition temperature is higher than 350ºC.

B. Glass interposer process flow

Glass interposer wafers, 300 mm in diameter and 700 µm thick, with more than 10,000 blind vias 30 µm diameter and 130 µm deep were prepared by Corning's proprietary process. An image of a TGV interposer wafer is shown in fig. 4 [5]:

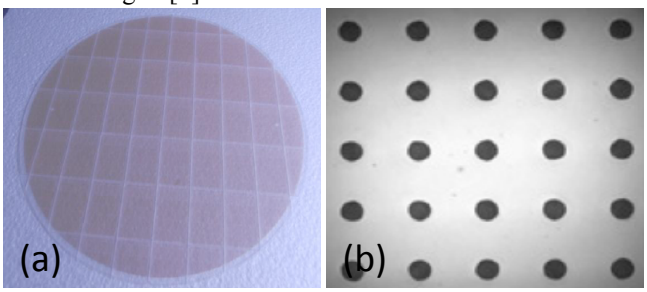

Fig. 4: Image (a) is an example of a 300-mm TGV interposer wafer, and image (b) shows vias with 30-µm diameter and 100-µm pitch.

Inspection by optical microscopy was required to ensure the TGVs had clean sidewalls. Copper plating with a bottom-up mechanism was then applied to minimize overburden on the TGV interposer wafer, subsequent to titanium barrier layer and copper seed layer deposition. Copper overburden and the titanium barrier were then removed by a wet etching process before the first top redistribution layer (RDL; line width of 20 µm, polybenzoxazole [PBO] cured at 200ºC) was applied. The same processes were repeated to form the second RDL before formation of top under-bump material (UBM), 15 µm in diameter, and copper/tin pillar, 4 µm and 5 µm thick, respectively.

A bonding material, 25 µm thick, with characteristics as shown in figs. 2 and 3, was applied on the front side of the TGV interposer wafer to bond it to the treated glass carrier, which is 300 mm in diameter and 500 µm thick, before thinning the TGV interposer wafer down to 100 µm by grinding and chemical-mechanical polishing (CMP) to reveal the copper TSVs. With PBO as passivation, one RDL on the backside of wafer and a bottom UBM, 85-120 µm in diameter, were fabricated.

The thinned TGV interposer wafer was then mounted on a film frame for protection before mechanical debonding at room temperature. The overall process in debonding was kept to less than 90 seconds to maximize throughput. The carrier can be reused after solvent cleaning, and the thinned TGV interposer wafer on the film frame after spray cleaning can be subjected to dicing.

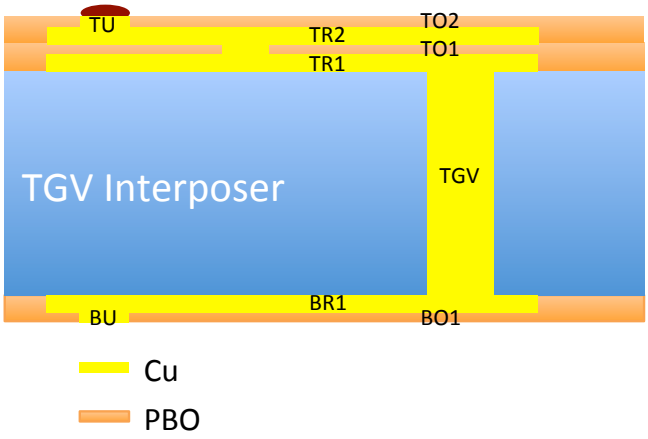

Fig. 5: The structure of glass interposer wafer [6].

III. Glass Interposer Wafer Fabrication Process

A. TGV interposer wafer front-side fabrication

A cross section of a TGV interposer wafer from Corning is shown in fig. 6. Each via has an aspect ratio of 4.3 with taper around 75°. The sidewall of each via must be residue-free before Ti and copper seed layer deposition [7].

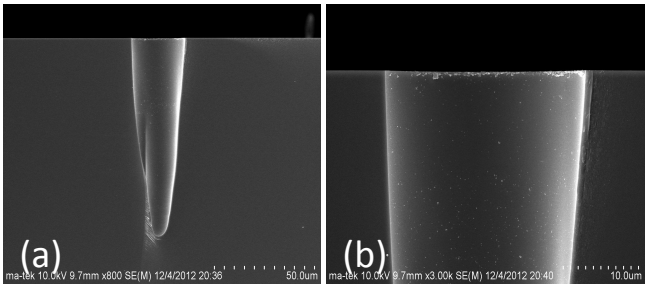

Fig. 6: Cross section of TGV.

It is critical to remove overburden after the copper plating process to ensure the TGV interposer wafer is flat. In this study, a gentle wet etching process was applied to minimize dishing on copper TSVs before RDL deposition.

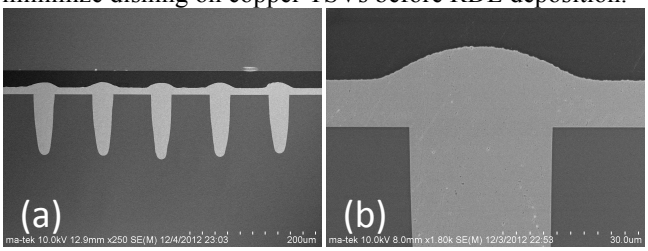

Fig. 7: Cross section of TGV with overburden.

B. Carrier preparation and bonding material coating

Glass carriers from Corning 300 mm in diameter and 500 µm thick were treated by spin applying a release layer from Brewer Science to adjust adhesion to the Brewer Science bonding material. The release layer is kept less than 10 nm to ensure it does not affect the TTV of the bonded pair.

Measurement	Average thickness	Average contact angle
Release layer	48.2Å	104°

Table 1: Thickness and contact angle of release layer on carrier.

Then Brewer Science bonding material was applied on the TGV interposer wafer with a spin speed of 1200 rpm for 30 s to create a 25-µm coating. After baking at 160ºC and 200ºC for 2 minutes at each temperature, the coated TGV interposer wafer was then placed onto the bonding platen to bond it with the glass carrier previously treated with the release layer. Temporary bonding was done under vacuum, 15 mbar, with a temporary wafer bonder, with 7,000 N of bonding force at 210ºC for 2 minutes to ensure no bonding material squeeze-out. The bond line could be visually inspected for any voids.

C. Backside grinding

During subsequent backside grinding and CMP to reveal copper TSVs, two TGV pairs bonded with silicon carriers were found with delamination and fly-out, respectively, in the grinding process, while the TGV pairs bonded with glass carriers passed grinding and CMP. CTE mismatch between the TGV interposer wafer and silicon carrier was considered to be the possible root cause of the delamination and fly-out. Both bonded pairs with a silicon carrier did not undergo further processing.

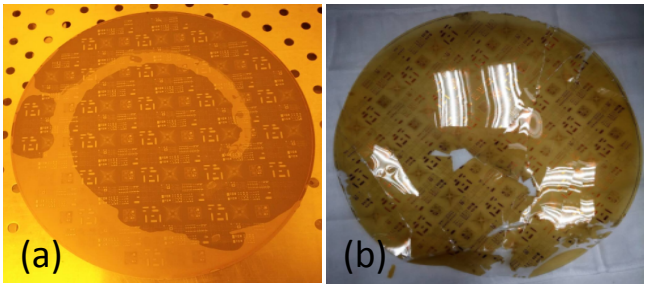

Fig. 8: Image (a) shows delamination exhibited by a TGV interposer wafer bonded with a silicon carrier, and image (b) is what remains of a TGV interposer wafer after it exhibited fly-out during the grinding process.

D. TGV interposer backside processes

Subsequent to backside copper RDL plating ~2 µm thick, PBO ~4 µm thick was applied to pattern backside openings, about 85 to 120 µm wide, through lithography processing. A 0.1-µm Ti barrier layer and a 0.3-µm Cu seed layer were then deposited by physical vapor deposition (PVD) before plating the copper pad, ~4 µm thick. Finally, photoresist (PR) was stripped and the seed layer was etched to complete backside processing.

Process	TTV (µm)	Warpage (µm)
After temporary bonding	3.39	84
After BR1 plating	1.45	187
Before de-bonding	1.49	149

Table 2. TTV and warpage of a TGV bonding pair with glass carrier in different step. (BR1 – backside redistribution layer 1)

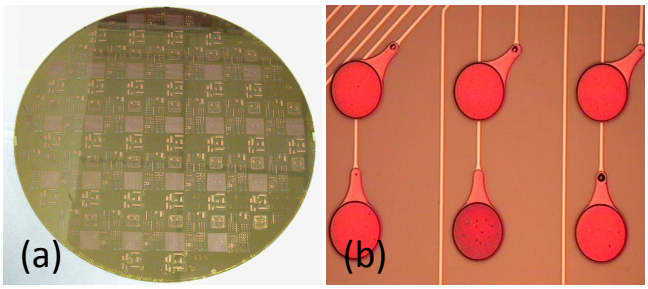

Fig. 9: Image (a) shows the backside of TGV interposer wafer on a glass carrier after backside processing. Image (b) shows its copper openings.

E. Debonding, cleaning, and dicing

Debonding was carried out in mechanical debonder at room temperature after mounting film frame. A metal tip was used to initiate separation at the edge of the interface between the glass carrier and the bonding material and the carrier was lifted off from the surface of the bonding material. Separating the surface of the carrier from the bonding material ensures minimal stress on the TGV interposer wafer during the debonding process. Fig. 10 shows that debonding was successful.

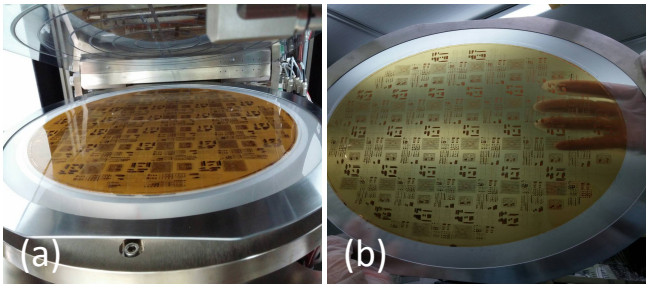

Fig. 10: Image (a) shows a TGV interposer pair with glass carrier face up in the debonding chamber, and image (b) shows a 100-µm TGV interposer wafer on a film frame.

The 100-µm TGV interposer wafer was then cleaned with a cleaning tool to remove bonding material. Cleaning was completed with pure D-limonene solvent through repeating spraying, puddling, and spinning off, without additional force being applied to minimize damage on the thinned TGV interposer wafer.

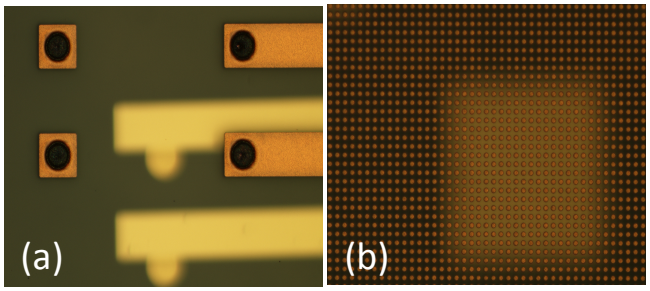

Fig. 11: Images (a) and (b) show the residue-free surface obtained after D-limonene cleaning via repeated cleaning steps.

Chips were diced, as shown in fig. 12, for further stacking trials. Details of stacking results will be presented in a future paper.

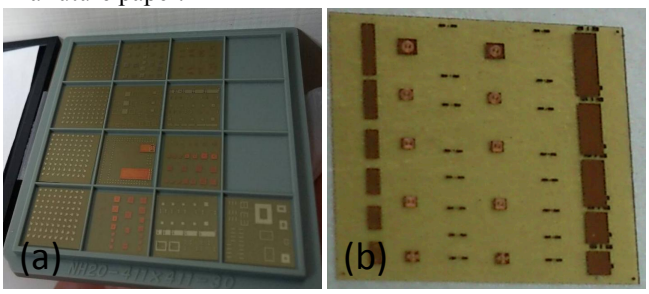

Fig. 12: Top view of TGV chips.

IV. Conclusion

A simplified temporary bonding and debonding solution was successfully implemented for fabricating TGV interposer wafers. With a single spin-coating step to treat the surface of the glass carrier, room temperature separation of the glass carrier from thinned TGV interposer wafer becomes possible. The survival through backside processes of the robust bonding material used to make the TGV bonded pairs was vital for the success of this study. All in all, seamless coordination among materials, equipment, and processes is essential for realizing 2.5-D IC integration. With this successful demonstration, evaluation on large panels will be carried out in the future for advancement of 2.5-D IC integration.

Acknowledgment

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