Development of a stress compensation layer for thin pixel modules 3D assembly

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Abstract

The pixel modules are the fundamental building blocks of the ATLAS pixel detector system used in CERN LHC facility. They consist in their basic form of a silicon sensor that is flip-chipped bonded to a CMOS read-out integrated chip (ROIC). One of the main objectives for the ATLAS experiment is to develop an approach towards low mass modules and thus reducing radiation length. From the module perspective this can be achieved by using advanced 3D technology processes that includes the formation of copper and solder micro-bumps on top of the ROIC front-side, the thinning of both the sensor and the CMOS ROIC and finally the flip chip assembly of the 2 chips. The thinning of the silicon chips leads to low bump yield at the solder reflow stage due to bad co-planarity of the two chips creating dead zones within the pixel array. In the case of the ROIC, which is thinned to 100um, the chip bow varies from - 100 µm at room temperature to + 175 µm at reflow temperature resulting of CTE mismatch between materials in the CMOS stack and the silicon substrate. Our objective is to compensate dynamically the stress of the front side stack by adding a compensating layer to the back-side of the wafer. Utilising our material thermo-mechanical database coupled with a proprietary analytical simulator and measuring the bow of the ROIC at die level we are able to reduce the bow magnitude by approximately a factor of 3 by the introduction of the compensating layer. We show that it is possible to change the sign of the bow at room temperature after deposition of a SiN/Al:Si stack. This amplitude of the correction can be manipulated by the deposition conditions of the SiN/Al:Si stack. Further development of the backside deposition conditions are on-going where the target is to control the room temperature bow close to zero and reducing the bow magnitude throughout the full solder reflow temperature range hence conserving bump yield. In keeping with a 3D process the materials used are compatible with Through Silicon Via (TSV) technology with a TSV last approach in mind should we integrate this technology in the future.

Key words

Pixel detector, Stress layer compensation, Thin chip, Warp management.

Introduction

ATLAS experiment (A Toroidal LHC ApparatuS) is part of the Large Hadron Collider (LHC) from CERN located near Geneva, Switzerland. This is a general purpose detector to be used to look for signs of new physics, including the origins of mass and extra dimensions. It will explore the fundamental nature of matter and the basic forces that shape our universe.

After a first demonstration of functionality which as lead to the experimental discovery of the Higgs boson several upgrades are planned to go further in the capability of the system. For the high luminosity upgrade of LHC around 2022 (HL-LHC) a complete new Inner Detector is necessary to cope with the increased luminosity of $5x10^{34}$ $cm^{-2}s^{-1}$. In this context also a new pixel detector has to be developed which can fulfill the challenging requirements. New technologies like 3D packaging of integrated circuits, new smaller electronic processes and new sensor technologies apart from standard silicon have to be considered. This comes also with the introduction of the new ROIC chip generation called FEI4 replacing the current FEI3 chip with the former fabricated on a IBM 130nm process.

One of the main objectives for the pixel upgrade is to develop an approach towards low mass modules and thus reducing radiation length. This comes with the reduction of the thickness of the silicon of both the detector tier and the ROIC tier which are flip-chip mounted together by solder µbumps. This can be achieved by thinning both the sensor and the CMOS ROIC. The thinning of these chips leads to low bump yield due to bad co-planarity of the two chips (26,880 bumps in 80 columns) during the solder reflow stage.

Most of the warp is generated from the ASIC tier in particular the thick metallization BEOL stack. One approach considered to solve this issue is to develop an alternative wafer level back-side process that compensates for the CTE mismatch of the front-side stack. This approach has been developed at CEA-Leti previously in the case of large high density interposers with dense copper damascene BEOL lines [1].

Micro-bump process development used for flip chip technology and wafer thinning down to 100 µm will be also presented in this paper.

Architecture & Technology

A. Pixel detector for ATLAS experiment

The center part of the ATLAS experiment which is only few centimeters from the proton beam axis and extends over 6.2 meter in length is composed of 3 concentric parts: the Transition Radiation Tracker (TRT), the Semi-Conductor Tracker (SCT) and the Pixel detector.

The pixel detectors are the innermost part of the detector and are subjected to very high level of radiation. It contains three concentric layers and three disks on each end-cap, with a total of 1,744 modules, each measuring two centimeters by six centimeters. The detecting material is constituted of 250 µm thick silicon. Each module contains 16 readout chips and other electronic components. The smallest unit that can be read out is a pixel; there are roughly 47000 pixels per module.

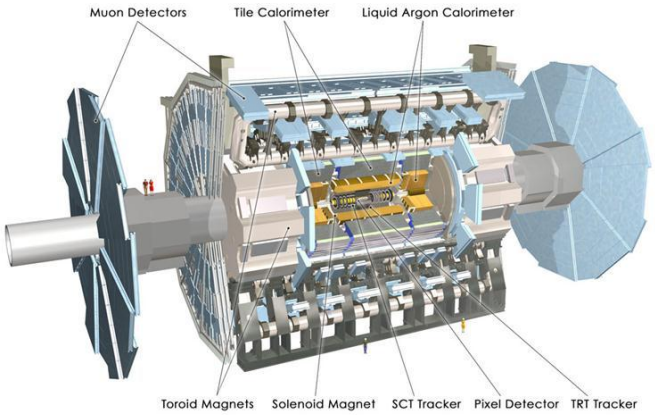

Figure 1: ATLAS experiment schematic showing the different modules.

Two phases of upgrades are planned for the ATLAS experiment [2]:

- Phase 0: Insertable B-layer (IBL): 2013-2014

This new innermost pixel barrel layer was installed in 2014, while the rest of the pixel detector stayed in place. This new b-layer called IBL will be located even closer to the interaction point at R = 3.7 cm than the current b-layer and therefore has to cope with much higher data rates and radiation load. The new ROIC chip called FE-I4 which is a direct successor of the currently used FE-I3 chip will be used.

- Phase 1: Upgrade of the ATLAS pixel detector (>2022)

For the high luminosity upgrade of LHC around 2022 (HL-LHC) a complete new Inner Detector is necessary to cope with the increased luminosity of $5x10^{35}$ $cm^{-2}s^{-1}$. In this context also a new pixel detector has to be developed which can fulfill the challenging requirements. New technologies like 3d packing of integrated circuits, new smaller electronic processes and new sensor technologies apart from standard silicon have to be considered. The work presented in this paper is targeted for this upgrade.

The new FEI4 pixel ROIC [3] (Figure 2) is more than 4 times larger than the previous one and the number of pixels is close to 10 times higher.

	FE-I3 (ATLAS exp.)	FE-I4 (ATLAS IBL)
Width [cm]	0.7	2.0
Length [cm]	1.1	1.9
Chip Size [mm²]	82.08	383.8
Active Area [cm²]	0.58	3.36
Num. pixels	2880	26880
Technology [nm]	250	130
Active Fraction	74%	89%
Rad.-hardness [MRad]	>200	>50
Analog Current [µA/pix]	26	10
Digital Current [µA/pix]	17	10
Analog Voltage [V]	1.6	1.5
Digital Voltage [V]	2	1.2

Figure 2: Main characteristics of pixel detector ROIC comparing current version FEI3 and new version FEI4.

B. FEI4 ROIC process flow

The FEI4 chip is processed with a 130 nm node CMOS technology ending with one layer of 4 µm thick aluminum metal as shown in Figure 3. This very thick BEOL stack is likely to have a prominent contribution in the stress of the front side technology which leads to high warpage of the chips.

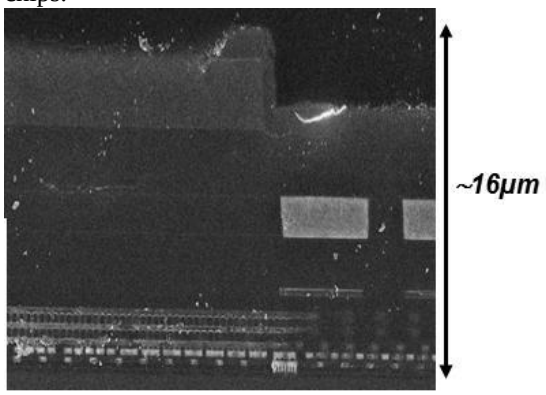

Figure 3: SEM cross section of the FEI4 chip showing the thick metals at two uppermost levels.

Figure 4 describes the process flow followed in this work.

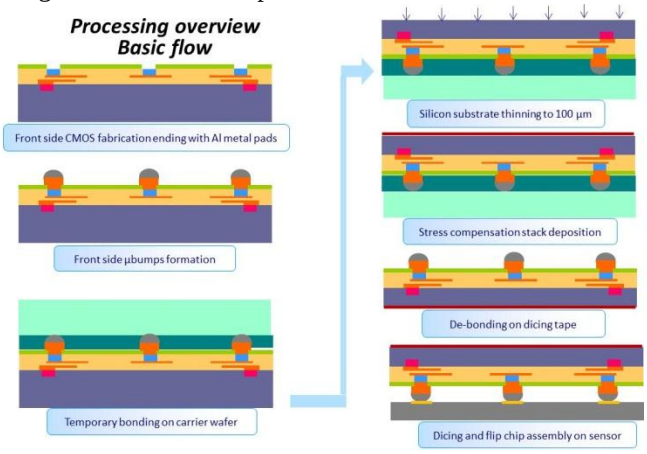

Figure 4: Basic post-processing flow for ROIC FEI4 chips.

It consists of four main steps: fabrication of the micro-bumps for subsequent flip-chip assembly on the sensor tier, thinning of the ROIC wafers to 100 µm using a substrate carrier and a temporary bonding process, deposition of the stress compensation stack on the wafer back side and finally de-bonding and dicing of the wafer.

C. Temporary bonding technology

A thermoplastic glue from Brewer Science (type BSI) with thickness of 30 µm and ZoneBond™ [4] technology have been used for temporary bonding on glass carrier wafers. This technique allows thinning the active wafer to extremely thin thickness and then de-bonding is achieved at ambient temperature and with a low mechanical force using chemical dissolution of the glue on the edge of the wafer thanks to the anti-sticky surface deposited on the carrier wafer before bonding.

D. Wafer thinning

Wafer thinning consists in a two steps grinding process (Z1, Z2) followed by a Chemical Mechanical Polishing (CMP) step to remove the damaged silicon layer and relieve the stress from the grinding operation and a mirror finish surface. Final thickness of 100 microns was obtained on all the FEI4 wafers processed with a TTV of about 6 microns.

Characterization methods

A. Wafer bow measurement

Wafer bow measurement was carried out using laser scattering method on a KLA FLEXUS instrument. Measurements can be performed at even intervals of time while the wafer is submitted to thermal cycles to determine the deformation change with the temperature.

The biaxial stress of the deposited film at a given temperature can be calculated with the Stoney model (1) where R_0 and R are the radii of curvature of the wafer respectively before and after deposition of the film, (E_s) is the elastic modulus of the substrate (silicon), υ_s its Poisson ratio, t_s is the thickness of the substrate and t_f thickness of the film.

$$\sigma_{film} = \frac{E_s}{6(1-\nu_s)} \cdot \frac{t_s^2}{t_f} \cdot \left(\frac{1}{R} - \frac{1}{R_o} \right) \quad (1)$$

The equipment is equipped with an in-situ furnace, which allows us to heat the wafer with a controlled temperature ramp. The mean stress in the deposited layer is obtained by using the bow variation of the wafer before and after the deposition step and during thermal loads.

B. Die level bow measurement with confocal microscopy

For thin die bow measurement, FRT Microprof tool equipped with a double chromatic confocal sensor has been used. This equipment can measure bow, warp, TTV but also making 3D reconstruction of chip profile by measuring surface topology with an accuracy of 40nm (Figure 5).

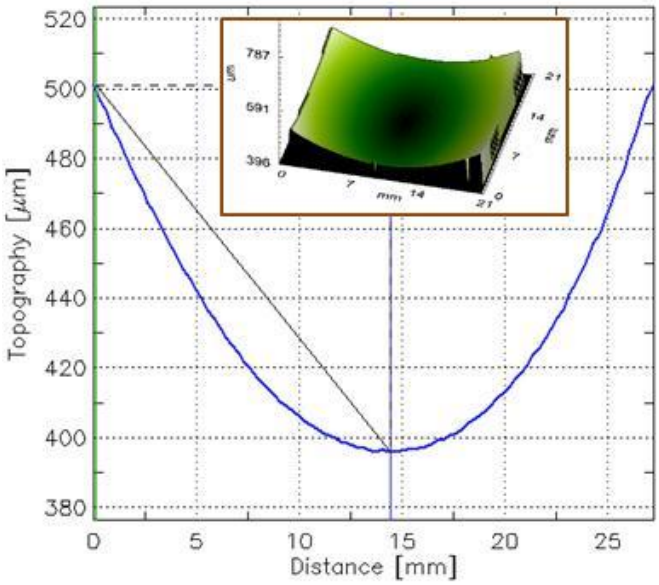

Figure 5: FRT measurement 2D and 3D profiles of individual chip.

C. Nano-indentation for thin film elastic modulus determination

Elastic moduli (E) of the thin films are determined using nano-indentation technique with a nano-indenter from MTS, (model XP). The method used is CSM (Continous Stiffness Measurement) with a diamond Berkovich type tip [5]. Two values of the modulus can be extracted from this measurement, the polynomial fit of the experimental curve and the value at 10% of displacement which is typically higher. In this work we utilize the value of this polynomial fit. Film hardness (H) can be also determined with this technique.

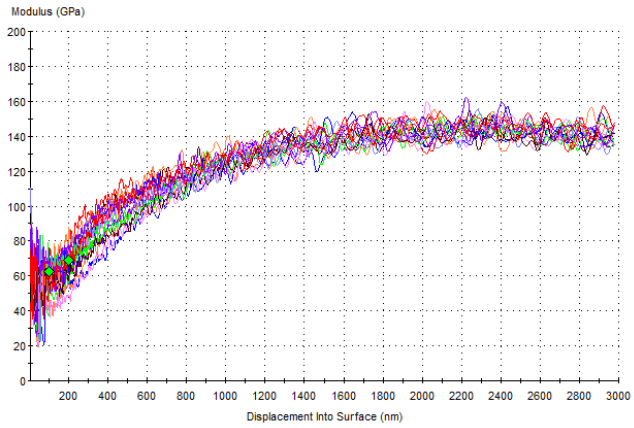

Figure 6: Young modulus determination by nano-indentation of a 2 µm AlSi film deposited at 175°C.

D. Topography and Deformation Measurement (T.D.M.) under thermo-mechanical load

This characterization was carried out using TDM-HR equipment from Insidix which has a full-field and fast acquisition mode of the optical deformation of the sample dies under thermal load (Figure 7). Temperature of the sample is

imposed with infrared heating on top and bottom sides of the samples.

The out of plane resolution of the optics is ±3 µm and in-plane (x, y) detection ability is $\Delta L/L = 5 \times 10^{-5}$.

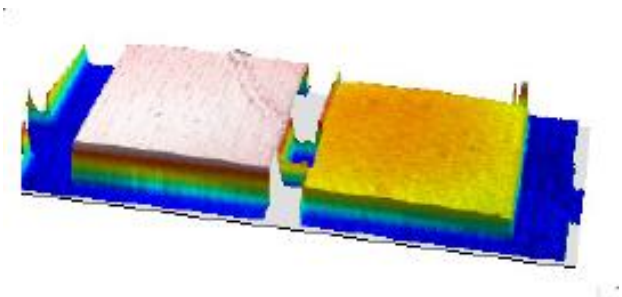

Figure 7: 3D view of 2 chips with the TDM measurement camera.

E. Analytical thermo-mechanical simulation

For calculation of the wafer deformation after each deposition step of one stack an analytical model has been developed internally [6]. The entry parameters are the thermo-mechanical properties of the deposited layer (Elastic modulus, young modulus and coefficient of thermal expansion), the temperature of deposition, the thickness of the films and also the intrinsic stress of the films. All these parameters are determined for each layer experimentally with the aforementioned methods. Unlike the Stoney approach that does not take into account the elastic properties of the deposited thin film to evaluate its average stress, our analytical approach takes into account the whole history of the multilayers system including the processing conditions of each layer. This full analytical model allows us to estimate the stress distribution in a multi-layered structure whatever are the ratio between the films and substrate thicknesses. In particular, the thinning of the silicon substrate is incorporated in our description.

Results and discussions

A. Micro-bump fabrication

The micro-bumps are formed on top of the aluminum pixel pads by using a conventional semi-additive process through a negative tone resist. Ten microns of copper followed by eight microns of SnAgCu 305 are grown by electro-chemical deposition over a seed layer of Ti/Cu deposited by physical vapor deposition (PVD). After stripping the resist the seed layer stack was etched by wet chemistries. The main issue observed with this process was to remove all the seed material. This was particularly problematic with the Ti layer in the dense area of the pixel matrix (see Figure 8 and Figure 9) with a minimum space of 30 microns. The surface also has a large topology shielding metal surrounding the pads.

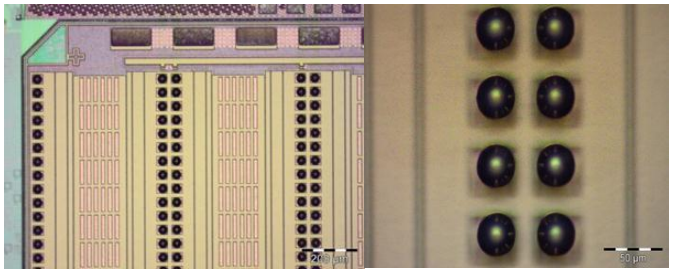

Figure 8: Microscope views of FEI4b Cu/SAC Micro-bumps.

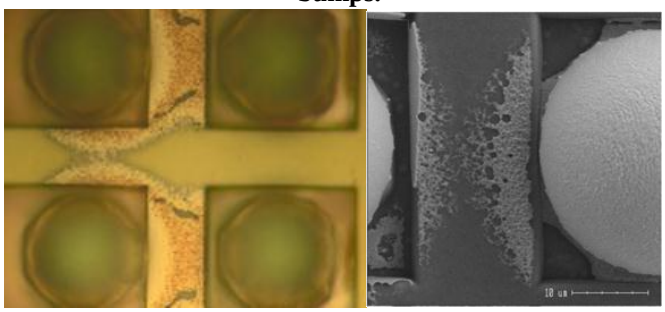

Figure 9: Seed layer residues inside pixel matrix.

After some optimization of the seed etching process which consisted of limiting the Ti layer thickness and control of the over-etching, metal residue was significantly reduced as illustrated by Figure 10.

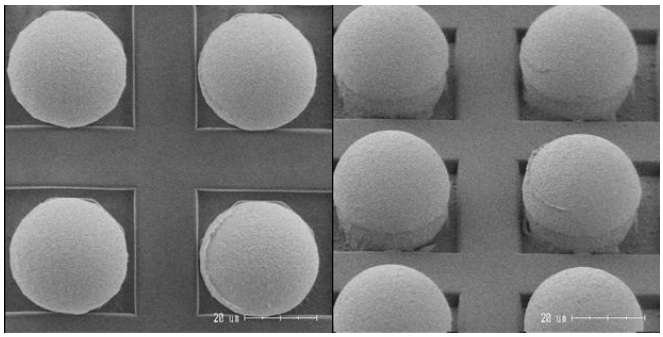

Figure 10: SEM observation of micro-bumps grown in FEI4 pixel matrix after seed process optimization.

Last we have characterized the influence of the micro-bumps on the FEI4 wafer stress by measuring the bow of the wafer before and after realization of this technology. Measurements were conducted on thick CMOS wafers prior to micro-bump formation and a bow of 8 to 20 µm was observed. Post bump deposition a bow of 25 to 44 µm was found corresponding to a compressive contribution of this technology of about 20 µm, representing an equivalent impact than the overall CMOS technology stack.

B. Material selection for back side stress compensation layer (SCL)

In order to determine the stress compensation to apply on the backside of the ROIC, we have first characterized the bow of bare FEI4 dies thinned to the desired thickness of 100 µm using TDM and confocal FRT (only at ambient temperature) techniques as depicted in Figure 11. The sample has been submitted to two identical thermal cycles in a row from

ambient temperature to solder reflow temperature (260°C). Note that in all this study we will always refer to the bow taken from the back side of the wafer or of the die. Before any thermal excursion the chip is concave with a bow of +50 microns well in accordance with previous measurements obtained at a thickness of 150 microns [7]. During heating, we observe a first linear regime up to about 100°C where the bow starts to decrease and becomes negative to reach -120 microns, then a second asymptotical regime up to 260°C where the bow continues to decrease smoothly to a minimum of -175 microns. During cool down we observe also two subsequent regimes, the first between 260 and 150°C with a strong decrease of the bow followed by a second regime from 150°C to ambient with a slower rate ending to + 100 µm. During the second cycle the behavior is identical, starting from the new origin and with a temperature shift of the linear portion of the heating curve, then during cool down the values are identical to the first cycle.

Additionally, 3D images captured during the temperature cycle (Figure 11) allow the type of the chip deformation to be determined, which is in this case is spherical specifying, the model to adopt for the simulation.

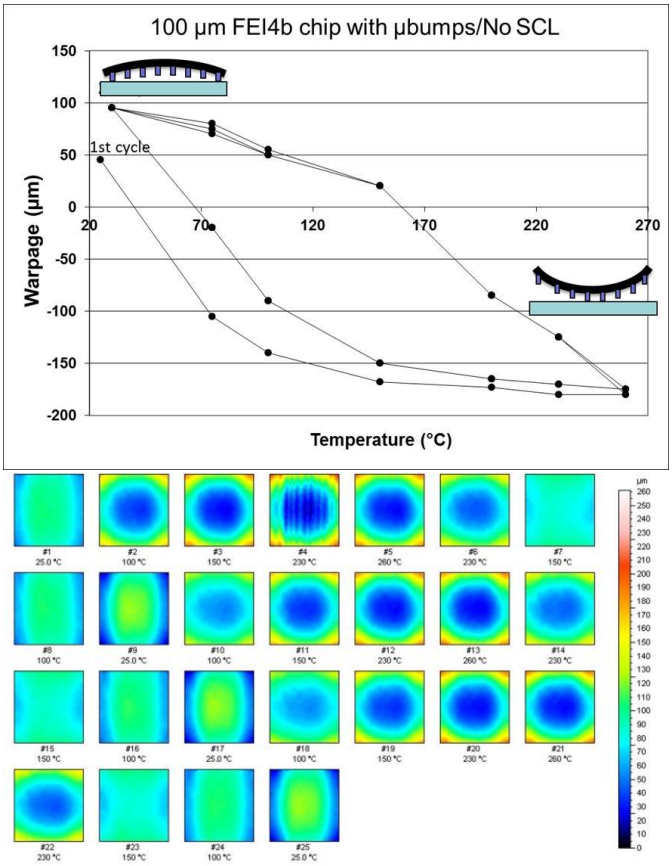

Figure 11: Bow variation with temperature measured by TDM of 100 µm thick FEI4 chip. Measurement is done on back side of the chip.

When analyzing the origin of the stress inside the front side technology it was quite predictable that one of the main contributors would be the thick aluminum metal level built on top of the copper BEOL stack. This observation is corroborated by the stress behavior of aluminum based (Al-Si or Al-Si-Cu) metallization deposited on silicon substrate reported in [8] which is very similar to the measurement shown in Figure 11. On heating, up to 90°C, the first regime corresponds to the elastic deformation of the metal driven by the differential coefficient of thermal expansion between the aluminum and the silicon, the plateau regime corresponds to the plastic deformation or yielding of the metal for high stress values. The same behavior is observed on cooling with a first elastic regime followed by the starting of some yielding below 150°C.

Based on this observation, Al-1 wt. % Si material has been considered as the ideal candidate to be used as the main thermo-dynamical compensation layer for the ROIC FEI4 chip. In addition a PECVD SiN film will be used as dielectric for electrical insulation of the metal layer from the substrate back side. The SiN layer also has the capability to have its stress tailored in a large range of values from compressive to tensile by tailoring the power of the mix RF frequency generator [9]. Hence, the intrinsic stress of the SiN layer the static deformation of the chip can be offset close to zero. Additionally, all depositions on back side need to be made at a temperature not exceeding 200 °C to be compatible with the temporary bonding. Al-Si deposition is carried out by PVD at chuck temperature of 175 °C and SiN deposition is done by PECVD at 200°C. In order to enhance the adhesion between the SiN and the Al-Si films a thin layer (20 nm) of PVD titanium was deposited. This layer has a minor contribution the SCL overall stress.

Based on the choice of these two materials for the compensation layer we have characterized their thermo-mechanical properties in order to be used in our analytical simulator. Elastic moduli are determined by nano-indentation, Poisson coefficient are taken from literature data [http://www.matweb.com/] and CTE are extracted from the elastic regime of σ(T) using (2) from bow measurement characterization (Figure 12 and Figure 13).

$$\sigma_{film} = \sigma_{Si} - \frac{\Delta\sigma}{\Delta T} * (1 - \upsilon_{film})/E_{film} \qquad (2)$$

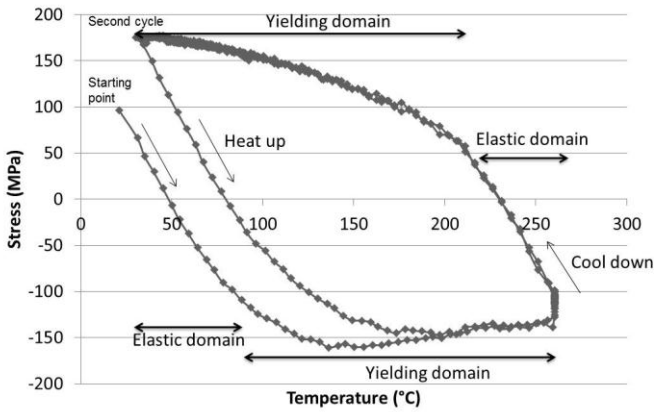

Figure 12: Stress evolution with temperature of 2 µm Al-Si film deposited on 730 µm silicon substrate.

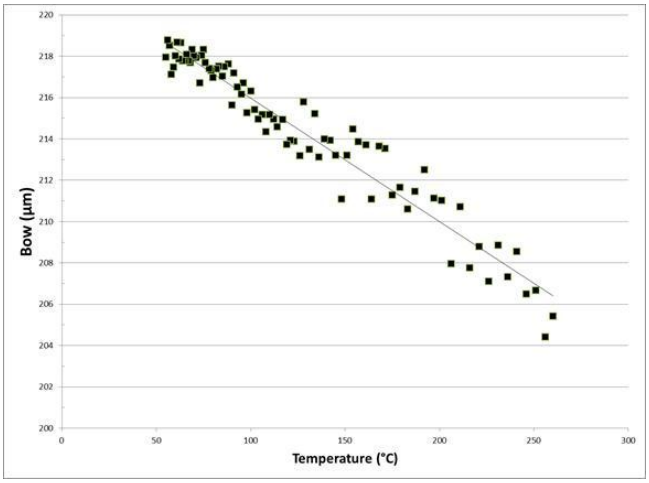

Figure 13: Bow evolution during heat up of 2 µm compressive SiN film deposited on 450 µm silicon substrate.

All the values are reported in Table I. Note that for low temperature SiN film the elastic modulus is lower than standard silicon nitride film. Also CTE of this layer is very close to the silicon one which indicates that SiN will not contribute much to the dynamic compensation.

For Ti/AlSi stack deposited on SiN layer an equivalent model has been considered which keeps the same modulus and CTE than the AlSi layer but with an intrinsic stress set at 50 MPa.

Table I: Measured thermo-mechanical characteristics of studied materials.

	Elastic modulus (E) (GPa)	Poisson coefficient (υ)	CTE (K^{-1})	Intrinsic stress (MPa)
Comp. SiN	135	0.25	2.7	- 176
Al-1% wt. Si	66	0.36	19.6	+ 80

To compensate the stress of the front side chip at ambient temperature compressive stress needs to be applied first. Since Al-Si is also tensile, a high compressive SiN layer needs to be deposited first to compensate both contributions. Therefore compressive SiN layer will allow adjustment of the deformation closer to zero at low temperature by tuning the thickness and its intrinsic stress. The Al-Si layer will then act to compensate during the thermal excursion due to its high CTE but limited by the yielding effect over 90°C. The thickness of the Al-Si is then used to adjust the intensity of the dynamic compensation. Based on these layer properties a SiN/Ti/Al-Si stack has been first estimated with 0.5 µm of SiN and 4 µm of Al-Si.

C. Die level bow compensation layer characterization with temperature.

First deposition trials were made directly on individual thin FEI4 chips with the µ-bumps on the front side to confirm the compensation effect of the SiN/Ti/Al-Si stack. Figure 14 shows a first result using SiN 0.5 µm compressive/Ti 20 nm/AlSi 4µm. Compared to the non-compensated chip of Figure 11 the bow at ambient temperature has been reduced from +100 to – 60 µm and the amplitude of the deformation during the heating was reduced from 275 to 85 µm. This first result is already very promising but further optimization is necessary to reduce the bow offset at ambient. This can be achieved by increasing the SiN thickness and to reduce the amplitude of the deformation during heating by increasing the Al-Si thickness. From the simulation work the optimum conditions can then be extrapolated to give the layer stack: compressive SiN 2 µm/Ti/6 µm Al-Si.

This assumption presumes that the deposition conditions are same on thin individual chips supported on a silicon holder rather than deposition directly on a silicon substrate. Both approaches may result in differences in the measured values considering, in particular, the actual temperature of deposition but also some possible edge effect. Also nonlinear effects may occur for thicker deposited layers due to stress relaxation inside the film and possible loss of adhesion at the interface if the stress becomes too high. This phenomenon has been effectively observed with a deposition of 5 µm of Al-Si which exhibit some delamination from the substrate and no improvement in the compensation effect compared to 4 µm.

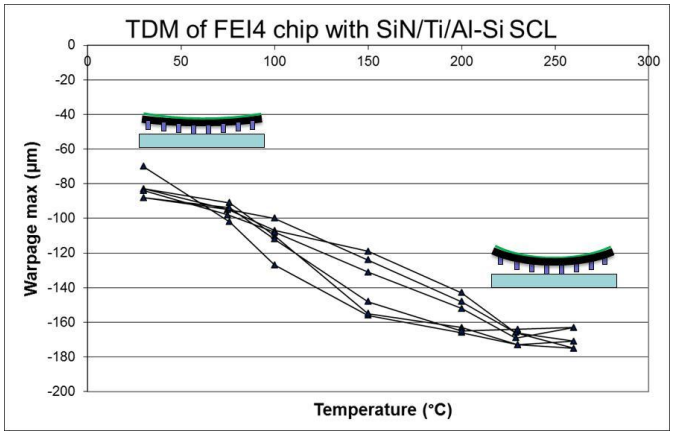

Figure 14: TDM measurement on an individual FEI4 chip with 0.5 µm C SiN /Ti/4 µm Al-Si stress compensation layer stack.

Conclusions

The reduction of the ROIC silicon thickness used in high energy particle detectors leads to an important warpage issue in particular during the flip chip assembly process occurring at relatively high temperature. The chip deformation is intrinsically due to the stress of the front side CMOS stack constituted in particular for this technology by two thick aluminum metal layers at the upper interconnect levels. Also the fabrication of Cu/SnAg solder micro-bumps used for the flip chip technology on top of the CMOS was found to bring a significant contribution to the overall stress.

Thus, the objective of this study was to develop a solution to compensate dynamically the deformation of the chips with

temperature by applying a stress compensation layer applied at the wafer level on the backside of the substrate after thinning to 100 microns.

The development of our solution was supported with three main activities: the characterization of the film thermo-mechanical properties, the construction of a model for the deformation response with the temperature and several loops of experimental trials to fine tune the compensation result.

After selection of the potential candidates, the compensation layer was determined using a stack of two different materials each having a specific role in the compensation response. First a layer of silicon nitride was applied for which the stress of the film can be adapted from tensile to compressive to minimize the chip deformation at ambient temperature. Second an Al-Si layer was deposited to act dynamically with the temperature thanks to its high coefficient of thermal expansion.

Finally, using our stress layer compensation solution, the static chip bow can be strongly reduced as well as the dynamic chip deformation. Few more optimization loops still need to be conducted to achieve the lowest possible bow amplitude. Based on these very promising results the next step will be to apply this stack on a real FEI4 wafer after µ-bumps formation and thinning.

Additionally this solution is fully compatible with the fabrication of the sensor module. Additionally, this work demonstrates the benefits of introducing smarter backside technology as TSV-last which can equilibrate the stress of thin chips while adding breakthrough functionalities to the devices.

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