Lithography Process Optimization for 3D and 2.5D Applications

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Abstract

Lithography process optimization is a key technology enabling mass production of high-density interconnects using 3D and 2.5D technologies. In this paper, Canon continues its investigation of lithography optimization of thick-resist profiles and overlay accuracy to increase process margins for Through-Silicon Via (TSV) and Redistribution Layer (RDL) applications. Canon will also provide updates on the FPA-5510iV and FPA-5510iZ i-line steppers that are gaining acceptance as high-resolution, and low-cost lithography solutions for aggressive advanced packaging, 3D and 2.5D applications also preliminary data illustrating 450 mm wafer process challenges.

Key words

Lithography, 450 mm, stepper, IR Alignment, bonded wafer

I. Introduction

In this paper, Canon lithography solutions that optimize alignment and exposure performance for 3D and 2.5D applications are explained in detail. Canon has identified many key factors related to equipment and materials optimization that affect 3D and 2.5D manufacturing processes.

Key lithography process requirements for 3D and 2.5D applications is provided in Figure 1 and include accurate processing of severely warped and distorted bonded wafer stacks. Wafer warpage will increase as TSV usage and dense backside wiring usage rise. Due to the additional metal used for dense TSV arrays and Redistribution Layers (RDL), a larger mismatch in the Coefficient of Thermal Expansion (CTE) is experienced, causing stress and warpage.

Canon has developed the FPA-5510iV and FPA-5510iZ-TSA steppers to support high-density processes and to provide performance and functions to support implementation of 3D and 3.5D technology.

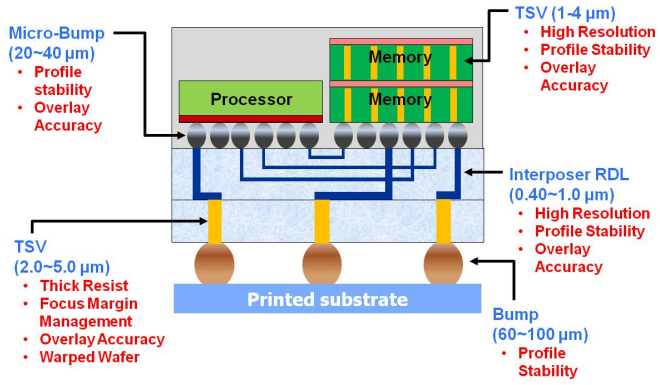


Figure 1: 3D & 2.5D Lithography Process Requirements

The FPA-5510iV delivers good imaging profiles through thick resist, the ability to perform accurate backside alignment, while the FPA-5510iZ provides even superior resolution and overlay to support the most aggressive TSV last processes. A comparison of key specifications and features of the FPA-5510iV and FPA-5510iZ are provided in Table 1.

Table 1: Canon TSA Stepper Specification Comparison

Benefit	Item	FPA-5510iV Specification	FPA-5510iZ-TSA Specification
Imaging	Red. Ratio / Field Size	2:1 / 52 x 34mm	4:1 / 26 x 33mm
	Numerical Aperture	0.10-0.18	0.45-0.57
	Sigma	0.40-0.80	0.40-0.75
	Resolution	≤ 1.5µm L&S (≤ 1.0µm, off-axis illum.)	≤ 350nm L&S (≤ 280nm, off-axis illum.)
	DOF	≥ 10µm (@ 1.5µm) ≥ 6µm (@1.0µm)	≥ 1.2µm (350nm)
Alignment	Backside Alignment Option	Through-Silicon Alignment (TSA)	Through-Silicon Alignment (TSA)
	Overlay Accuracy (w/ *TSA Option)	≤ 0.300µm (front) ≤ 0.300µm (back)	≤ 100nm (front) ≤ 200nm (back)
Options	Shot-by-Shot Compensation	EAGA (Enhanced AGA)	EAGA (Enhanced AGA)
	Front-to-Back Overlay Metrology	D-Map (Dual-Side Metrology)	D-Map (Dual-Side Metrology)
	Warped Wafer Handling	≥ 450µm	≥ 450µm
	Wafer Edge Applications	WES (shield) WEE (expose)	WES (shield) WEE (expose)
	Thick Resist Processing	Resist Outgas Unit	Resist Outgas Unit

In a typical backside manufacturing process, patterned process wafers are bonded, face down, to a support wafer before being ground and thinned to a thickness a small as a few microns. The bonding and thinning process causes large distortion in the wafer that results in shot shape deformation. Downstream processes require lithography systems to produce patterns that accurately overlay distorted shots with high accuracy. Essentially, the stepper will be required to "distort" a "perfect" image to match the pattern existing on the wafer. Overlaying distorted wafers is a key technical challenge that must be overcome to provide high productivity and yield.

To provide accurate backside overlay of a bonded wafer stack, Canon steppers including the FPA-5510iV utilize the infrared Through-Silicon Alignment (TSA) System to measure wafer grid distortion using infrared (IR) light as the alignment light source. The TSA System IR light can be used to measure alignment marks on the back side of the wafer through silicon. An illustration describing the optical theory behind the TSA Scope is provided in Figure 2 [2].

Semiconductor exposure equipment generally employ a global alignment system that measures several sample shots on a wafer and calculates linear compensation factors for shift, rotation and magnification. The standard Canon stepper wafer fine-alignment sequence is known as Advanced Global Alignment (AGA). AGA compensation values are based on linear compensation models derived from the AGA measurement data and with severely distorted wafers, overlay alignment using linear compensation variables only can be challenging.

Non-linear errors caused by wafer distortion in backside processes have become a large technical challenge for high volume production and advanced alignment techniques are required to overlay accurately. For severely distorted wafers, the linear compensation provided by AGA compensation may not provide sufficient overlay across the entire wafer and/or across individual exposure fields and advanced shot-by-shot compensation by the stepper may be required. Canon steppers can to provide shot-by-shot compensation through the advanced alignment sequence known as Enhanced Advanced Global Alignment (EAGA). During the EAGA sequence the TSA System measures alignment marks within each accessible shot on a wafer. By evaluating multiple intra-field alignment marks in each field, actual shot shift, shot magnification and shot rotation may be measured and compensated. The shot information is used to control the position and rotation of wafer stage and the magnification of projection optics during the wafer exposure sequence.

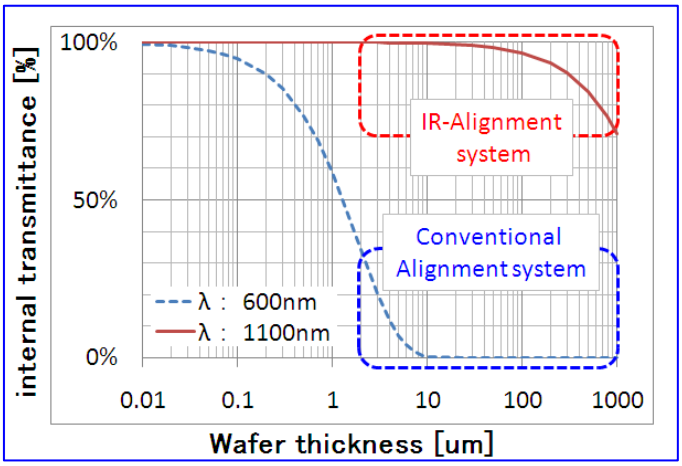


Figure 2: IR Alignment System allows backside alignment to targets under silicon

The stepper must accurately measure and apply large compensation amounts to correctly overlay distorted wafers. Standard compensation factors that are corrected to optimize overlay include shot shift, shot rotation and shot magnification. Extreme magnification conditions require accurate magnification or demagnification of the reticle pattern to match the existing fields on the wafer.

Wafer handling and depth of focus optimization is also accomplished through application of Canon stepper vacuum assist functions. Canon steppers have experience with a large range of warpage and bow conditions and the stepper can apply counter measures to improve wafer flatness after vacuum locking the wafer to the chuck. Information regarding Canon stepper warpage tolerances and system options are provided in Figure 3.

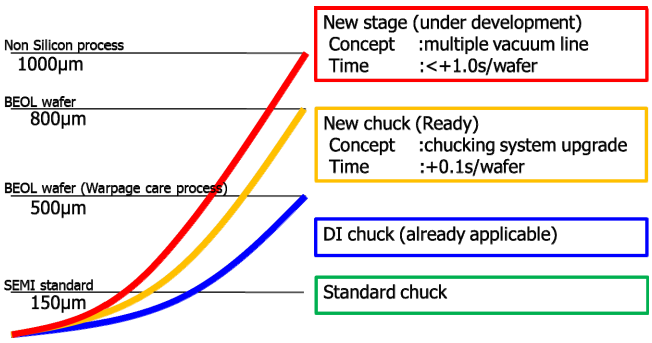


Figure 3: Canon Lithography Systems employ vacuum assist functions to compensate for large wafer warpage

Results and Discussion

Canon research has observed over 1,000 nm of pattern grid distortion between top and bottom wafers in 300 mm bonded wafer stacks, with over 200 nm variability between wafers. Advanced overlay compensation techniques must be applied by the stepper to properly overlay such distorted wafer grids.

EAGA compensation simulations have been conducted to estimate the effect of applying shot-by-shot compensation to severely distorted wafers exhibiting large amounts of wafer and intra-field distortion. A comparison of conventional linear AGA compensation and shot by shot EAGA overlay performance is shown in Figure 4. The data illustrates that distorted wafer overlay can be reduced by over 60% to meet the accuracy level required for dense 1 µm TSV fabrication.

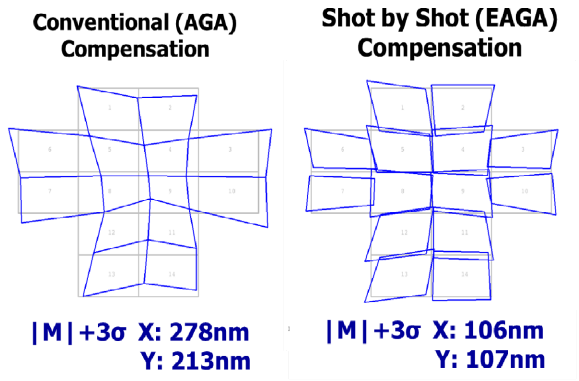


Figure 4: EAGA compensation of distorted 300 mm wafers meets overlay requirements for 1 µm TSV processes

EAGA improves stepper overlay on non-linearly distorted grids and if wafer-to-wafer grid distortion is equal, EAGA can be configured to measure each alignment target on the first wafer only to increase productivity. Wafers exhibiting very large random distortion may require wafer-by-wafer, shot-by-shot measurement and overlay compensation which will negatively affect throughput.

Canon has investigated the ability of the FPA-5510iV stepper to accurately apply pattern magnification at the maximum compensation values and distortion maps representing compensated exposure fields are provided in Figure 5. The experimental data shows that at the maximum magnification conditions, the FPA-5510iV provides accurate magnification compensation while maintaining acceptable levels of distortion. In general, "demagnified" patterns exhibited "pin-cushion" type distortion while extremely "magnified patterns exhibited minor "barrel" distortion effects.

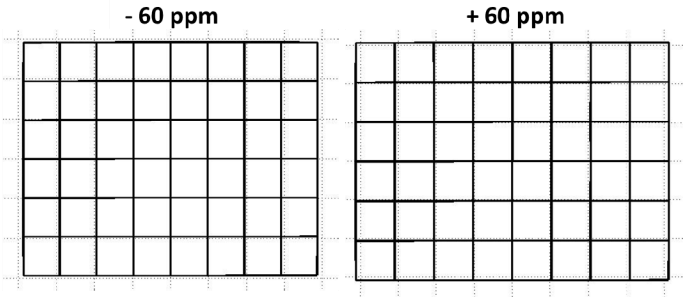


Figure 5: FPA-5510iV image distortion is small at maximum magnification

Wafer flatness must also be controlled to insure reliable wafer handling and accurate wafer focusing. Canon steppers can employ a variety of vacuum assist functions and chuck designs that serve to support safe handling of warped wafers, and also remove warpage from the wafers during exposure. Figure 6 illustrates the wafer flatness

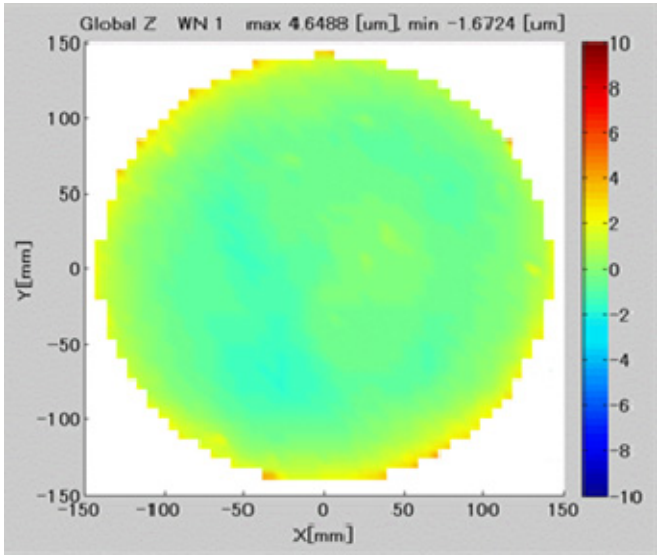


Figure 6: Canon Lithography Systems can reduce 730 µm of wafer warpage to 6 µm

after a bonded wafer stack possessing 730 µm of warpage was vacuum locked to a Canon stepper wafer chuck. Flatness measurements after chucking show only 6 µm of warpage across the wafer, illustrating the Canon stepper's ability to handle and process warped wafers.

450 mm wafers present an even greater challenge as wafer warpage and distortion due to process conditions are set to increase given the larger area of 450 mm wafers. Canon has performed fundamental 450 mm lithography equipment research and development activities and has produced what is reportedly the first ever, fully optically exposed 450 mm wafer as shown in Figure 7.

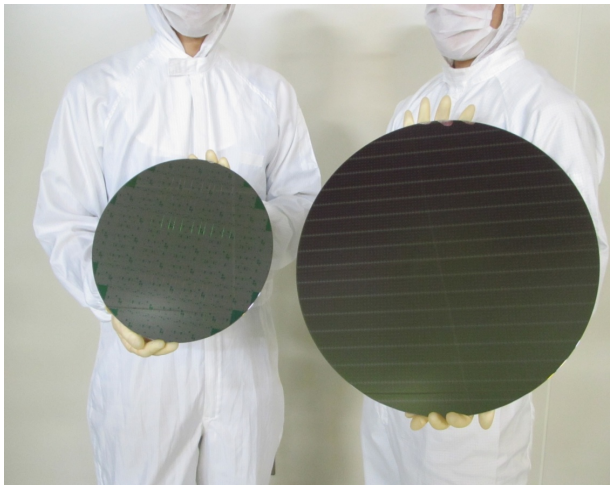


Figure 7: Canon is developing lithography equipment to support 450 mm requirements

Canon research into 450 mm distortion is based partially on knowledge gained from 300 mm experience where 285-300 nm of distortion is not uncommon. Based on Canon research, it can be expected that advanced wafers containing dense TSV arrays and RDL patterns may experience up to 1,600 nm of distortion across an entire 450mm wafer. Conventional AGA alignment with linear compensation will most likely not provide sufficient overlay accuracy for 450 mm wafers containing 1,600 nm of random error and EAGA may become a necessity for these wafers. A summary of simulate residual errors for AGA and EAGA compensation of distorted 450 mm wafers is provided in Figure 8. The raw data clearly shows increased error at the wafer edge and non-linear compensation amounts throughout the wafer.

Conclusions

This paper discusses how Canon continues to address the challenges of wafer grid distortion and wafer warpage in bonded wafer stacks. Current TSV process distortion is manageable, but will become an issue as device geometries are reduced, interconnect densities increase and wafer sizes increase to 450 mm. Reducing grid distortion of bonded wafers will become a priority in the future, but currently process requirements call for the lithography stepper to compensate for process-induced distortion.

Canon has contributed to improving yields and productivity by offering various lithographic solutions that address technical challenges in the bonded wafer manufacturing process. Canon is committed to supporting high-density 3D and 2.5D process technology development by clarifying technical challenges in the manufacturing process and proposing lithographic solutions. Until the industry removes distortion from bonded wafers, TSV steppers will continue to require robust Through-Silicon Alignment systems and powerful compensation capabilities.

Future 3D and 2.5 evaluation plans include application of Shot Shape Correction to correct for asymmetrical shot error and Low Oxygen Exposure to reduce exposure dose.

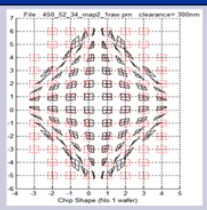
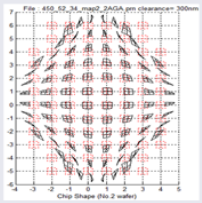
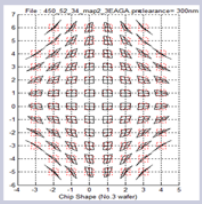
	Wafer Distortion Map	3σ [nm]
Raw Data		X = 1655 Y = 1647
AGA		X = 1215 Y = 1173
EAGA		X = 380 Y = 394

Figure 8: EAGA compensation provides superior overlay accuracy of distorted 450 mm wafers.

References

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[2] R, Sasaki, Y. Sumiyoshi, Y. Hasegawa, S. Miura, "Photolithographic solutions for image sensors with high pixel density", International Image Sensor Workshop 2013, June 2013