Thin-Wafer Handling with a Heat-Spreader Wafer for 2.5D/3D IC Integration

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Abstract
Thin-wafer handling is one of the key enabling technologies for 2.5D/3D IC integration. Usually, it temporary bonds the TSV (through-silicon via)/RDL (redistribution layer) wafer (e.g., passive and active interposers) to a supporting carrier wafer with an adhesive, backgrinds the TSV/RDL interposer wafer to very thin (≦100μm), goes through all the necessary processes, and then de-bonds the thin TSV/RDL interposer wafer from the carrier wafer. In this study, a different route will be taken which eliminates the temporary bonding and de-bonding processes. Emphasis is placed on using a heat-spreader wafer as a supporting carrier wafer during the manufacturing processes and after the assembly is completed (diced), the heat-spreader remains on the thin TSV/RDL interposer. This is a very simple and low-cost thin-wafer handling method for 2.5D/3D IC integration.

Key words
3D IC integration, through-silicon via, thin-wafer handling, heat-spreader wafer, thermal interface material.

I. Introduction
One of the key reasons why 3D IC integration is so attractive to semiconductor industry today is because it uses thin chips/interposers with TSVs (through-silicon vias) and RDLs (redistribution layers). For examples; 50μm or less for memory chips and 100 to 200μm or less for active and passive interposers.

Making the wafer thin is not a big problem because most back-grinding machine can grind wafers to as thin as 5μm. However, handling thin TSV/RDL wafers through all the semiconductor fabrication and packaging assembly processes is difficult. Usually [1-46], the TSV/RDL chip/interposer wafer is temporarily bonded with an adhesive on a support (carrier) wafer before back-grinding to expose the Cu TSVs (Cu revealing) and make the wafer thin. Then it goes through the fabrication processes, such as metallization, passivation, under bump metallurgy (UBM), and wafer bumping. After all these are done, removing the thin TSV/RDL wafer from the support wafer (debonding) poses another big challenges such as broken wafers and adhesive residues [1-46], which translate to higher yield lost.

In this study, a different route is taken which uses a heat-spreader wafer as the supporting carrier. When the manufacturing process is completed, the heat-spreader is remaining on the thin TSV/RDL interposer. In this case, the temporary bonding and debonding processes are eliminated and a simple and low-cost thin-wafer handling method is achieved.

The most likely 3D IC integration which will get into volume manufacturing is the 2.5D IC integration. It consists of a TSV/RDL passive interposer, which supports high-density, high-performance, and high pin-count chips without TSVs on its top side. Figure 1 (Xilinx/TSMC) [40, 41] and Figure 2 (Altera/TSMC) [42, 43] show some examples. TSMC called this chip on (interposer) wafer on (package) substrate (CoWoS). The chips are FPGA (field programmable gate array) with Cu-pillar solder microbumps at a 45μm pitch. The top-side of the TSV interposer has 4 RDLs (on a minimum 0.4μm pitch) to provide lateral communication of the chips. The thickness of the interposer is ~100μm and the TSV diameter is 10μm. In this study, this structure will be used to demonstrate the proposed simple and low-cost thin-wafer handling method with a heat-spreader wafer. (The necessity of a heat spreader for FPGAs will be shown in the appendix.) This structure will also be used to demonstrate TI and TSMC's thin-wafer handling method with a polymer or molding compound [44-46]. The conventional thin-wafer handling method will be presented first.

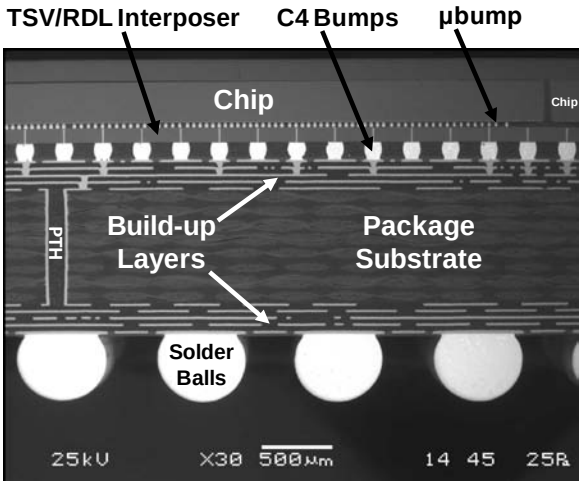

Fig. 1 Xilinx/TSMC's chip on wafer on substrate

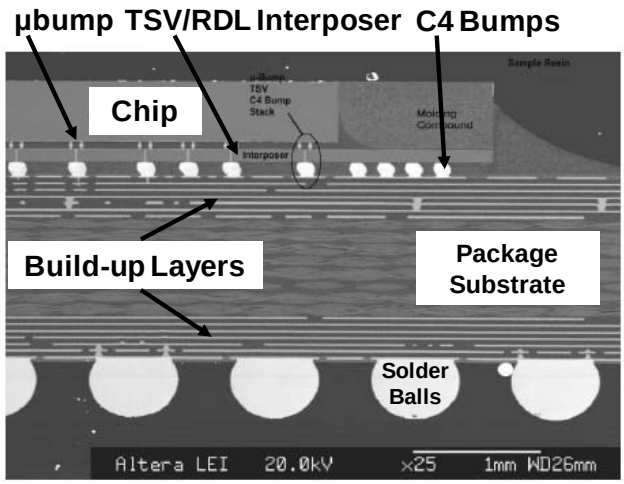

Fig. 2 Altera/TSMC's chip on wafer on substrate

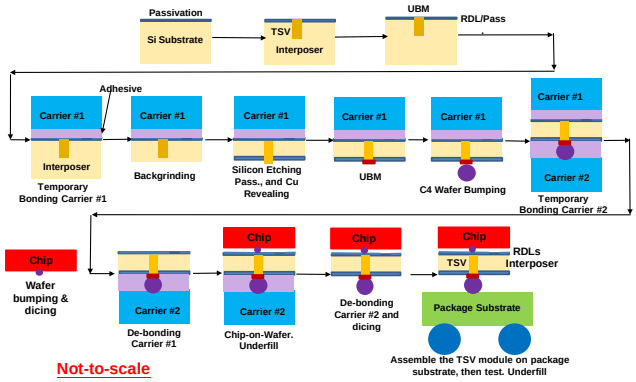

Fig. 3 2.5D/3D IC integration conventional process flow

II. Conventional Thin-Wafer Handling Method

Figure 3 shows a conventional thin-wafer handling method. After the fabrication of TSV, RDLs, passivation, and UBM, the TSV/RDL (active or passive) interposer wafer is temporary bonded to a supporting carrier by adhesive. Then, backgrind the TSV/RDL interposer wafer, Si etch, low temperature passivation, and Cu reveal. It is followed by backside RDL (optional), UBM, and ordinary C4 (controlled collapse chip connection) wafer bumping. Then, temporary bond another carrier wafer to the backside (with solder bumps) and de-bond the first carrier wafer. It is followed by chip-on-wafer bonding (attaching the micro bumped chip on the interposer wafer) and underfilling. After the whole interposer wafer is completed, then de-bond the second carrier wafer and transfer the thin TSV/RDL interposer wafer with attached chips to a dicing tape for singulation. The individual TSV/RDL interposer with chips is attached on the package substrate by natural reflow and then underfilled.

Today, the available adhesive materials are, e.g., (1) the LC-series and light-to-heat-convention (LTHC) layer provided by 3M, (2) HT-10.10 and ZoneBOND by Brewer Science, (3) TZNR-A series and WSP series by TOK, (4) XP-BCB by DOW, (5) WL-40XX and WL-30XX by Dow Corning, (6) HD-3007 and HD-7010 by Du Pont, and (7) TMAT by Thin Materials. The supporting carrier wafer materials are, e.g., (1) glass and (2) silicon. The temporary bonding and de-bonding equipments are, e.g., (1) TWM12000 for bonding and TWR12000 for debonding provided by TOK, (2) 850TB for temporary bonding and 850DB for debonding by EVG, (3) XBS300 for both temporary bonding and debonding provided by SUSS, and (4) WSS by 3M. The de-bonding methods are, e.g., (1) mechanical peel-off, (2) solvent release, (3) a combination of mechanical peel-off and solvent release, (4) thermal-sliding, and (5) laser irradiation.

III. TI's TSV-WCSP Integration Process

Figure 4 shows TI's [44] TSV-WCSP (wafer-level chip scale package) integration process flow. Up to Cu reveal and UBM, the processes are exactly the same as those (Figure 3) of the conventional process flow. Then, instead of wafer bumping, TI perform the chip-on-wafer bonding and underfilling. It is followed by overmolding the whole wafer

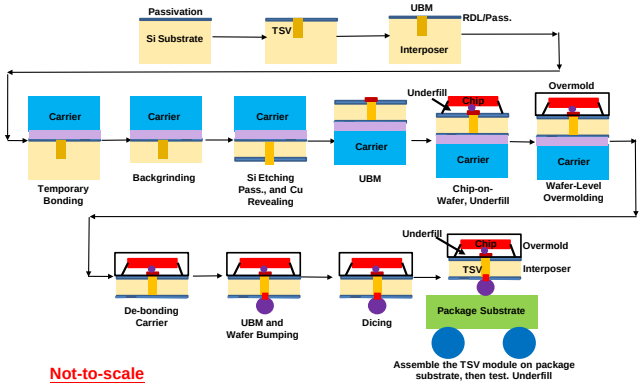

Fig. 4 TI's TSV-WCSP integration process flow

and de-bonding the carrier. Then, UBM, wafer bumping, and dicing. The individual TSV module is attached on the package substrate and underfilled. In this case, the second set of temporary bonding and de-bonding as shown in Figure 3 is eliminated.

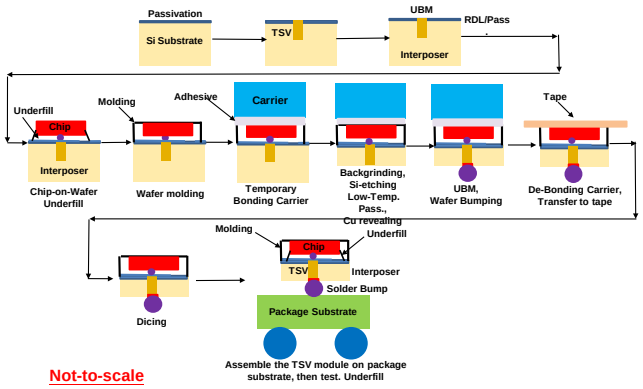

Fig. 5 TSMC's chip-on-wafer integration process flow

IV. TSMC's Thin-Wafer Handling with Polymer

In contradict to TI, TSMC perform the chip-on-wafer bonding [45] right after the fabrication of TSVs, top RDLs, and UBM as shown in Figure 5. It is followed by underfilling, overmolding the whole wafer, removing the portions of molding over chips, temporary bonding a carrier, backgrinding, low-temperature passivation, Cu revealing, UBM, and wafer bumping. Then, de-bond the carrier and transfer the TSV module to a dicing tape for singulation. The individual TSV module is attached on the package substrate and underfilled. Again, the second set of temporary bonding and de-bonding as shown in Figure 3 is eliminated.

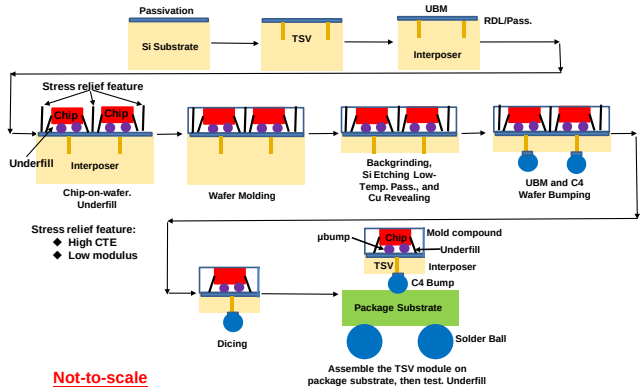

Fig. 6 TSMC's chip-on-wafer integration process flow (without temporary bonding and de-bonding)

V. TSMC's Thin-Wafer Handling without Temporary Bonding and De-Bonding

In contradict to the conventional thin-wafer handling method as shown in Figure 3, Figure 6 shows TSMC's thin-wafer handling method with molding chips on interposer wafer [46]. After the fabrication of TSV, RDLs, passivation, and

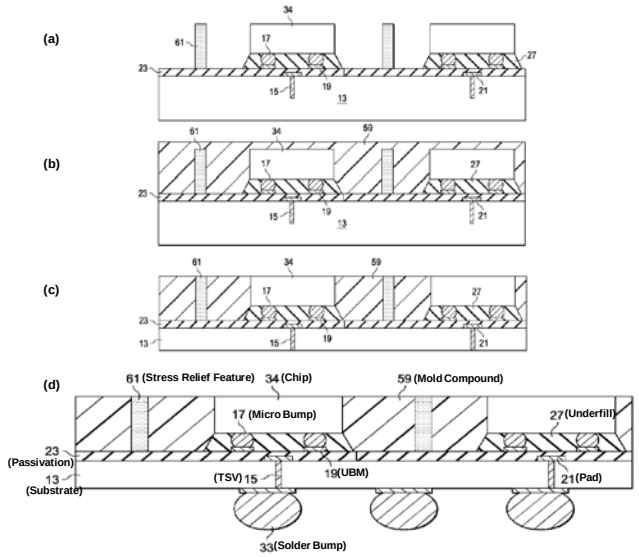

Fig. 7 TSMC's molding chips on interposer wafer (without temporary bonding and de-bonding)

UBM, the micro bumped chips are bonded on the TSV/RDL full-thickness (>700μm) interposer wafer and then underfilled. Then, over mold the chips on top of the interposer wafer with a molding compound and a stress relief feature to reduce the wafer warpage while backgrind to reveal the Cu TSV. It is followed by UBM, C4 wafer bumping, dicing, and attaching the individual TSV/RDL interposer with chips and molding compound on a package substrate by natural reflow and then underfilling.

Figure 7 shows more details on TSMC's method. In Figure 7(a), the micro bumped chips are bonded on the full-thickness TSV/RDL interposer wafer. Underfill is applied to cement the chips to the interposer to ensure the micro bump reliability. Stress relief "dams" (walls) are formed between the chips on the topside of the interposer. The material of the stress relief walls should have a high CTE (coefficient of thermal expansion) and a low modulus. In Figure 7(b), compression molding is performed and mold compound now covers the chips and the stress relief features. Then, the mold compound and the stress relief features may be cured. Figure 7(c) shows the top-grinding of the mold compound to expose the backside of the chips and back-grinding of the silicon substrate to expose (reveal) the Cu TSV. Figure 7(d) shows the C4 wafer bumping. In TSMC's manufacturing process, temporary bonding and de-bonding processes are eliminated. Instead, similar to embedded wafer-level ball grid array package (eWLP) [47] by using molding compound as a stiffer, in addition they also use the stress relief features to increase the stiffness of the molding compound to resist the warpage.

VI. Thin-Wafer Handling with a Heat-Spreader Wafer

Figure 8 shows the process flow of the proposed thin-wafer

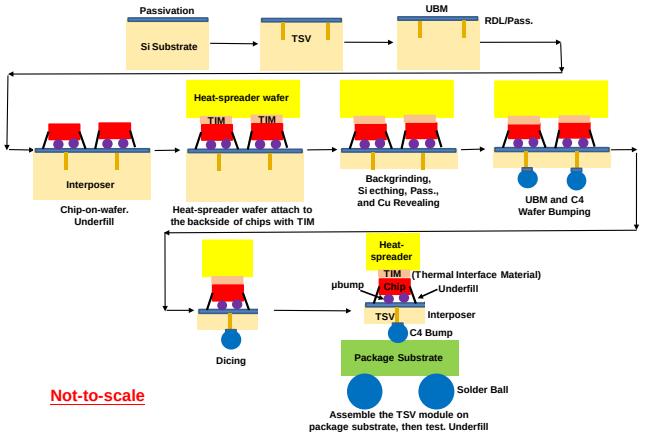

Fig. 8 Process flow of thin-wafer handling of 2.5D/3D integration with a heat-spreader wafer

handling with a low CTE and high thermal conductivity heat-spreader wafer. After the fabrication of TSV, RDLs, passivation, and UBM, the micro bumped chips are bonded on the TSV/RDL full-thickness (>700µm) interposer wafer and then underfill as shown in Figure 9(a). Then, attach the heat-spreader wafer to the backside of all the chips with a high-temperature stable TIM (thermal interface material), Figure 9(b). It is followed by backgrinding the TSV/RDL interposer and Cu revealing to expose the Cu TSV, Figure 9(c). Then, UBM and C4 wafer bumping as shown in Figure 9(d), and singulation. The individual thin TSV/RDL interposer with chips and heat-spreader is then attached to the package substrate by natural reflow and then underfilled.

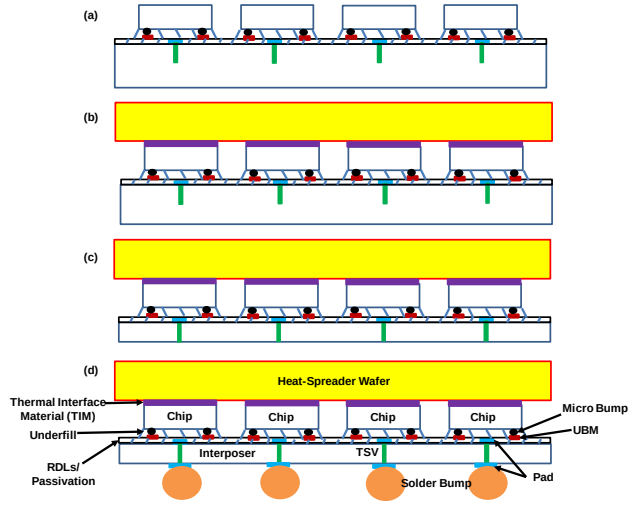

Fig. 9 Thin-wafer handling with a heat-spreader wafer

VII. Conclusions

Conventional thin-wafer handling such as adhesive materials, supporting carriers, temporary bonding and de-bonding equipments, and debonding methods has been discussed. TI and TSMC's think-wafer handling methods have also been presented and discussed. A new thin-wafer handling with a heat-spreader wafer is proposed and the process flow has been presented. Some important results are summarized in the following.

- With the proposal of bonding a heat-spreader wafer to the backside of chips on top of a TSV/RDL interposer wafer for thin-wafer handling, the conventional temporary bonding and de-bonding processes can be eliminated.
- With the new proposal, much less process steps are used (save cost) and much less chances to have yield-lost (save cost).
- One stone two birds! The heat-spreader wafer can be considered (used) as the supporting carrier during manufacturing and as the thermal management tool (heat-spreader) of the chips during operations.

Appendix

The objective of this appendix is to show (via simulation) that for wide I/O interface system with FPGAs a heat spreader is necessary. Figure 10 shows the systems for analysis: (a) with heat spreaders and (b) without heat spreader. There are two heat spreaders in Figure 10(a), the smaller heat spreader is attached to the backside of chips with TIM and has the same horizontal dimensions as the TSV interposer. The larger heat spreader is attached to the smaller heat spreader and stiffener with adhesive.

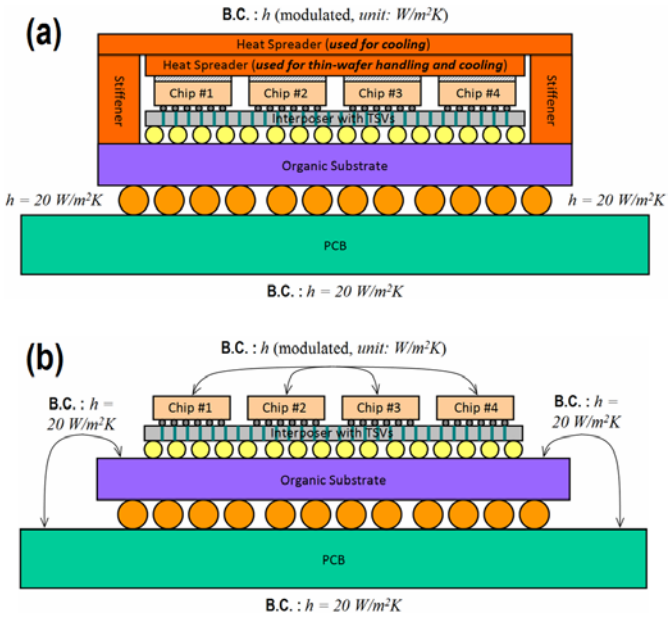

Fig. 10 Two FPGA systems. (a) With heat spreaders. (b) Without heat spreader.

Table 1 lists the boundary and power load conditions. There are four chips and the power consumption is 5W for each chip. The boundary conditions on all the surfaces of PCB (printed circuit board) and organic package substrate are h = 20W/m^{2}K (which means the substrate and PCB are cooled by a typical natural convection). As for the boundary

condition applied to the top surfaces of the larger heat spreader, Figure 10(a), and the chips, Figure 10(b), the convection coefficient, *h*, is tunable for parametric study. The modulated coefficient *h* is depending on the thermal resistance *Rca* that is changed from 0.2 to 4.0°C/W; the *h* can be calculated by the formula: $h = 1/R_{ca} \cdot A$; here, *A* denotes the heat spreader area (or chip area). Typically, the cooling ability of liquid cooling is for *Rca* < 0.3°C/W. For active heat sinks: 0.3 < *Rca* < 1.0, and for passive heat sinks: 1.0 < *Rca*.

Table 1 Power loading and boundary conditions

Power Load Condition	5W per chip (#1-4, total 20W)
Boundary Conditions	The thermal resistance (R_{ca}) of a heat sink: tunable for parameter study
	The convection coefficient h = 20 W/m^2.K on the both sides of PCB and organic substrate
	Other surfaces are regarded as adiabatic

Table 2 lists the dimensions of the systems for analyses. In performing the simulations, the detailed systems are replaced by equivalent models for simplification. The conversion from a detailed TSV system to an equivalent model has been described and demonstrated in [48-50]. Table 3 shows the materials properties and the calculated equivalent thermal properties of the TSV/solder bumps/solder ball structure.

Figure 11 shows the temperature distributions of the two analyzed systems with the applied boundary condition (*Rca* = 2.0 °C/W) on spreader and chips. It can be seen that the average chip temperature (~105 °C) of the system without heat spreader is much higher than that (~57 °C) of the system with heat spreader.

Table 2 Dimensions of the systems for analyses

	Length	Width	Height	Diameter	NOTE
Chip#1 - 4	12 mm	7 mm	500μm	---	The four chips are in the same sizes
Interposer	25 mm	31 mm	100μm	---	
Organic Substrate	35 mm	35 mm	800μm	---	
PCB	50 mm	50 mm	2000μm	---	
Heat Spreader (for thin-wafer handling and cooling)	25 mm	31 mm	700μm	---	
Heat Spreader (for cooling)	35 mm	35 mm	300μm	---	
TSV	Pitch = 250μm			10μm	
Micro-Bump	Pitch = 45μm			15μm	Between chip and interposer
Ordinary bump	Pitch = 180μm			150μm	Between interposer and organic substrate
Solder ball	Pitch = 1000μm			600μm	Between organic substrate and PCB

Table 3 Thermal conductivity of the systems

	k_{xy} (W/m.K)	k_z (W/m.K)	Thickness (um)	Notes
Grease	2	2	50	Between chips & heat spreader
Grease	2	2	50	Between the 2 heat spreaders
Interposer	147.27	141.46	--	Calculated equi. properties
Heat Spreader	401	401	200	
BT Substrate	40.9	0.38	800	
PCB	27.4	0.35	2000	
Micro-bump	0.63	4.36	15	Calculated equi. properties
Ordinary bump	0.63	27.3	150	Calculated equi. properties
Solder ball	0.05	14.14	600	Calculated equi. properties

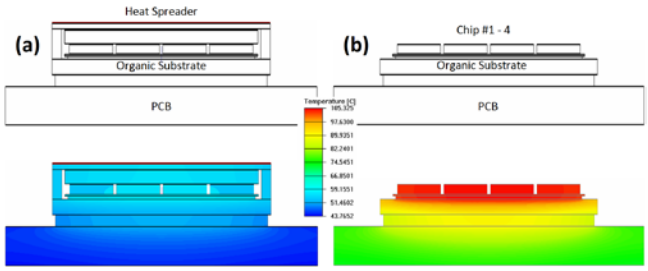

Fig. 11 Temperature distributions of the systems: (a) is for the one with heat spreaders and (b) is for the one without heat spreader

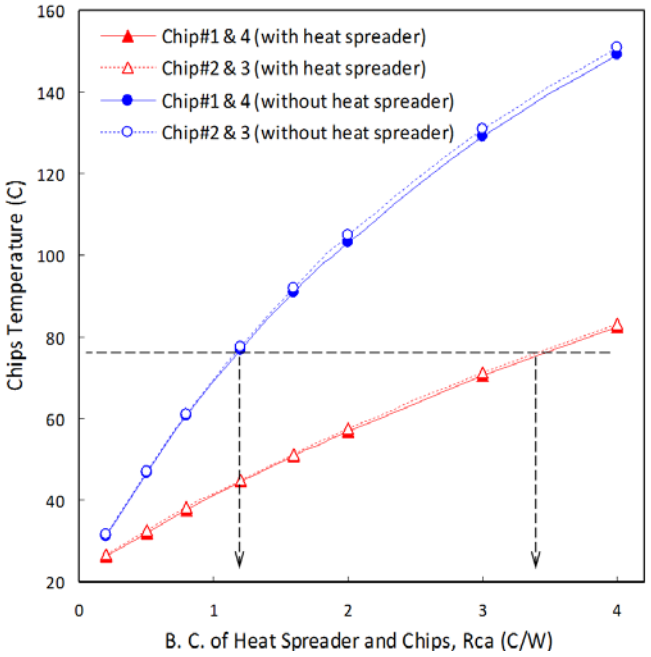

Fig. 12 Average chip temperature vs. thermal resistance of heat spreader

Figure 12 shows the correlation between chip temperatures and the applied *Rca*. Again, the average chip temperature of the system without the heat spreader is nearly 2.5 times

higher than that in the system with heat spreaders. Besides, from Figure 12, if the chip temperatures have to be cooled under 75°C (at ambient temperature of 20 °C), the system without heat spreader should use an active heat sink (usually with fan) that having a cooling ability of $Rca < 1.2$ °C/W. On the other hand, the system with heat spreaders should just use a passive heat sink (a small heat sink cooled by natural convection) that having a cooling ability of $Rca < 3.3$ °C/W.

Acknowledgements

The authors would like to acknowledge the financial support of MOEA, Taiwan. The strong support of the 3D IC Integration project by Dr. C. T. Liu, VP and Director of Electronics & Optoelectronics Research Laboratory is greatly appreciated.

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