

Characterizations of Fan-out Wafer-Level Packaging

Ming Li¹, Qingqian Li¹, John Lau¹, Nelson Fan¹, Eric Kuah¹, Wu Kai¹, Ken Cheung¹, Zhang Li², Kim Hwee Tan², Iris Xu², Dong Chen², Rozalia Beica³, CT Ko⁴, Henry Yang⁴, Sze Pei Lim⁵, Jiang Ran⁶, Cao Xi⁶,

⁶Huawei Technologies Co. Ltd.

⁵Indium Corporation

⁴Unimicron Technology Corporation

³Dow Chemical Company

²Jiangyin Changdian Advanced Packaging Co., Ltd.

¹ASM Pacific Technology

Ph: 852-2619-2804; Fax: 852-2619-2159

Email: mli@asmpt.com

Abstract

The calling for smaller form factor, higher I/O density, higher performance and lower cost has made fan-out wafer level packaging (FOWLP) technology the trend. Good control of die position accuracy and molded wafer warpage are some of the keys to achieve high-yield production for FOWLP. In this study, 10mm × 10mm test chips were fabricated and attached (chip-first and die face-up) onto 12 inch glass wafer carriers using die-attach-film (DAF). These reconfigured wafers were compression-molded with selected epoxy molding compounds (EMC). Cu bumps (contact-pads) were revealed by grinding, and redistribution layers (RDLs) were fabricated by lithography and electroplating process. The fan-out wafers were evaluated and characterized after each process step with main focus on the die-misplacement/die shift, re-configured wafer warpage, compression molding defects and RDL fabrication defects. The root causes of these defects were investigated and analyzed, while the possible solutions to overcome the defects were proposed and discussed.

Key words

Fan-out wafer level packaging (FOWLP), die-attach, compression molding, warpage control, RDL (re-distribution layer) process, defect characterization

I. Introduction

Die-shift/misalignment and warpage are the key points to achieve successful and high yield fan-out packaging devices [1, 2]. Die-attach pitch and position accuracy are important as the Cu bump (contact-pad) positions should match with the RDL masks, which are designed and cannot be modified. [3] Die-attach process should be carefully designed and controlled to meet the required tolerance. Warpage is another concern as it involves plenty of problems, including wafer handling difficulty and out-of-focus during RDL development. Warpage control has been widely investigated [4, 5], and it was reported that materials selection, fan-out ratio, package structure design and molding parameters are the key factors for controlling the warpage within an acceptable level. Molding process is another step that might involve defects and cause yield loss or reliability failure in the fan-out packaging manufacturing process [6]. Understanding the physics leading to the deformation behavior in wafer-level molding is crucial for minimizing warpage through process optimization.

II. Materials and experiments

The schematic illustration of the chip-first and die-up - fan-out sample structure in this study is shown in Figure 1.

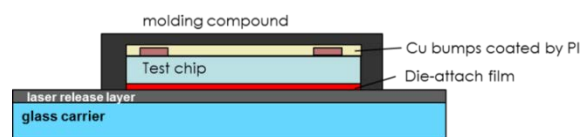


Fig. 1 Chip-first and die face-up sample structure

To achieve the designed structure, samples were fabricated by the following process steps:

A. Test vehicle structure design and fabrication

In this study, 10mmx10mm Si chip was designed as the test vehicle. The die thickness is 150μm. There are 1988 pads on one chip, with a minimum pitch of 150μm. The diameter of the Cu bumps (contact pads) is 60μm, and the height of the Cu bumps is 25 μm. The top-view of the test die is shown in Figure 2. Daisy-chains on the chip and RDL layout were designed as well for yield verification and reliability test.

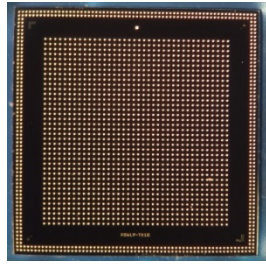


Fig. 2 Top-view of the 10mm×10mm test chip with Cu bumps,

B. Die-attach process

One reconstructed wafer contains 325 units of test chips populated on a 12 inch glass carrier. The package outline is 13.42mm×13.42mm with a fan-out ratio of 1.8.

Glass wafer carriers were used in the die-attach process. Carriers (die-attach side) were coated by 3M light-to-heat-conversion (LTHC) layer, as the molded fan-out wafer need to be released by laser from the glass carrier before package singulation. Test chip vehicle wafer was grinded to 150μm and DAF was laminated to the backside of the wafer. Carriers of 3 different coefficients thermal expansion (CTEs) values, including 3.25ppm/°C, 7.6ppm/°C and 8.1 ppm/°C, were used for the sample building. Die-attach process was carried out at 120°C (both bond-head and the bond-stage) with the bond force of 2.0 kg and the bond time of 2000ms, using ASM Nucleus multi-purpose precision die-bonder.

After die attach, post-cure was carried out at 125°C for 1 hour, die position data were then collected at room temperature (25°C). Bonding quality was checked by die-shear test and die-tilt measurement.

C. Molding process

Molding process was carried out using ASM ORCAS molding machine. The illustration of the mold chase set-up was shown as Figure 3. First, the glass carrier (die-attached) was fixed onto the top mold chase by vacuum. And then, molding compound was dispensed on the bottom plunger. Compression molding was then carried out with different molding speeds and packing forces. Molding temperature was 120°C and the mold clearance (from die-top to mold surface) was controlled at 100μm. KOZ (keep-out-zone) method was used and the mold cap diameter is Ø295mm (2.5mm clearance from the 12 inch glass carrier edge). The samples were then put into post-mold-cure process with 15kg deadweight, for a better warpage control. After cooling to room temperature, warpage level of the fan-out wafers were measured, and molding quality was then checked by optical microscope and C-SAM.

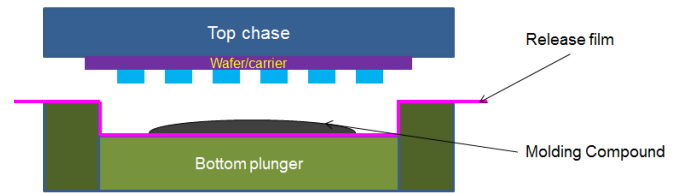


Fig. 3 Mold chase set-up illustration

D. Grinding and RDL process

Grinding and polishing process were carried out on Disco grinder. Cu bumps were revealed and the grinding quality was checked by optical microscope.

RDL layers were then built by stepper lithography and plating process. The alignment accuracy and quality of RDL layers were checked and verified, before moving to the next step.

III. Results and discussion

A. Carrier material selection

It was widely mentioned that CTE of the glass carrier affects the warpage of the molded fan-out wafer [7, 8]. Hence, simulation was carried out to estimate the best carrier CTE, molding compound CTE and the package thickness, as have already been included in our previous publication [5].

Model was established based on this packaging structure design, and the simulation result of CTE's effect on warpage level was shown in Figure 4. Based on the simulation result and glass carrier availability, three different glass carriers, with CTE of 3.25ppm/°C (for comparison), 7.6ppm/°C and 8.1ppm/°C (close to the optimized CTE by simulation result) were used for this evaluation.

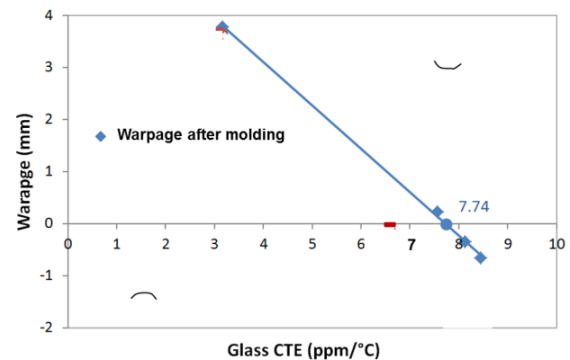


Fig. 4 Simulation of glass carrier CTE on molded wafer warpage (EMC volume shrinkage was assumed to be 0.27%)

B. Re-constructed wafer and die-attach process

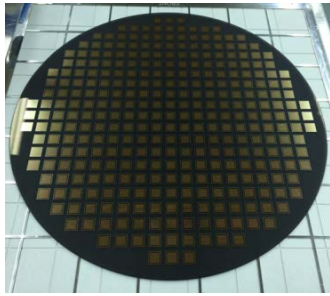


Fig. 5 Re-constructed wafer after die-attach process

The reconstructed wafer was shown in Figure 5. The X and Y pitch offset (the measured pitch subtracted from the designed pitch) was plotted against the column and row, separately, as shown in Figure 6(a). Without pitch compensation, large position offset ($\sim 100 \mu\text{m}$) was observed. Since die-attach was performed at 120°C , but the final pitch aligned for RDL process was carried out at room temperature. Therefore, pitch compensation (caused by heating during die-attach process) was needed which can be calculated by the following equation:

$$P_A = P_R + \alpha_L \Delta T$$

where P_A is die-attach pitch, P_R is the designed RDL pitch, α_L is the linear thermal expansion coefficient of the glass carrier, ΔT is the temperature difference between die-attach temperature and RDL temperature.

From the equation, it clearly showed that the accurate temperature control for both die bonding and RDL process are affecting significantly on the pitch compensation. Results in Figure 6(b) were obtained after compensation and process optimization, the placement offset was reduced from $\pm 100 \mu\text{m}$ (without pitch compensation) to $\pm 4.0 \mu\text{m}$ (with pitch compensation), and this is a good performance that can meet the process specifications.

Die-shear test was performed to assess the bonding strength, as the dice were subjected to a shear force during the compression molding process. Shear speed used was $300 \mu\text{m/s}$ and shear height was $40 \mu\text{m}$. For all the dice tested, the shear force was larger than 80kg , which could ensure the die-position stability during molding process as explained in the next molding session.

It is important to ensure the leveling of the Cu bumps on a same plane, as the molded wafers would be grinded to reveal the Cu bumps for RDL process. In this study, there are several factors that might contribute into the Cu bump leveling variation:

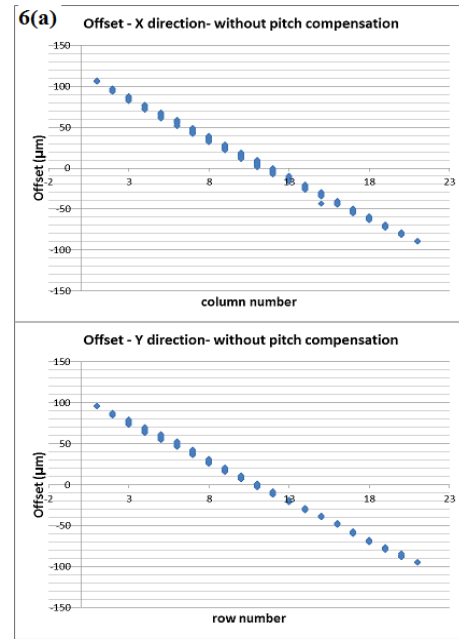


Fig. 6(a) Position offset data: X and Y direction (WITHOUT pitch compensation)

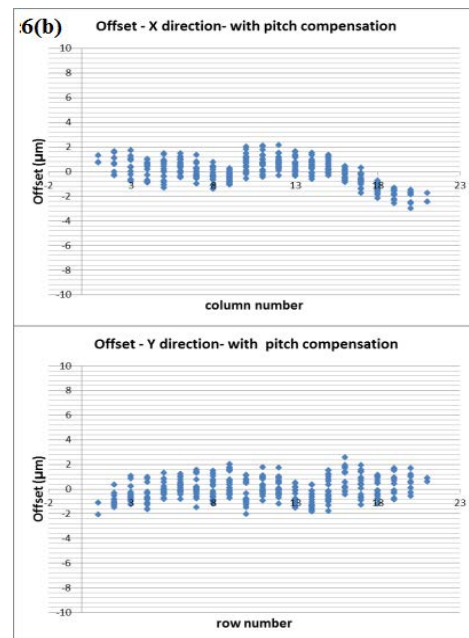


Fig. 6(b) Position offset data: X and Y direction (with pitch compensation)

- Total thickness variation (TTV) of the glass carrier. In this study, the glass TTV is less than $3.0 \mu\text{m}$ as provided by the vendor.
- Thickness variation of DAF material.

- c. Thickness variation of Si chips. In this study, the thickness variation of the test chips was measured and the variation range is $9.3\mu\text{m}$.
- d. Cu bump plating variation. In this study, the Cu bump height variation range is $5.3\mu\text{m}$ as measured.
- e. Die-tilt during die-attach process.

Die-tilt is one of the main causes of leveling variation of the Cu bumps. If there's die-tilt during die-attach process, the bumps could not be exposed at the same time during grinding process, even within one die. The die tilt defect was observed on the preliminary samples of this study, as shown in Figure 7(a). After process optimization, die tilt could be controlled much better to eliminate Cu bump exposure failure. The maximum leveling difference on the whole wafer could be controlled within $11.2\mu\text{m}$. The Cu revealing with optimized die tilt is shown in Figure 7(b). This leveling variation range is acceptable for this project, as it could be compensated by the Cu bump height, which is $25\mu\text{m}$.

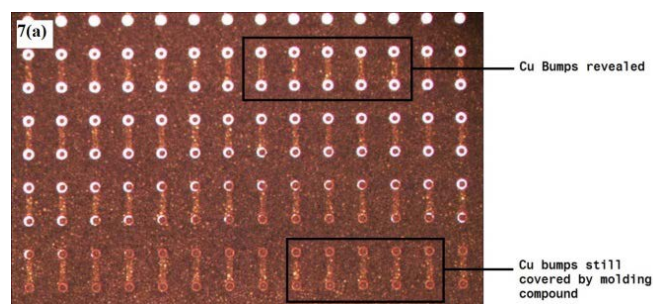


Fig. 7(a) Cu-bump revealing defect caused by die-tilt

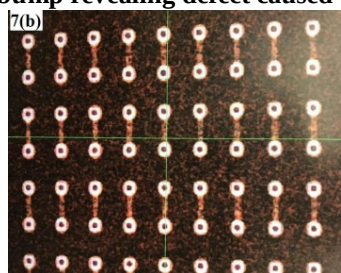


Fig. 7(b) Cu-bump revealing with optimized die tilt level

C. Molding Process and Characterization



Fig. 8 Molded fan-out wafer

The molded wafer sample is shown in figure 8. Molding quality was characterized in following areas: incomplete fill,

molding voids, warpage, and die shift after molding.

Incomplete fill is an important issue for fan-out wafer quality. Before optimization of the molding parameters (dispensing pattern, molding speed and packing force), coverage defects on top of the die were observed by optical microscope. Some of the incomplete fill points are at Cu bump positions and causing Cu bumps visible at top-view, as shown in Figure 9. The un-covered Cu bumps were easily damaged during grinding process and lead to yield loss.

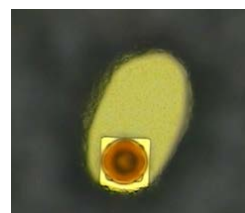


Fig. 9 Top view of the Cu bump exposed at the incomplete fill defect

Inspections for molding voids were carried out by C-mode scanning acoustic microscope (C-SAM). To balance the resolution and signal penetration depth, transducer of 75MHz was selected for the voids observation. Before molding parameter optimization, around 10 molding voids were detected in each of the molded wafers, especially located at the die-edge. The corners between wafer-carrier and die-edge could trap voids easily when liquid molding compound flows rapidly. Acoustic signals at suspicious void positions and normal positions were captured and compared, as shown in Figure 10. During process optimization, it was found that the incomplete fill and voids could be eliminated when the packing pressure was between 40 to 50 kg/cm^2 with a circle dispensing pattern.

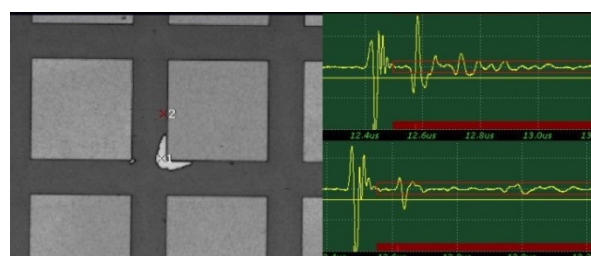


Fig. 10 Scanning acoustic microscope observation of the molding voids

Thicknesses of the molded wafers were checked and confirmed. After that, warpage of the molded wafers were measured using a Shadow Moiré system and contour was plotted. It has already been discussed in our former report that warpage after molding can be affected by glass carrier CTE and thickness, fan-out ratio, die thickness and molding thickness [5].

In this research, glass carriers with CTE = 3.25ppm/°C, 7.6 ppm/°C, and 8.1ppm/°C were used for sample building. After post-mold-cure with deadweight, the warpage of CTE 3.25ppm/°C carrier wafers were larger than 3mm and the warpage of CTE 7.6 ppm/°C and 8.1 ppm/°C glass carriers can be controlled within 0.4 mm. The data align with the simulation result [5]. Wafers with warpage under 0.5mm are acceptable for the following RDL processes requirements. Warpage data were collected by measuring the z leveling of the sample surface, and the contour of CTE 8.1 ppm/°C and CTE 3.25 ppm/°C glass carrier samples were plotted as Figures 11(a) and (b). Average warpage level of molded samples with different glass carriers were listed in Table I. The result proved that it is a must to optimize glass carrier CTE to control warpage level.

Table I Average warpage level of molded samples with different glass carriers (measured result)

Glass CTE	average warpage level
3.25ppm/°C	4.003mm
7.6 ppm/°C	0.380mm
8.1ppm/°C	0.250mm

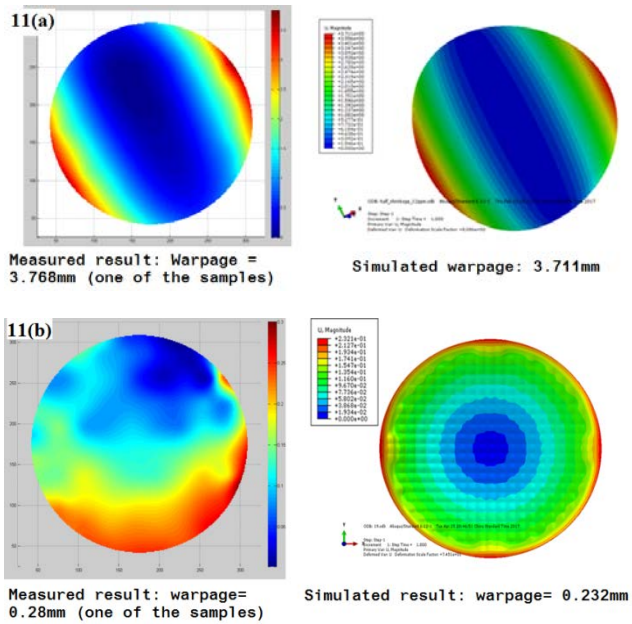


Fig. 11 Measured warpage and simulation contour of the molded wafers with (a) carrier CTE of 3.25ppm/°C, (b) carrier CTE of 8.1ppm/°C

For chip-first and die face-down, die-shift was reported by Robert L. Hsieh and his colleagues [1], that the location-change of the chips from the designed position causes alignment problem in the RDL exposure processes. In this study, (chip-first and die face-up with DAF), the

position of each die was recorded before and after molding. Then the die-shift caused by molding process was calculated by deducting the position coordinates before-and-after. Molding caused die-shift data were then statistically plotted in Figure 12. It was proved (together with the die-shear test result) that the adhesion between die and carrier is very strong. The position difference could be controlled within $\pm 4.0\mu\text{m}$. It is within the expected tolerance and acceptable for the RDL process, based on the designed Cu diameter size and sample structure in this study.

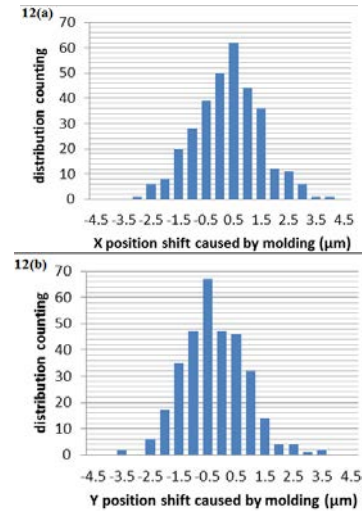


Fig. 12 Molding induced die-shift distribution data (a) X direction (b) Y direction

D. Grinding and RDL characterization

Grinding process quality was checked by optical microscope and Cu smear was observed before parameter optimization, as Figure 13(a) shows. It was found that Cu smear issue could be eliminated by optimizing grinding wheel and polishing process, together with soft etching. The optimized result is shown in figure 13(b).

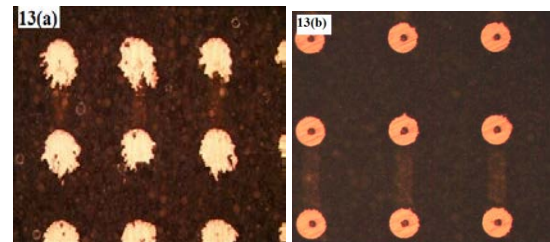


Fig. 13 (a) Cu smear during grinding process. (b) Optimized Cu exposure result

In RDL process, quality issues include exposure misalignment, development opening size error or residue, electroplating thickness control and over-etching/residue in etching process.

In this study, misalignment was checked by optical microscope, and it was found that the first RDL mask alignment accuracy was affected by the grinding quality. Cu smear might cause difficulty in the alignment mark matching, and lead to misalignment in exposure process. The misaligned exposure and accurately aligned RDL pattern were shown in Figures 14(a) and 14(b). Development process quality and etching quality were also evaluated by microscope. Cu RDL layer thickness was checked and confirmed by 3D profiler system, after each plating process.

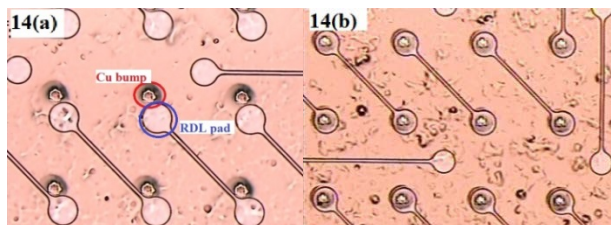


Fig. 14 RDL pattern with (a) misaligned exposure and (b) accurately aligned exposure

After RDLs fabrication and solder ball mounting, the fan-out wafers were released from the carriers by laser-debonding process. 355nm DPSS Nd: YAG UV laser source was used. The laser spot-size was 240 μ m, the scanning speed was 500mm/s and the scanning pitch was 100 μ m. The laser-debonded wafer is shown in Figure 15(a). The units on the fan-out wafer were diced into singulated packages, as shown in Figure 15(b), and tested for daisy-chain continuity.

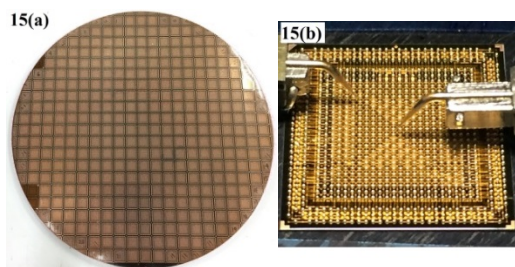


Fig. 15(a) laser-debonded fan-out wafer, and (b) singulated package and continuity testing

IV. Conclusions

In this study, fan-out wafer level packaging samples were fabricated and the process quality after each process step was characterized. Results are summarized in the following:

- Die-attach accuracy and pitch compensation are the key issues that need to be evaluated and controlled, for the position accuracy in RDL process. Factors including bond-stage temperature accuracy, RDL process temperature control and glass carrier CTE affect the compensation accuracy.
- Die tilt is an important factor that affects Cu bump (contact-pad) revealing (during grinding), and the

die-bonder should be carefully optimized to control the leveling.

- Die-attach strength was verified by die-shear test, as die position should be kept accurate during molding.
- The position data before and after molding was compared, and it was proved that molding induced die-shift could be controlled within an acceptable level.
- Apart from die shift during molding, there are two other concerns for the molding process: warpage level and voids. CTE of the glass carriers should be optimized based on simulation in order to minimize wafer warpage.
- For the designed fan-out ratio and package structure in this research, samples which were built with optimized carrier CTE showed very low warpage level and samples with large CTE mismatch warped severely.
- Molding compound selection is another factor that is important for the warpage control. Molding voids were characterized by optical microscope and scanning acoustic microscope. Defects can be eliminated by optimizing the molding process parameters.
- De-bonding of the glass carrier from the fan-out molded wafer has been successful performed by a YAG UV laser.

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