Using a Metal Oxide Adhesion Layer and Wet Chemical Cu Metallization for Fine Line Pattern Formation on Glass

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Abstract

With the trends towards miniaturization and heterogeneous integration, both IC and advanced substrate manufacturers are striving to meet the needs of next generation platforms, to increase the density of interconnects, and generate conductors featuring finer lines and spaces. Advanced manufacturing technologies such as Semi-Additive-Processing (SAP) and Advanced Modified-Semi-Additive-Processing (amSAP) were devised, realized and implemented in order to meet these requirements. Line and space (L/S) requirements of copper conductors will be below 5/5µm for advanced substrates, with 2/2µm L/S required for chip to chip connections in the near future. Herein we report about the performance of the new developed ferric sulfate based EcoFlash™ process for SAP and amSAP application with the focus on glass as the substrate and VitroCoat as thin metal oxide adhesion promotion layer.

The adhesion promotion layer (about 5-10 nm thickness) is dip-coated by a modified sol-gel process followed by sintering which creates chemical bonds to the glass. The sol-gel dip coating process offers good coating uniformity on both Though-Glass-Via (TGV) and glass surfaces under optimized coating conditions. Uniform coating can be achieved up to aspect ratios of 10:1 by using a 300µm thick glass with 30µm diameter TGV.

The thin adhesive layer enables electroless and electrolytic copper plating directly onto glass substrates. Excellent adhesion of electroless plated copper seed layer on glass can be achieved by using the adhesive layer and annealing technology. The thin adhesive layer is non-conductive and can be easily removed from the area between circuit traces together with the electroless copper seed layer by etching with a ferric sulfate based process. We have successfully integrated the adhesion layer and electroless and electrolytic copper plating technologies into semi-additive process and seed layer etching capable producing L/S below 10 µm.

Key words

Adhesion Layer, Differential Etching, Glass, Metal Oxide, Wet Chemical Metallization

I. Introduction

The attractions of glass as an interposer or substrate, include superior dimensional stability versus organic materials and CTE matching to the silicon chip that lowers the risk of warpage [1]. Glass has inherently superior electrical properties to silicon such as low dielectric constant and loss tangent which is beneficial to high frequency application. Electrical characterization and electrical models have demonstrated the advantages of the insulating properties of glass, and its positive impact on functional performance [2]. However, the smoothness of the glass surface, which enables fine line patterning, one of the major benefits of glass, creates difficulties for plating, which is the main topic of the present investigation.

Unlike an organic substrate it is challenging to metalize a glass surface because the smoothness of glass inhibits mechanical anchoring between metal and glass, typically seen in an organic substrate, to provide good adhesion [3]. Therefore it is desirable to have an effective adhesion promoter between metal and glass to provide good adhesion while not changing the mechanical and electrical properties of glass. Physical metal deposition techniques such as physical vapor deposition and sputtering deposition are

widely used for metalizing silicon wafers in semiconductor industry. This technique has also been applied on glass surface metallization by depositing tens of nanometers of titanium or chromium as an adhesion layer prior to bulk metal deposition [4].

A. Adhesion Promoter

For metalizing glass substrates with TGV's and blind glass vias with copper we have developed a metal oxide adhesion promotion layer which can be dip coated conformally on the inside wall of TGVs and glass surfaces using a modified sol-gel coating technique. The adhesion layer allows electroless copper plated directly on glass as a seed layer and then electrolytically plating thicker copper [5] - [7].

This wet metallization combined with annealing procedures can give excellent adhesion between electroless copper and glass. Adhesion layer coating, electroless copper plating, photolithographic patterning and electrolytic plating to form conducting circuits (so called semi-additive process, SAP) have been integrated seamlessly to the process of fabricating devices in wafer and panel scales. The major benefit of using a metal oxide adhesion promoter instead of a sputtered Ti or Cr layer is its easy etchability during Cu seed layer etching and pattern formation avoiding separate etching of the adhesion promoter layer.

B. Differential Etch

Commonly used differential etchants are based on sulfuric acid / hydrogen peroxide in combination with different organic additives. This etchant type is well known to form undercut of the conductor tracks (up to several micrometer), which clearly affects the mechanical stability and hence interfacial integrity especially for fine line conductors (track width < 10 µm).

As an alternative etching solution and complete new concept a ferric sulfate based process was introduced to the market by Atotech. The etching solution was based on oxidation of solid copper by Fe(III) as shown in equation (1). This type of etchant does not exhibit undercut as obtained for the peroxide based process of record (POR). [8]

$$Cu^0 + 2Fe^{3+} \rightarrow Cu^{2+} + 2Fe^{2+} \quad (1)$$

The combination of the metal oxide adhesion promoter on a smooth glass surface with a ferric sulfate based etchant - providing less undercut formation - is the key to fine line and space formation and future miniaturization.

II. Method and Process

A. Materials and Cleaning

Glass substrates were manufactured by Corning Incorporated. The glass substrates before adhesion promoter application were pre-cleaned via a wet chemical approach.

B. Adhesion promoter coating and SAP process flow

The core process steps are applying the adhesion promoter in step 2 followed by the SAP metallization processes and seed layer etching in step 7. Figure 1 shows the process flow chart.

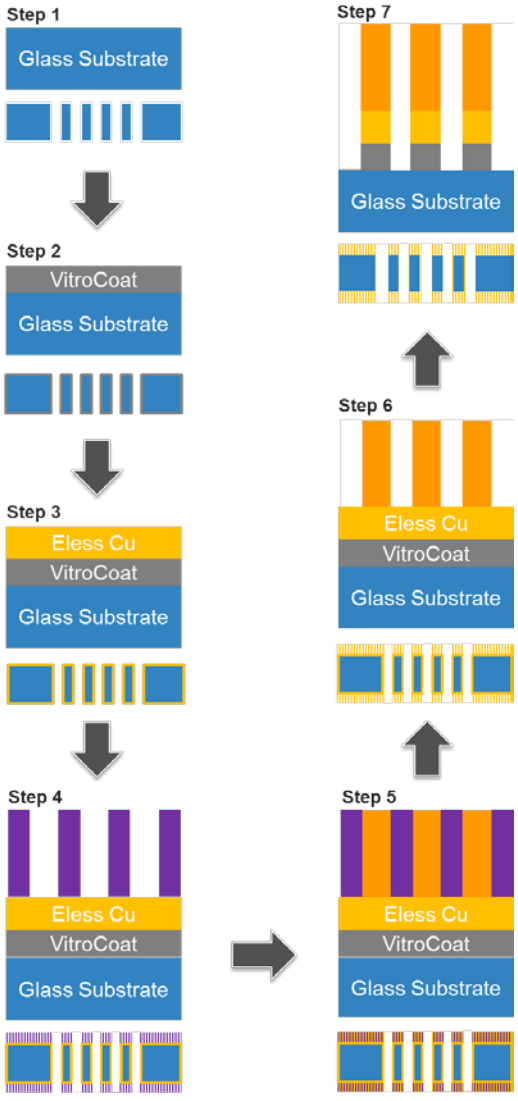

Figure 1. Cu metallization on glass surface and TGV by adhesion layer application and SAP

1) Glass Cleaning:
Glass substrates were pre-cleaned with EXPT VitroCoat GI PreClean-3 (Atotech), as shown in Step 1 (Figure 1). This is done to remove any organic and inorganic residue on the glass surface and prepare a clean surface for the following coating step to avoid any areas of de-wetting.

2) Adhesion Promotion Layer Formation:
The pre-cleaned substrates were dipped in EXPT VitroCoat GI S-1 (Atotech) solution containing the adhesion promoter precursor as shown in Step 2 (Figure 1). By pulling out the sample at a specific speed a uniform layer was formed on the glass surface after the solvent evaporated. A prebaking step was applied on the coated layer to remove additional solvent. To form the final adhesion layer a high temperature sintering step is necessary. The thickness of the adhesion layer is adjustable by changing precursor concentration, withdrawal speed and number of coating /pre-baking steps.

3) Electroless Copper Seed Layer Plating:
This process formed a thin copper seed layer on the adhesion layer as shown in Step 3 (Figure 1). The adhesion promoter coated glass substrates were activated by a palladium catalyst (Atotech: SigmaTech GI Activator MS) and finally plated in an electroless copper bath (Atotech: CupraTech GI M). The thickness of the electroless copper is controlled usually in the range of 400nm. Annealing of the electroless copper deposit was carried out to improve further the adhesion.

4) Photolithographic Patterning:
Dry film photoresist patterns were formed on the electroless copper seed layer as shown in Step 4 (Figure 1) by dry film lamination, light exposure, development and dry film residue cleaning. The dry film used for our test was Hitachi RY-5725EC (thickness 25µm).

5) Electrolytic Copper Pattern Plating:
Copper was plated electrolytically (Atotech: Cupracid InProSAP 2) to a thickness of 15-20 µm on the electroless copper seed layer as shown in Step 5.

6) Dry Film Stripping and Electrolytic Cu Annealing:
Stripping off dry film photoresist (Reiststrip IC-2™) and subsequent electrolytic copper annealing is conducted in Step 6.

7) Differential Etch and Circuit Formation:
Step 7 in Figure 1 is the last step of SAP process consisting differential etching of the electroless copper seed layer and adhesion layer in one step via the ferric sulfate based process (Atotech: Ecoflash™). Noted that here the adhesion layer can be removed with the same etching solution as electroless copper seed layer in one step.

C. Measurement tools and methods

The thickness uniformity of the adhesion layer and electroless Cu on flat substrate was investigated by X-ray fluorescence (XRF) mapping.
The interface of ultrathin layer was observed with energy filtering transmission electron microscope (EF-TEM) and scanning electron microscopy in combination with energy-dispersive X-ray spectroscopy (STEM XEDS).
The electrolytic Cu thickness distribution was measured by Profilometer after pattern plating.
The cross section samples were prepared by epoxy casting, grinding and polishing. The samples were investigated by optical microscope and scanning electron microscopy (SEM).

III. Results and Discussion

A. Coating quality of the adhesion layer

The dip-coating approach is an easily controllable and cost-effective method for glass substrates with and without TGV structures in high throughput and large panel scale.
Ultra-thin layers of less than 10nm can be achieved at specific withdrawal speed with reduced material consumption. The size of the samples which can be dip coated varies from small glass slides, 200mm diameter glass wafers and the full panels with the sizes up to 515mm x 515 mm. Panel size is equipment dependent only.
Glass panels (150 mm x 150 mm) coated with the adhesion layer has been mapped with XRF at 3.0 mm slit/15sec. The measured thickness value is 5.9±0.4nm on the front and 5.9±0.4 nm on the back. This shows a uniform distribution of the adhesion promoter during dip coating on both sides of the panel as can be seen in Figure 2.

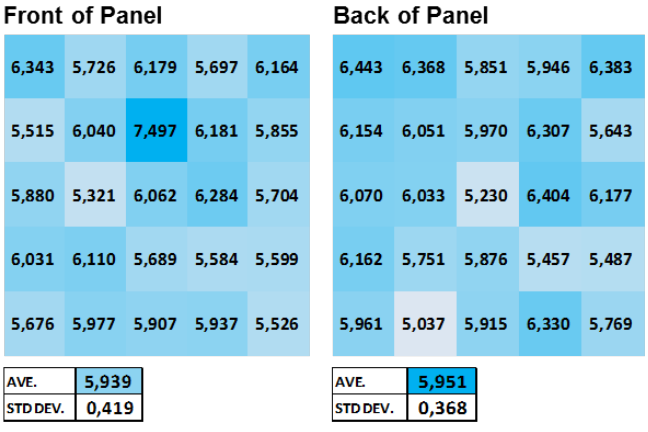

Figure 2. XRF mapping of the adhesion layer is shown on both sides of a 150 x 150 mm size glass panel.

The x-section of the adhesion layer was characterized by EF-TEM and It was shown that the adhesion layer is about 5-10 nm thick and uniform.

B. Electroless copper seed layer plating

It is important to have a uniform copper seed layer on the surface and inside of TGVs to get a high quality of conformally plated electrolytic copper in the SAP process. To check the uniformity of the Cu coating during initiation phase of the electroless Cu plating process a XRF mapping was conducted after 60 seconds of electroless plating. Figure 4 displayed the 150 x 150 mm glass panel after 60 seconds deposition with electroless copper and shows a uniform coverage of the whole panel with 30nm±2.4nm Cu.

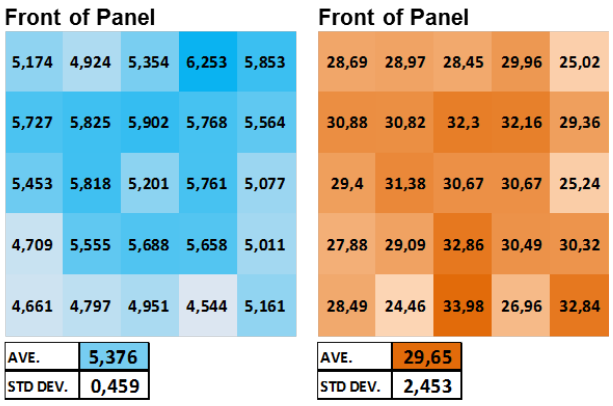

Figure 3. XRF mapping on front side of a 150 x 150 mm size glass panel showing the adhesion layer on the left side and electroless Cu (60 seconds plating time) on the right.

The total Cu thickness plated on the panels was in the range of 400 nm. There is no delamination or blistering on electroless copper seed layer before and after annealing. The seed layer passes the hatched tape test.

C. Photolithography

Finding reasonable process conditions for exposure and developing are important as exposure energy can influence final structuring performance. Low exposure energies lead to dry film adhesion loss or dry film integrity loss especially in fine line areas, respectively.

Evaluating X-section of the plated samples it turned out that fine lines (< 10 µm) are more influenced by the exposure energy than larger traces. The latter is almost independent from the applied exposure energy. The reason for this behavior might be the developing process. To get sufficient developer solution into the desired spaces is harder if the spaces become finer. Hence a significant impact of exposure energy and developer conditions was found. To get a similar distance to target (see Figure 4) for all measured line sizes, controlled exposure energy is required. For wider traces the exposure conditions are not as significant. The same tendency was found for the corresponding track shape (see Figure 4). Fine lines showed straighter shapes using higher exposure energy where-as lower exposure led to a trapezoidal shape.

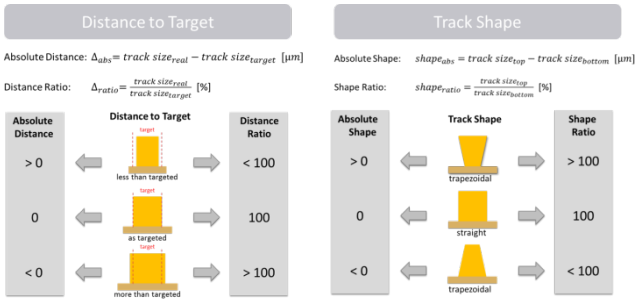

Figure 4. Distance to target and track shape definitions.

Undercut or a negative foot on the dry film started to form for the highest energy tested but was still very small (see Figure 5). Controlled exposure energy is essential to achieve straight sidewalls.

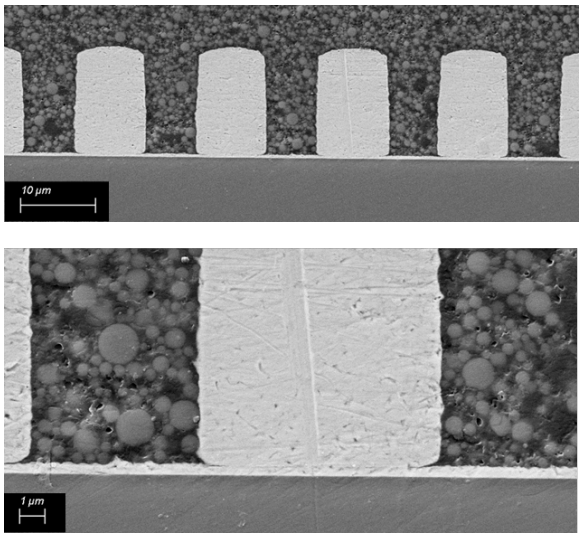

Figure 5. Line Shape at optimum exposure energy before seed layer removal. Top image: Overview of at optimum exposure energy after pattern plating and dry film removal. Bottom Image: close up of negative foot created in the dry film.

D. Electrolytic copper pattern plating

After depositing the electroless copper seed layer and photolithography an electrolytic copper pattern plating step

was carried out to deposit the thick copper layer for circuitry. The requirement for this step includes thickness uniformity across a panel and good adhesion of copper to glass substrate. Plating with lower current density leads to a better track height distribution but as a compromise between process time and performance the higher current density is favored (2 A/dm² calculating a Copper surface of 60%). For finer lines the track height decreased in general this is largely related to solution dynamics as copper plating requires a high flow of electrolyte in these areas and can be optimized accordingly, but highest decrease was found for the constant space of 50 µm. Difference between 1.5 A/dm² and 2.0 A/dm² in this test was the variation of plating distribution and as expected the track height. For Space=50 µm pattern at 1.5 A/dm² variation of 20 % was found (12-15 µm) whereas it increased for 2 A/dm² to 25 % (15-20 µm).

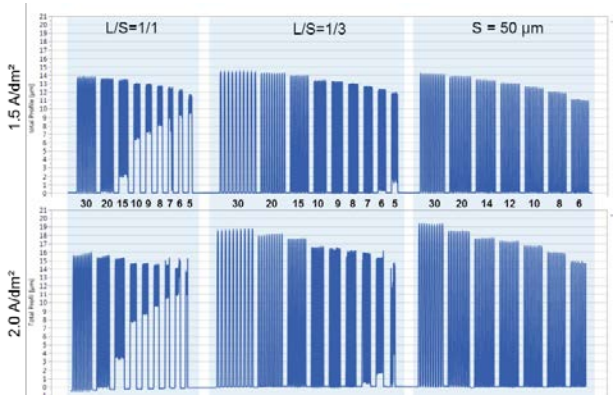

Figure 6. The image is showing electrolytic plating uniformity results for different L/S and applied current density.

As a summary of Photolithography and Electrolytic Plating optimum exposure energy is essential to achieve straight sidewalls. However, for fine line features (<10 µm L/S) the used dry film thickness and electrolytic Cu thickness plays a key role for all following steps like resist removal and differential etching in fine line features. The used dry film thickness of 25 µm and 15 µm plated electrolytic Cu is thus at the limit for features below 8-9 µm L/S.

E. Dry film resist removal and differential etching of electroless seed layer

After pattern plating dry film resist patterns were removed by resist stripper and followed by an annealing step to release the internal stress of electrolytic copper. The ferric sulfate based process was used to remove the seed layer as shown in Figure 7.

Especially in the finest L/S areas >10 µm the differential etch step has to be well controlled. To guarantee an electroless seed layer free differential etch result over the entire sample the differential etch solution was sprayed with 2 bar spray pressure. This enables a good fluid exchange in the smallest fine line areas.

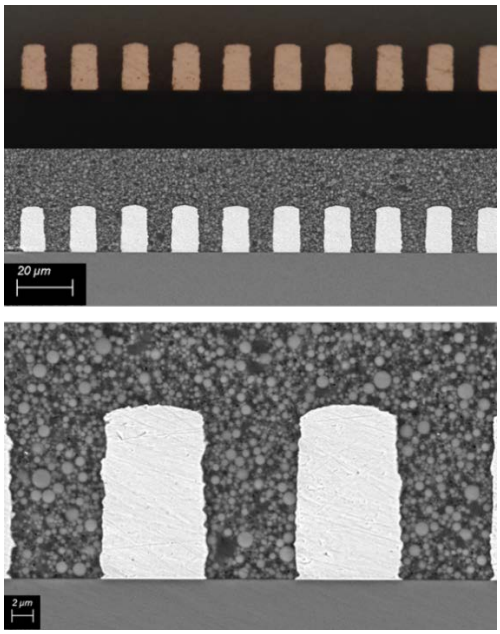

Figure 7. Fine Line area 9 µm l/s after seed layer differential etch. Top image: Showing a microscopy and SEM overview of 9 µm l/s area. Bottom Image: close up of 9 µm l/s tracks

Furthermore, a 20% longer treatment time was conducted, than would be necessary for the electroless copper on a planar surface. The prolonged etching time has no negative impact on the line shape or undercut formation.

F. Downstream for inner layer bonding

Advanced surface preparation for improved inner layer bonding is the next step after differential etching. The features plated on glass were treated with various processes for inner layer bonding as shown in Figure 8.

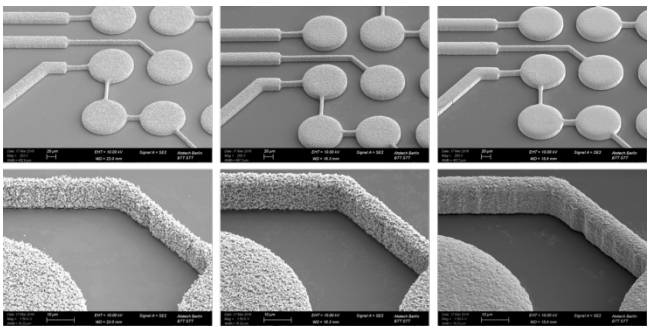

Figure 8. Left: copper-chloride µ-roughening; Middle: Cu-oxide adhesion promoter; Right: nano-roughening.

We tested a micro roughening copper chloride etch process (CupraEtch SR), an oxide adhesion promoter process

(BondFilm) and a nano-roughening approach developed for fine line features (Novabond IT). The detail image shows the different surface roughness after treatment. All process steps were compatible with the adhesion promoter and plated Cu tracks.

III. Conclusion

The adhesion layer coated on glass allows electroless copper seed layer plating on glass with good adhesion to fulfill the whole SAP process for fine line fabrication. The adhesion promotion process is a robust, high throughput and cost effective method of electroless plating of copper on smooth glass surfaces and TGVs. The process has been successfully applied on copper metallization on TGVs in both wafer and panel scales.

In order to fulfill the criteria for advanced substrates manufacturers require new processes to meet the finer L/S requirements in the immediate future. SAP and amSAP process flows require a differential etching step to remove the copper seed layer. The current process of record employs hydrogen peroxide as an oxidizer. One major drawback of this etchant is undercut formation and hence the maintaining of the interfacial integrity especially for fine line application.

Herein we also reported about a newly developed ferric sulfate based differential etching system named EcoFlash™. The additive packages lead to agitation independent etch attack and ensure minimal line width reduction. In contrast to peroxide etchants no undercut occur even with prolonged etching. This enables fine capability and optimized etching results even for small conductors.

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