Plasma Dicing Process-Flows for Advanced Packaging Fabrications

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Abstract

Comprehensive investigations were conducted on identifying integration efforts needed to adapt plasma dicing technology in BEOL pre-production environments. First, the authors identified a few suitable process flows. Within the plasma dicing process flows, laser grooving before plasma etching was shown to be a key unit process to control the resulting die sidewall quality. Significant improvement on laser grooving quality has been demonstrated. Through these efforts, extremely narrow kerfs and near ideal dies strengths were achieved on Si dies. The Bosch-etching based plasma dicing process generates fluorinated polymer residues both on the Si die sidewalls as well as under the topography overhangs on wafer surfaces, such as under the solder balls or micro-bumps. The fluorinated polymers in certain areas cannot be cleaned by an in-chamber post-treatments. Multiple wet chemistry-based cleaning methods demonstrated excellent process capability, and are compatible with plasma singulated dies-on-tape handling. Lastly, many methods exist for backside metal and under Si die-attach-film (DAF) separations. The authors highlighted recent processing results suitable for post-plasma dicing die separations of such film materials.

Key words

Bosch etching, dicing streets shrinkage, die singulation, fluorinated polymer removal, fluorine polymer clean, laser grooving, plasma dicing, wafer-level CSP

I. Introduction and Review

In recent few years, die singulation of silicon (Si) wafers by anisotropic plasma etching, i.e., plasma dicing, has gained significant attention of the semiconductor industry for the development of next generation advanced packages. This promising processing technology offers several potential benefits in terms of cost of ownership (CoO) and device performances over existing methods, namely, mechanical blade- and laser-based dicing processes.

Benefit 1. Allowing for Reduction of Kerf Widths by Design Leading to Increased Die Counts per Wafer

Similar to deep Si etching for MEMS or TSV formation, plasma dicing uses Bosch deep reactive ion etching to achieve high-aspect ratio etching of Si [1]. When such etching is limited to only the spaces between dies on a wafer – dicing streets, plasma dicing is achieved. Later, Section IV describes this technique in more detail. Since this technique by essence is a masked anisotropic etching process with minimal lateral etching, the die separation created by such techniques can be as arbitrarily narrow on a Si wafer as one designs. By decreasing the wafer real estate consumed as dicing streets, more device dies can fit onto the wafer surface under a new mask design. Using a generic die lay-out calculator, one can calculate the maximum number of dies that can fit onto a wafer surface by assuming the dimensions of die edges and dicing streets. Figure 1 illustrates the results from such calculation example using various die dimensions and a fixed 3mm edge exclusion region for the wafer. Here, the authors omitted considerations for test structures or fiducial dies. The normalized percentage trends are nearly identical for such die layout exercises based on 200mm and 300mm Si wafers. The plot contrasts the die counts for 80µm dicing streets, which is approximately the current production standard for CMOS logic and memory devices, to those of

40µm dicing streets, which is achievable using current advanced laser and blade-based dicing techniques, as well as to those of 20µm dicing streets, which can be achieved using plasma dicing. In Figure 1, for all die sizes, the die counts per wafer are normalized to that of 80µm dicing streets, represented as 100%. As illustrated, for all die shapes, the die counts per wafer increases by shrinking the dicing streets, i.e., more dies can fit on the wafer surface. This implies obtaining more product dies per wafer using nearly identical wafer based thin film processes at the front-end resulting in dramatic cost savings per end device. Figure 1 also shows that such die count gains are more pronounced for dies of smaller sizes because the area fractions of the dicing streets on smaller dies are more significant compared to those on larger dies.

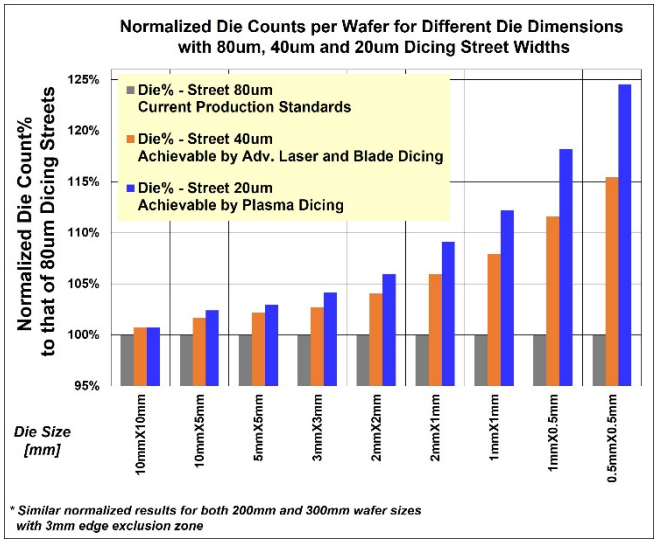


Figure 1. Die counts per wafer for 80µm, 40µm, and 20µm wide dicing street widths at various die dimensions. Die counts normalized to those of 80µm dicing street width.

Benefit 2. Improved Die Corner and Edge Qualities and Allowing Multi-Project Wafer Dicing

Since the die separation is created by gentle chemical consumption of the Si substrate, minimal thermal and mechanical damages are introduced onto the die edges and corners. This generally results in an enhancement of the die breakage strengths. The authors have summarized specific empirical comparison results in a later section of this manuscript. Designers can also introduce rounded die corners to further mitigate die impingement during pick-up and/or intrinsic thin film stresses built into the device die. See Figure 2 as an example [2].

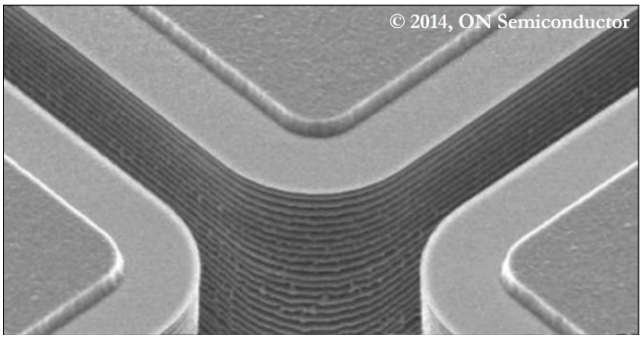


Figure 2. Examples of rounded die corners created by plasma dicing, previously shown in Ref.[2].

Following a similar logic, since Si etching to achieve die separations can follow any non-linear, non-continuous traces, multi-project wafer die layouts, curve-linear die shapes can be formed without any un-wanted wafer loss by plasma dicing.

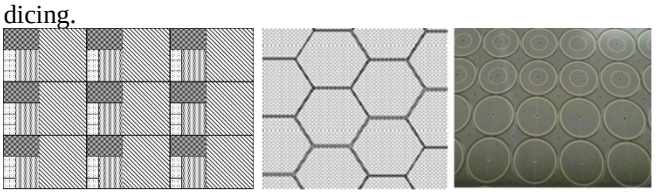


Figure 3. Examples of multi-project wafer, hexagonal die, and rounded die layouts [2].

Benefit 3. Improved Dicing Throughput

Dicing by mechanical blade or laser deliberately eliminates the real estate between dies following a single-point, serial process to singulate the devices on a wafer. While the later sections of this paper highlights the necessities of such techniques for other purposes in the overall process flow, by principle, wafer-based etching process would result in faster die separations. All the dies on each wafer is processed as a single batch. The authors have demonstrated etching rates in excess of 20-25µm/min on 300mm Si wafers on tape and frame. At such rates, for small device dies and thinned wafers, the throughput advantage of plasma dicing can easily manifest itself. Quantified advantages has previously been reported in Ref [2].

Combining the potential die count increases by changing from mechanical blade dicing to plasma dicing with the throughput increase and other process factors, the authors could devise a methodology for estimating the cumulative CoO per device die by using either blade dicing or plasma dicing methods. The specific quantitative assumptions of such calculations are not applicable for generalized introductions for all device types. However, the general *qualitative* trends for cost-effective applications of plasma dicing can be captured by Figure 4. When applying plasma dicing without benefiting the potential to re-design the dicing streets, only the very thin wafer thicknesses and very small

die sizes can gain advantage, as seen in Figure 4(a), only leveraging the after UPH of plasma dicing. However, if device designers could potentially take advantages of aggressive dicing streets shrinking to fit more dies per wafer, more die size-wafer thickness combinations would benefit in terms of overall CoO improvement, as seen in Figure 4(b).

Die Size	Smaller → Bigger									
Wafer Thickness	PD	PD	PD	PD	Blade	Blade	Blade	Blade	Blade	Blade
Thinner	PD	PD	PD	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	PD	PD	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	PD	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
Thicker	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade

(a) Both blade and plasma dicing equally wide kerf

Die Size	Smaller → Bigger									
Wafer Thickness	PD	PD	PD	PD	PD	PD	PD	PD	PD	Blade
Thinner	PD	PD	PD	PD	PD	PD	PD	PD	Blade	Blade
	PD	PD	PD	PD	PD	PD	PD	Blade	Blade	Blade
	PD	PD	PD	PD	PD	PD	Blade	Blade	Blade	Blade
	PD	PD	PD	PD	PD	PD	Blade	Blade	Blade	Blade
	PD	PD	PD	PD	PD	Blade	Blade	Blade	Blade	Blade
	PD	PD	PD	Blade	Blade	Blade	Blade	Blade	Blade	Blade
	PD	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade
Thicker	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade	Blade

(b) Design for plasma dicing having much narrower kerf

Figure 4. Qualitative, cumulative device die CoO trends comparing between conventional blade dicing techniques to plasma dicing. Other dicing techniques are not compared here.

The aforementioned potential advantages prompted the authors to continue the investigations on the challenges and improvements required in order to integrate plasma dicing unit process into current day fabless-foundries-OSAT packaging product supply chain as well as pre-production development to high volume manufacturing (HVM) environments, by utilizing primarily commercially available methods and consumables.

II. Plasma Dicing Process Flows for BEOL

Conventionally, the plasma etching process requires photolithography-based masking process. Figure 5 illustrates the process flow. In this fashion, an aligner or stepper mask is required to expose a layer of photoresist acting as a mask defining the dicing streets. Then, Si can be etched, followed by a last step of stripping off the photoresist layer.

Figure 5. Conventional photolithography based plasma etching process flow.

As reported in Reference [2], the authors have developed a plasma dicing process that is extremely '*gentle*' to the devices. So die designers can use passivation layers on the top surface of the devices themselves as the wafer's own plasma dicing mask. This is accomplished by changing the mask layout for the final bondpad openings to include dicing streets openings. Figure 6 illustrates this concept.

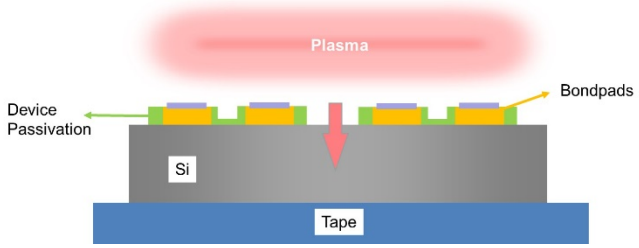


Figure 6. By changing the mask design of bondpads opening to include dicing streets opening, a gentle, dicing tape compatible plasma system can be used for plasma dicing without any photolithography using photoresist masking specifically for dicing streets.

However, currently, mainstream integrated circuit devices with multi-layer on-chip interconnects cannot yet adopt such treatments. Two main challenges exists for both approaches outlined above. (i) The device wafers generally require passivation layers, test element groups, and/or other metallic structures in the dicing streets. Such structures are generally used for wafer fabs' process witness tests, actual devices testing, or simply mechanical stabilization structures for the fragile thin films in the dicing streets. Regardless of the purposes, the metal structures cannot be etched by plasma. Meanwhile, it would take generations of device designs and millions of dollars of efforts to re-arrange these structures away from the dicing streets. Presently, there is a need to remove such structures *ad-hoc*, after their formations.
(ii) In current day product flow, dicing processes may be performed by overseas contracted sites rather than the original wafers manufacturing sites. At such die-fab / assembly locations, it is cost-prohibitive to maintain a photolithography process. There is a need to be able to open the dicing streets areas without using photolithography.

Laser grooving to expose the bulk Si in the dicing streets is the most suitable method. Such method can achieve extremely narrow widths (<10µm), helping realize the full potential of plasma dicing. Short-pulsed laser can ablate away the surface layers, removing metals and dielectrics. Then, plasma dicing can be applied. Figure 7 shows the concept of the process flow.

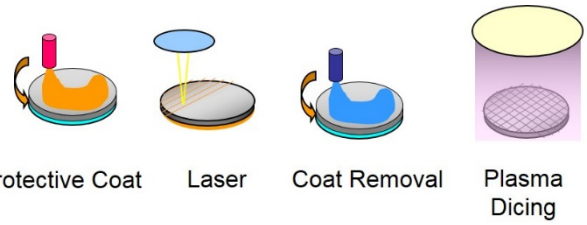


Figure 7. Using laser ablation to remove the un-etchable layers in the dicing streets before applying plasma dicing.

III. Laser Grooving Process for Plasma Dicing

A. Laser Pulse Width Effects on Grooving Quality

According to literature [3], current generations of short pulse-based laser grooving can still involve a significant large portion of thermal process that induces direct vaporization. During a laser pulse, the laser beam deposits irradiated thermal energy on a surface layer. When the pulse is sufficiently long in time, the surface can reach thermal equilibrium and heat conducts to the surrounding areas near the beam spot. A molten layer then forms while the laser continues to deliver more energy. This leads to materials' vaporization. Local high vapor pressure causes materials' melt to expel. The splattered material solidify as residues, or the heat affected zone (HAZ) surrounding the ablated regions [4]. Also, as a secondary effect, the highly molten material's excited electrons may further interact with the laser beam during irradiation pulse causing scattering and deflections. Consequently, the laser cut edges can be non-clean and jagged. Such conventional laser grooves are sufficient for *[laser + mechanical blade]* type of dicing processes. For such processes, a blade that is slightly narrower than the laser grooved width is used to dice through the dicing streets. The targeted device layers for such dicing processes generally consist of porous low-k dielectrics, onto which direct impact of mechanical blade dicing would lead to large chipping and delaminations. However, the slightly jagged edges from laser grooving would not impact the blade dicing performance. Therefore, such laser grooving processes are tolerated in HVM production.

On the other hand, such jagged edges may not be suitable for plasma dicing, because the die top edges serve as micro masks casting shadows over the etching sidewalls. Consequently, the etched die sidewalls generally would have a rough and wrinkled appearance following such jagged laser grooving tracks. The authors have made significant process improvement, while still utilizing conventional laser equipment, to the laser grooving shapes. See example result shown in Figure 8. By having such straight die top edges, the etched dicing streets also result in much smoother profiles.

Furthermore, if lasers with even shorter pulses are used while being able to maintain a similar average energy output, then each pulse's peak energy (fluence) dramatically increases. The rapid delivery of high pulse peak energy leads to much more crisp and direct transitions from solid to gas or plasma during pulsed laser ablation, while leaving less heat on the surface and less interferences with the laser beam spot. During an extremely short beam pulse, the surface cannot yet reach thermal equilibrium. The resulting cutting edge quality becomes much cleaner, and the widths of HAZ would also drastically reduce. Figure 8 compares examples of conventional, improved-conventional, and new (even shorter pulsed) laser equipment's grooving qualities as well as the resulting post-plasma dicing die sidewall qualities. One can see that a cleaner laser grooved track leads to a significantly cleaner die sidewall after plasma dicing.

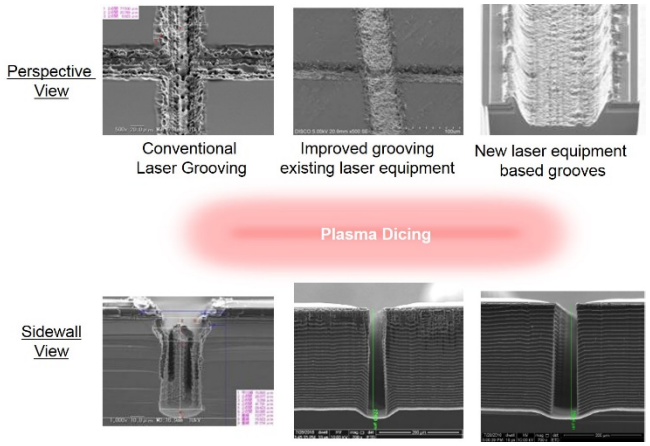


Figure 8. Laser grooving cleanliness and sidewall quality selections for plasma dicing.

One further empirical observation worth mentioning: Depending on a combination of the materials system of the wafer device layers stack and laser recipe variations, the existing laser equipment could produce either smooth or roughened Si sidewalls at narrow kerf widths. See Figure 9. However, for cases the sidewall quality still require further improvements, additional pre-etching treatment step can be added to recover the desired sidewall quality when using conventional laser grooving equipment. The flexibility to implement the additional treatment step enables manufacturing sites with existing conventional laser grooving equipment to achieve the ultimate narrow kerf shrinking of plasma dicing for nearly all devices. Such a process flow implies a HVM-ready, stable solution for plasma dicing with minimum modifications to the existing production equipment line-up at common overseas contracted sites.

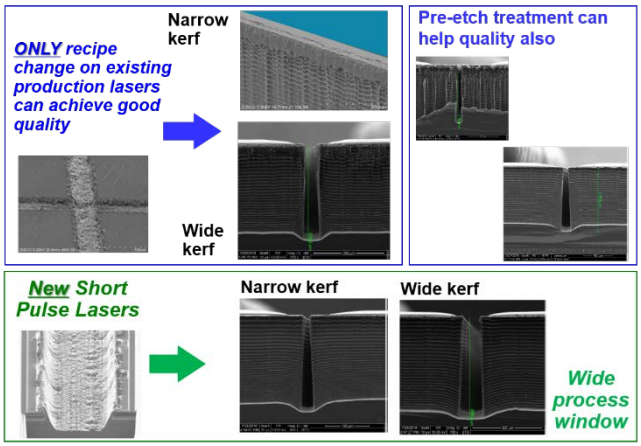


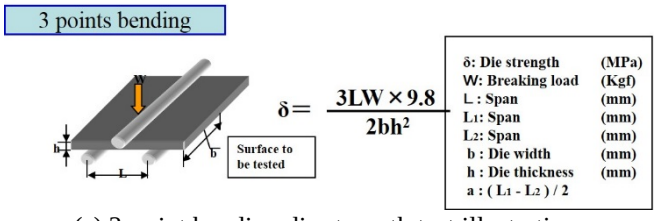
Figure 9. Laser grooving and plasma dicing at various kerf ranges.

B. Sidewall Quality and Die Strengths

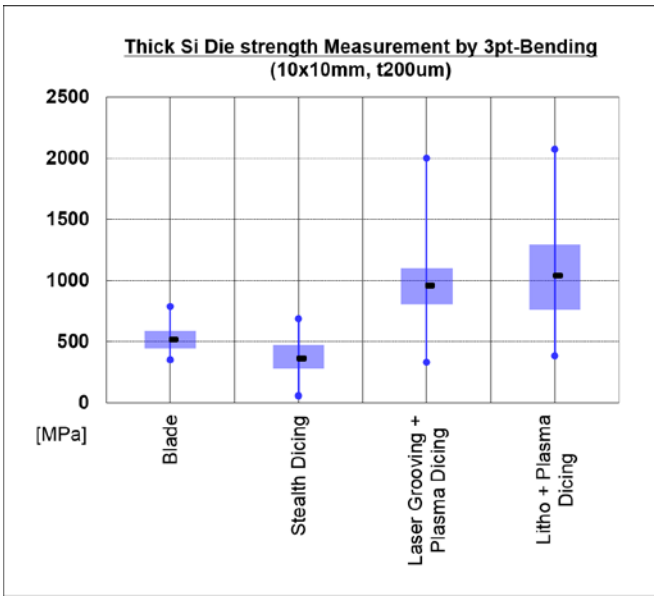
The Si die sidewall quality improvements are motivated by die strengths improvements. However, when making such correlations using bare Si dies, the results are only relevant for *thick* Si dies, such as, 100-200µm Si thickness range. For *thin* Si dies, a few 10's µm of Si thickness range, die strengths are independent of dicing methods. See measurement results shown in Figures 10 (b) and (c).

At relative thick die thicknesses, a higher fraction of the die breakage contributions come from 'sharp' defects on the die edges. The breaking strengths of plasma diced bare Si dies are the highest, having the least sharp corner defects leading to cracks. The photolithography defined, plasma diced dies have only slightly higher strengths than those made by laser grooving. This result attests to the proficiencies of the laser grooving top edge quality achieved. The other dicing methods produced lower die strengths in this case.

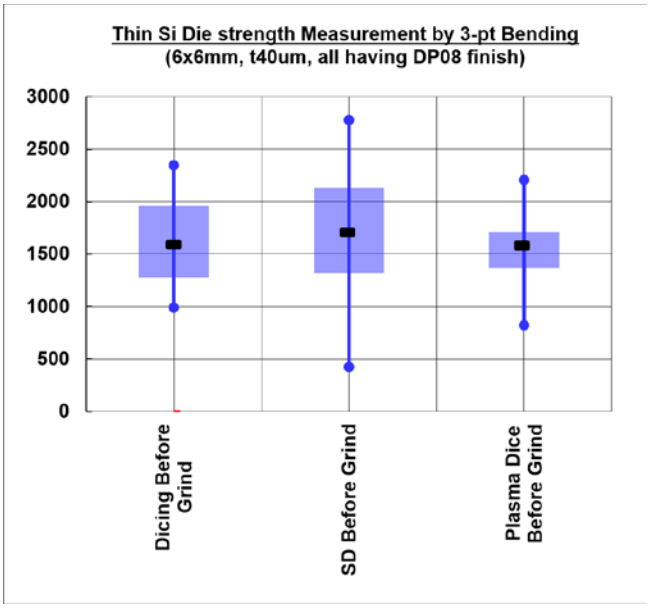
At very thin die thickness, however, the contributions of die breakages from defects on the sidewall become much less. Defects on the back surfaces as a result of die backside finish dominates. In actual devices, interfacial strengths may also determine critical die strengths. Broad generalization on thin bare Si dies strengths might not be comprehensive.



(a) 3-point bending die strength test illustration



(b) Box-plot of 3-point bending measurements of thick Si dies; 10mmX10mm, t-200µm



(c) Box-plot of 3-point bend measurements of thin Si dies; 6mmX6mm, t-40µm. All have same back finish, DP08.

Figure 10. 3-point bending die strengths resutls of various dicing methods.

IV. Fluorinated Polymer Removal

It is well known that Bosch deep Si etching generates fluorinated polymer residues on the sidewalls and surfaces of the wafer [1, 2, 5]. This is a direct result of the Bosch etching process loop. The Bosch anisotropic deep Si etching is achieved by the following steps:

(1) From the opening in the top passivation layer, highly chemically reactive, SF_6 plasma is introduced. This is an isotropic etching step that removes bulk Si via surface reactions turning solid Si into volatile compounds;
(2) In order to prevent excessive lateral undercut, Step (1) is then shortly interrupted. In Step (2), C_4F_8 gas based plasma is introduced to form a surface protective layer, a Carbon-Fluorinated polymer, which coats all of the freshly exposed Si;
(3) After the formation of the protected polymer coating, at the base of the etched pit, the Fluorinated polymer is removed by a stream of downward directional SF_6 plasma. So once again, only a small opening in passivation at the bottom is opened, while the polymer on the sidewalls acts as passivation against isotropic Si etching in subsequent steps;
(4) Steps (1) to (3) are repeated. As a result, the finished Si sidewalls have the so-called '*scalloped*' appearance. See Figure 11 for an overview of the Bosch Si etching process.

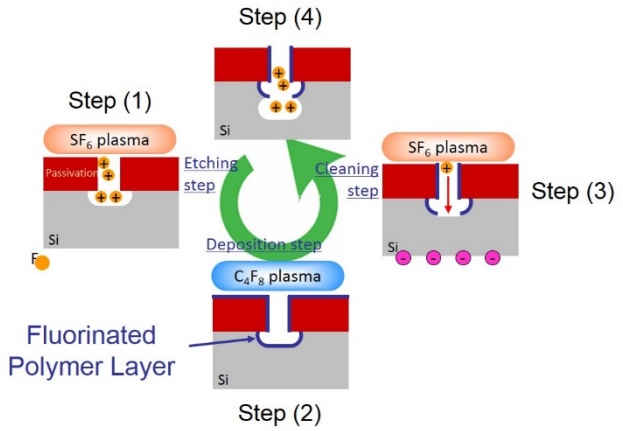
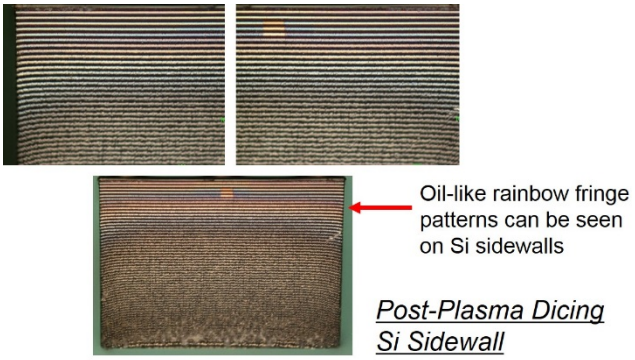


Figure 11. The Bosch deep Si etch process loop illustration.

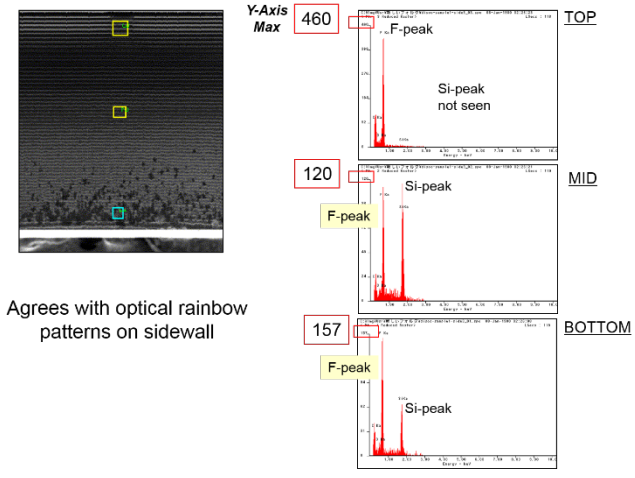
The fluorinated- (F-) polymer must remain on the die sidewall to prevent lateral etching. Also, during the Step (3) of each etching loop, the F-polymer can be bombarded and re-distributed onto other exposed surfaces. After plasma dicing, the die sidewalls usually appear to have F-containing residues. Figure 12 shows the Si sidewalls after plasma dicing, (a) the appearance under the microscope. Often times, an oil-like layer with rainbow fringes can be seen. (b) SEM/EDX elemental analyses show the Si sidewalls are heavily polluted by C and F elements. Taller F peaks seems to correlate with to more visually intense rainbow colorations under the microscope.

Furthermore, when the wafer contains surface topographies like solder balls or micro-bumps, the re-casted F-polymer can easily redeposit under the overhangs of such structures. See Figure 13 for example of solder ball appearance post-plasma dicing.

Such residues may be benign to certain types of electronic devices. Also, its adverse effects have not been widely reported by the industry. However, if untreated, for many packages, the oil-like layer would remain during epoxy over-molding processes, such as the formation of Fan-Out packages. Thus, presumable affect die to mold adhesions. In other cases, residues would remain during die attach and underfill processes jeopardizing the solder joint reliability. Fluoride ions are known to corrode certain metals [6]. Previous reports have shown additional cleaning steps within the plasma chamber can effectively treat F-polymer residues on flat top surfaces like Al bond pads, and that the wire pull strengths do not degrade [2]. However, in this case, the authors' attempt to clean the F-polymer under the overhangs of solder balls using within-plasma chamber methods have not been successful. As a result, alternative *ex-situ* F-polymer cleaning processes have been successfully developed.



(a) Optical microscope view of Si sidewall. An oil-like rainbow fringed residue layer can be seen on Si die sidewalls after plasma dicing. Bosch etched scallops can be seen.



(b) SEM/EDX analyses results of the Si sidewall after plasma dicing showing heavy contamination of Fluorine.
Figure 12. Si sidewall observations after plasma dicing.

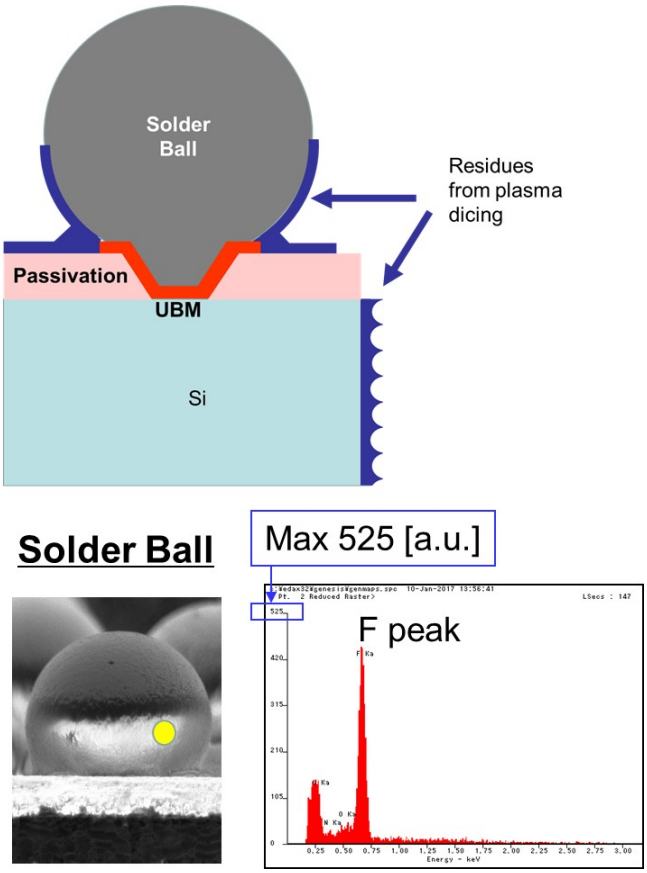
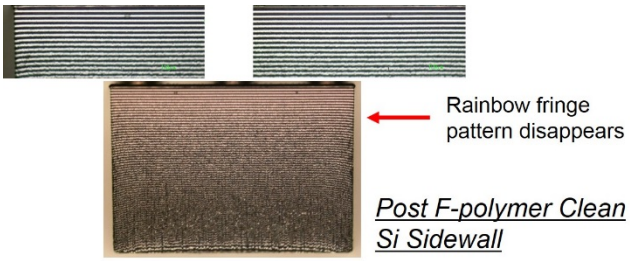


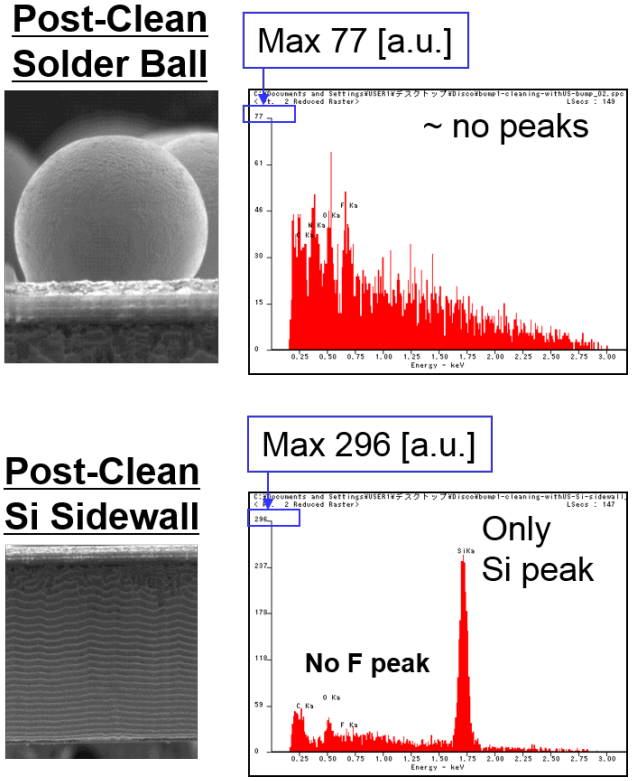
Figure 13. Post-plasma dicing F-polymer residues trapped under the solder balls.

The authors have found that more than one wet chemical methods can effectively cleaning the F-polymers. Figure 14 shows the post-clean results from one of such methods. The post-clean surfaces are compared with corresponding die locations un-exposed to any plasma, baseline controls. There is no difference seen in terms of EDX between the baseline samples and post-cleaned surfaces, therefore, achieving complete F-polymer removal. (Plots not reproduced here.) This type of wet cleaning agent is safe for all UV-type of dicing tapes.

In the evaluation of another wet cleaning method, compatibility to different dicing tapes is a pre-requisite. 1mmX1mm Si die arrays on various dicing tapes are exposed to this different cleaning method. Time to the first die lift off from tape is recorded. See Figure 15. 11 different dicing tapes showed a broad spectrum of first-die lift-off behaviors. All dicing tapes evaluated here are readily sold 'off-the-shelf.' Make, brand names, and model numbers are omitted by the authors. All 1mmX1mm dies remained on Tape-A approximately 10times as long as time on Tape-K. Tape-A is clearly more suited for this type of clean.



(a) Optical microscope view of Si sidewall. The rainbow colored fringed residues are removed.



(b) SEM/EDX results of solder ball and Si sidewalls showing no more F-polymers after cleaning process.

Figure 14. Post-clean Si sidewall and solder ball overhang characterizations. No polymer is observed.

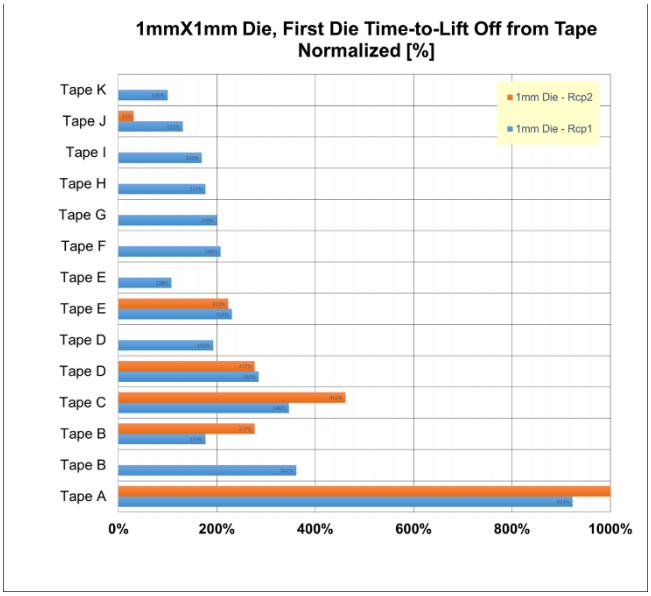


Figure 15. Separate cleaning method tape compatibility test. Normalized time for first 1mm die lift-off from tape under this particular cleaning process.

V. Back-Metal and DAF Separations

Wafer backside metallization, like the metal film stacks present in power devices, as well as certain types of die attach films (DAF), like those used for flash memory die stack packages, cannot be readily etched through by the Bosch plasma process. For such film stack layers, after plasma dicing, a separate die separation process is required. Several commercially available processes exist for metal film separations, such as, tape stretching, laser grooving, or other techniques. The authors have been surveying different separation techniques for post-plasma dicing process. Figure 16 shows an example of backside multi-metal layer film stack separation results by one of such commercially available methods. The authors have also successfully achieved DAF separation using multiple types of processes. The authors plan to give further detailed update during the iMAPS2017 conference presentation.

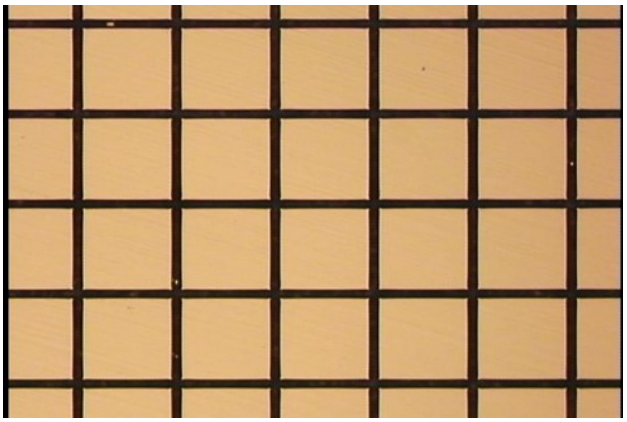


Figure 16. Clean backside metal separation. Additional process step needed after plasma dicing for dies with backside metal films. Several commercially available process options exist to date.

VI. Summary and Conclusions

The authors performed investigations on the ancillary processes and materials required in order to integrate plasma dicing technology into present day BEOL supply chain. Plasma dicing on 300mm dicing tape-and-frames can readily be introduced to pre-production. Previously presented method of modifying bondpad masking layer to open up the passivation in the dicing streets exposing Si for plasma dicing is still valid.

Furthermore, for BEOL, laser grooving has been identified as suitable process for removing passivation layers and metal structures when aforementioned re-arrangement is not possible. The authors have made significant optimizations on the laser grooving quality for plasma dicing. Both conventional as well as new types of laser equipment can be adopted for plasma dicing, achieving extremely narrow kerf widths and high die strengths after plasma dicing as a result. Post-plasma dicing, the authors observed copious amount of F-polymer residues on Si die sidewalls and below the overhang regions of top surface topographies like solder balls. Additional cleaning processes are evaluated. Commercially available wet cleaning processes for tape-and-frame singulated die handling can be introduced. Several commercially-available methods already exist for backside metal film stacks and DAF separation. Such processes can be added post-plasma dicing for all device types' separation needs.

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