Novel Interconnect Materials for Advanced Packaging Assembly Processes

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Abstract

As advanced packaging continues to drive towards heterogeneous integration, new materials need to be developed to address the many challenges faced in the assembly process. Development of novel materials for the various assembly processes is crucial to ensuring high yield for the assembly process for reliable SiP applications, and high density, fine pitch interconnects.

As ultra-fine pitch flip-chips become prevalent in advanced packaging, with reduced standoff of flip-chips and other IC packages, cleaning becomes ever more challenging, especially as the chip and package sizes increase. The shift towards using semiconductor grade ultra-low residue no-clean flip-chip fluxes, which eliminates the cleaning process, is therefore one of the solutions for overcoming these challenges. The flux residue left behind after the soldering process is minimal and is compatible with the underfill or molding materials used in the subsequent processes. Further, adhesive agents, which leave near zero residue, have also been developed to enable fluxless soldering for wafer/die bonding. Another challenge is the warpage induced open joints defects as the chips are becoming thinner and larger, and thermo-compression bonding (TCB), and laser-assisted bonding (LAB) are being explored as alternatives for the typical mass reflow process, to improve process yield with robust flux materials.

With more semiconductor chips and smaller components packed into a smaller footprint, the deposition of solder paste for high density SiP applications has become very challenging. For fine feature solder paste applications, the quality of fine solder alloy powder, flux formulations, and solder paste rheology, are crucial to achieve consistent solder paste deposition and good soldering performance. Particularly, for solder paste applications down to 100um or less, fine solder alloy powder, robust flux formulations, and solder paste rheology have been developed to achieve consistent solder paste deposition and good soldering performance. Due to some packaging design where printing of solder paste may not be possible, dispensing or jetting can also be used as an alternative.

This presentation will cover innovative materials for advanced packaging and heterogeneous integration, including novel ultra-low residue flux formulations for flip chip attach that is compatible with underfill and molding compound, adhesive agent for fluxless soldering, and solder paste for ultra-fine pitch printing. These novel materials are critical enablers for high density packaging applications. Use cases for high density SiP modules, TCB and LAB, for advanced packaging and 2.5D modules, will be discussed as well.

Key words

Advanced packaging, flip-chip, flux, interconnect, TCB, SIP, solder, warpage.

I. Introduction

Advanced packaging has emerged as a critical technology enabler for artificial intelligence (AI), high-performance computing (HPC), networking, and data center applications. As conventional transistor scaling approaches physical and economic limitations, heterogeneous integration has become an increasingly attractive method to improve system performance by integrating multiple dies within a single package.

Technologies such as 2.5D interposer-based integration, 3D stacking, chiplet architectures, and advanced SiP platforms enable unprecedented levels of functional integration and bandwidth. However, these architectures introduce significant assembly challenges due to increasing interconnect density, reduced bump pitch, thinner dies, larger package sizes, and increasingly complex package stack-ups.

For flip-chip assembly, the reduction in die-to-substrate standoff height creates severe cleaning challenges following solder reflow. Conventional flux residues can become trapped beneath large dies and fine-pitch interconnects, potentially causing underfill voiding, delamination, conductive residues, dendritic growth, and long-term reliability concerns. At the same time, larger and thinner dies increase package warpage during reflow, resulting in non-contact opens and yield loss [1].

The migration from traditional mass reflow processes toward thermo-compression bonding (TCB) and laser-assisted bonding (LAB) introduces additional material requirements. Fluxes must withstand prolonged thermal exposure while maintaining activity and avoiding residue hardening. Furthermore, the industry trend toward true no-clean and fluxless assembly processes demands increasing emphasis on novel material development.

In parallel, high-density SiP applications require solder paste printing at increasingly smaller dimensions. Apertures approaching 100μm and below demand finer solder powders, optimized rheology, and improved oxidation resistance to achieve consistent deposition and soldering performance.

Consequently, material innovation has become a key enabler for advanced packaging assembly. This paper reviews several emerging material solutions designed to address these challenges.

II. Challenges in Advanced Packaging Assembly

A. High density fine pitch Flip-chip assembly [2]

As bump pitch continues to shrink and die sizes increase, cleaning flux residue after reflow becomes increasingly difficult. Traditional no-clean and water-soluble fluxes can leave significant residue beneath the die, where cleaning can be less efficient due to the tight standoff height.

Residual flux may adversely impact underfill adhesion and flow characteristics, potentially leading to void formation, delamination, and reliability degradation. Furthermore, ionic residues may contribute to corrosion and electrochemical migration in highly miniaturized interconnect structures, examples shown in Figure 1.

The challenge becomes even more significant in advanced 2.5D and 3D architectures where multiple assembly levels are stacked within a single package.

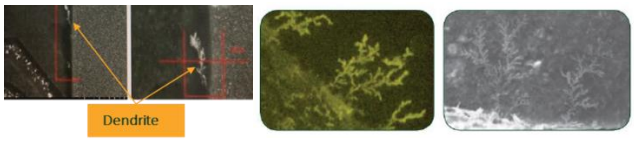


Figure 1. Examples of dendrites formation due to electrochemical migration.

B. Warpage-Induced Open Joints [3]

Advanced packages frequently incorporate large silicon dies on thin organic substrates or interposers. Differences in coefficient of thermal expansion (CTE) between materials generate significant package warpage during various thermal cycles.

As bump pitch decreases and stand-off heights become smaller, even modest warpage can prevent solder bumps from making proper contact during reflow, resulting in open joints and reduced assembly yield, examples shows in Figure 2. The problem is particularly severe for large-form factor packages used in AI accelerators and HPC devices.

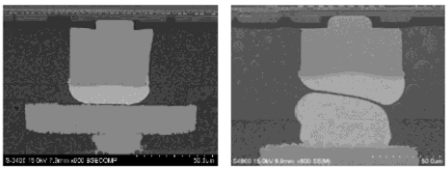


Figure 2. Examples of open joints

C. Fine-Feature Solder Paste Deposition

Increasing integration density within SiP modules requires solder paste deposition on smaller pads with tighter spacing. Traditional solder paste formulations may suffer from poor stencil release, insufficient transfer efficiency, bridging, and inconsistent volume control over time when used with ultra-fine apertures.

As powder size decreases, total surface area increases significantly, making oxidation control and flux formulation design increasingly important. Maintaining print consistency while preventing slumping and bridging becomes a major materials challenge.

III. Material and Process Solutions

A. Ultra-Low-Residue Flux solution [4,5]

One approach to addressing fine-pitch assembly challenges is the adoption of semiconductor-grade ultra-low-residue (ULR) no-clean fluxes.

Unlike conventional no-clean formulations that may leave 20–60% residue after reflow, ULR fluxes are designed to leave less than 10% residue while maintaining adequate wetting performance, refer to Figure 3 below. The significantly reduced residue amount improves compatibility with capillary underfill (CUF) and molded underfill (MUF) materials and eliminates the need for post-reflow cleaning processes.

The reduced residue also minimizes assembly-induced stresses associated with cleaning operations and lowers the risk of contamination beneath fine-pitch interconnects. In volume production environments, ULR fluxes have demonstrated robust wetting performance while supporting high assembly yields for advanced flip-chip applications.

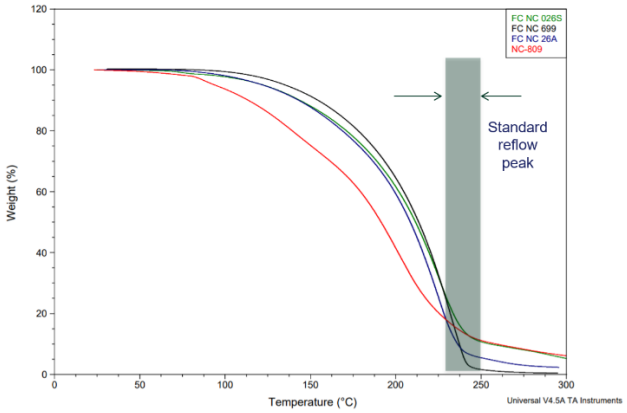


Figure 3. Thermo-Gravimetric Analysis (TGA) of typical ULR fluxes

B. TCB and LAB for Warpage Mitigation [6,7,8,9]

Traditional mass reflow subjects the entire package assembly to extended thermal exposure, typically at least 3-5mins, which can exacerbate substrate and die warpage.

Thermo-compression bonding (TCB) and laser-assisted bonding (LAB) have emerged as effective alternatives for advanced packaging applications. These processes utilize localized heating and significantly shorter thermal cycles, typically just a few seconds, reducing overall package deformation and improving bump contact uniformity.

TCB (Figure 4) combines heat, pressure, and controlled bonding time to establish reliable interconnect formation, but UPH can be greatly shortened as one die is bonded at a time. Whereas, LAB (Figure 5) reduces package stress by using highly localized laser heating and eliminating compressive force during bonding, at the same time with a bigger laser window which typically can heat multiple dies and components at the same time, thus improving UPH. Comparison of mass reflow, TCB and LAB can be referred to in Table 1.

However, these assembly processes impose new requirements on flux chemistry. During TCB, substrates may remain on heated pedestal for extended periods, often at temperatures between 100°C and 180°C. Conventional water-washable fluxes can be excessively burnt and hardened during this exposure, making residue removal difficult and potentially promoting corrosion on fine-pitch copper structures. Specialized TCB fluxes are therefore required to provide rapid activation, excellent wetting, thermal stability, and minimal residue generation.

The combination of optimized process conditions and advanced flux materials enables higher assembly yields for copper pillar and microbump applications commonly used in 2.5D and 3D integration.

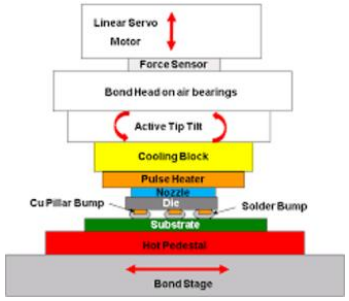


Figure 4. Typical Thermo-compression bonding (TCB)

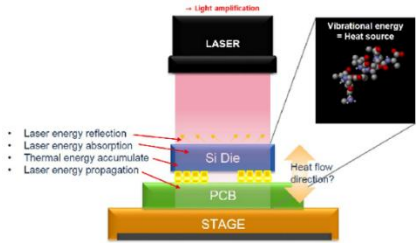


Figure 5. Typical Laser-assisted bonding (LAB)

	Mass Reflow	TCB	LAB
Thermal Stress on ELK	5x	1x	2x
Warpage	High	Low	Low
UPH / Productivity	Fast	Slow/Moderate	Fast
Selective soldering	No	Die only	Yes
Multidie & components	Yes	No	Yes
Selfalignment	Yes	No	Yes
Fine pitchcapability	Challenging	Yes	Yes

Table 1. Comparison of Mass Reflow, TCB and LAB

C. Fluxless Assembly Using Formic Acid Reflow and Adhesive Materials

As advanced packaging continues to push toward true no-clean assembly, fluxless soldering technologies are gaining increased attention.

Formic Acid Soldering Technology (FAST) utilizes reducing gases such as formic acid to remove metal oxides during reflow without requiring conventional flux chemistries. The formic acid reacts with surface oxides and converts them into volatile by-products that are removed during processing, leaving clean metal surfaces for solder wetting, as explained in Figure 6.

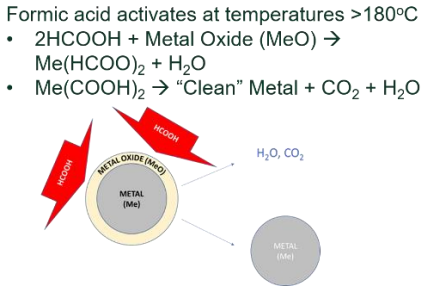


Figure 6. Mechanism of Fluxless Formic Acid Reflow Technology

The resulting process provides several advantages, including elimination of cleaning, reduced contamination risk, lower maintenance requirements, and near-zero post-reflow residue.

One challenge associated with fluxless assembly is maintaining die placement during reflow. To address this issue, specialized adhesive materials have been developed that provide sufficient tack force to hold components in position while remaining fully compatible with formic acid vacuum reflow conditions. These materials leave virtually no residue and support high-reliability assembly for advanced packaging applications, as shown in Figure 7.

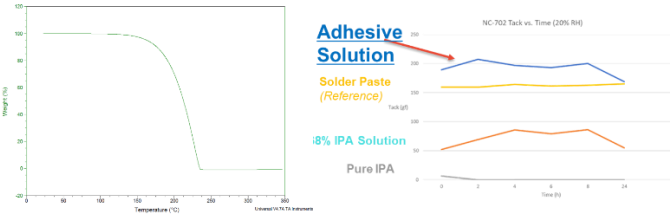


Figure 8. TGA and Tackiness of adhesive material for FAST

D. Fine-Powder Solder Paste for High-Density SiP [10,11,12,13]

High-density SiP applications require increasingly fine solder paste deposition capability. To support aperture dimensions below 100µm, the industry has transitioned from Type 5 and Type 6 powders toward finer Type 7 and Type 8 powder technologies.

Fine powder advancements focus on improved particle sphericity, tighter particle size distribution, and lower oxidation levels. These improvements enable better stencil transfer efficiency, more consistent deposition, and enhanced solder wetting performance.

However, decreasing particle size dramatically increases powder surface area, making oxidation control and flux design increasingly critical. Advanced solder paste formulations therefore incorporate optimized flux systems and rheological properties to maintain print stability while preventing bridging and slump defects.

Ultra-low-residue solder paste technologies further support advanced packaging by minimizing post-reflow residue while maintaining compatibility with underfill and molding materials. These formulations enable true no-clean processing while supporting consistent printing performance at aperture sizes down to approximately 90µm.

For applications where stencil printing is not feasible, dispensing and jetting technologies provide alternative methods for precise solder deposition. These processes are particularly valuable for cavity packages, highly localized solder placement, and variable solder volume requirements.

IV. Conclusions

The continued evolution of heterogeneous integration, 2.5D interposers, 3D stacking, and high-density SiP architectures is creating unprecedented challenges for semiconductor assembly processes. Fine-pitch interconnects, reduced stand-off heights, larger die sizes, and thinner substrates demand new approaches to both materials and process development.

Ultra-low-residue fluxes provide an effective solution for improving underfill compatibility and enabling no-clean assembly. TCB and LAB processes help mitigate warpage-related open joints while supporting increasingly fine interconnect geometries. Formic acid reflow combined with specialized adhesive materials enables fluxless assembly with near-zero residue generation. Meanwhile, fine-powder solder paste technologies support the deposition requirements of next-generation SiP applications.

No single material or process solution can address all advanced packaging challenges. Successful implementation requires a holistic evaluation of package architecture, interconnect design, material compatibility, assembly process requirements, reliability objectives, and overall manufacturing cost. As package complexity continues to increase, close co-optimization of materials, process technologies, and package design will remain essential for achieving high-yield and reliable advanced semiconductor assembly.

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