Packaging Technologies for Modern High-Reliability Electronics for Harsh Environment

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Abstract

Modern high reliability systems require electronic packaging that can withstand extreme thermal, mechanical, and environmental stresses while meeting the demand for increased functional density and a miniaturized design to realize SWAP gains. This paper explores critical design and process considerations for high-reliability applications, focusing on the strategic design and assembly of Ceramic Leadless Chip Carriers (CLCC), ceramic J-Lead and ceramic Area Array (Ball Grid Arrays (CBGA), Ceramic Column Grid array (CCGA) packages. While plastic packages are heavily favored in commercial consumer electronics due to their low cost and lightweight nature, ceramic structures remain indispensable for mission-critical, high-power, and aerospace systems. Several generic ceramic COTS package sizes were tested with different board materials and reliability gains were assessed. Size and material tradeoff studies showed the effect of these factors on reliability. This paper will highlight some of the observations that will guide designers to consider for high reliability.

Keywords: area array packaging, CLCC, CBGA, CCGA, thermal cycling fatigue, solder joint reliability, CTE mismatch, defense electronics, MIL-STD-883

Introduction

Electronics have evolved by packing more Input/Output (I/O) connections using High-Density Interconnect (HDI) technology. This density drives the need for advanced packaging to reduce Size, Weight, and Power (SWAP). However, high-reliability systems require specialized packaging to survive these high-stress, thermo-mechanical fatigue conditions.

Thermo-mechanical fatigue is caused by Coefficient of Thermal Expansion (CTE) mismatch between package and board requiring devices with a CTE closely matched to the printed circuit board [1]. Ceramic Leadless Chip Carriers (CLCC) and ceramic area array packages enable high-density electronics by bridging the CTE mismatch to function in these harsh environments. CLCC packages are standard for low I/O counts, while area array options like Ceramic Ball Grid Arrays (CBGA) and Ceramic Column Grid Arrays (CCGA) are preferred for high I/O electronics

Ceramic Leadless Chip Carrier (CLCC) components (figure 1) are widely used in high reliability applications and provide robust, hermetic sealing and excellent thermal dissipation, but their lack of compliant leads makes CLCCs highly susceptible to solder joint fatigue from thermal expansion mismatches with organic substrates. Under repeated thermal cycling, the CTE mismatch between the ceramic substrate (CTE ≈ 5–7 ppm/°C) and the organic FR-4 or polyimide PWB (CTE ≈ 14–18 ppm/°C) produces cyclic shear strains at the solder joints that accumulate as fatigue damage over thousands of cycles.



Figure 1: Leadless ceramic chip carrier (CLCC)

To mitigate this stress, J-leads offer some mechanical flexibility, yet both packages face physical limits as input/output (I/O) demands grow, since peripheral-leaded packaging cannot scale without drastically increasing package size. This limitation forced an industry shift toward area-array packaging, specifically Ceramic Ball Grid Arrays (CBGA) and Ceramic Column Grid Arrays (CCGA), which utilize the entire underside of the component to maximize I/O density in a compact footprint. Extensive reliability literature indicates that while CBGAs improve interconnect density, their rigid ceramic-to-board joints remain vulnerable to thermal cycling wear;

consequently, CCGAs utilize high-lead solder columns that flex under stress, significantly extending fatigue life in large, high-I/O applications.

The solder interconnections joining an area array package to a printed wiring board (PWB) represent the weakest mechanical link in the assembly. Repeated thermal-cycling fatigue loads throughout a device's service life cause the nucleation and growth of fatigue cracks. When a crack propagates completely through a current-carrying path, the circuit becomes electrically open—this event defines the device's failure.

Ceramic Ball Grid Array

The CBGA is a surface-mount package in which an array of high-lead non-collapsible solder balls (typically 90Pb/10Sn or 95Pb/5Sn) is attached to a ceramic substrate, with eutectic Sn/Pb solder forming the board-side fillet during reflow (figure 2).

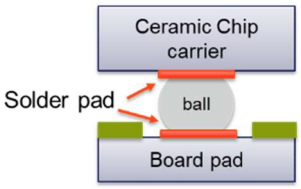


Figure 2 Ceramic Ball grid array (CBGA) Schematic

Non-collapsible balls are preferred as they provide controlled standoff to manage stress generated due to CTE mismatch between ceramic body and organic substrate. The ceramic substrate provides hermetic die enclosure and superior thermal conductivity relative to organic substrates, making it the preferred solution for high-power flip-chip modules. CBGA packages are commercially available in I/O counts ranging from 100s to over 1,000, with common pitches of 1.00 mm and 1.27 mm.

The fundamental reliability limitation of the CBGA is the low standoff height provided by the collapsed solder ball, which is typically 0.5 mm to 0.8 mm after assembly. Typical, classical damage accumulation equation is shown in figure 3, where solder joint damage depends on: package dimensional distance from center to farthest interconnect (distance to neutral point (L_D)) and solder joint height (h). Higher the solder height and smaller the package, would results in less damage accumulation. $\Delta\alpha$ is change in coeff of thermal expansion between ceramic and pwb, ΔT_e is effective temp swing during cycling, F is geometric constant factor.

$$\Delta D\,(leadless) = \left[\frac{FL_D\,\Delta\alpha\,\Delta T_e}{h}\right]$$

Figure 3: Damage Accumulation - Distance to Neutral point Equation [2]

Because the compliance of the interconnect is constrained by this limited height, the full magnitude of the differential thermal displacement between the ceramic package and the PWB is transferred as shear strain into the solder. For large package footprints—common in high-I/O ASICs and FPGAs—the displacement at the corner joints scales with the distance from the neutral point (DNP), resulting in substantially higher strain at outer-array joints than at inner-array joints, and corner-joint failures dominate the observed failure distribution (Perkins & Sitaraman, 2007; Wong et al., 1998).

Ceramic Column Grid Array

The CCGA was developed as a reliability-enhanced extension of the CBGA in which the solder balls are replaced by elongated solder columns, typically 0.5 mm diameter and 2.2 mm in height, composed of 90Pb/10Sn or 80Pb/20Sn high-temperature solder (figure 4).

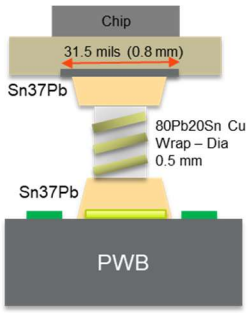


Figure 4: Ceramic Column grid array (CCGA)

The substantially greater standoff height of the column reduces the shear strain transferred to the joint for a given differential thermal displacement, producing a significantly longer fatigue life compared to an equivalent CBGA with the same substrate size and I/O count [3,4]. Alternate column configurations, including copper-ribbon-wrapped columns that provide additional ductility and columns attached via

interposers for reworkability, have also been evaluated [5].

CCGA packages have become the dominant area array format for high-reliability ceramic modules, particularly for FPGAs, digital signal processors, and high-performance ASICs with I/O counts exceeding 560. The column attachment to the ceramic substrate is achieved through a controlled eutectic solder reflow process, and the board-side joint is formed similarly to a CBGA using eutectic Sn/Pb paste. The additional process steps and the mechanical fragility of the columns during handling introduce unique manufacturing quality challenges, including column coplanarity variation and solder void formation, both of which affect board-level reliability [6,7,8].

Thermomechanical Loading Conditions in High Reliability Applications

Modern high reliability electronics encounter a broader and more severe range of thermal environments than most commercial applications. High-altitude aircraft, missiles, and spacecraft impose the most severe conditions with excursions to -65°C on the cold end and to +125°C or beyond on the warm end during operational and storage phases. MIL-STD-883 Method 1010 defines several temperature-cycling test conditions; Condition C (-65°C to +150°C) and Condition B (-55°C to +125°C) are most commonly applied to microelectronic packages intended for high-reliability qualification.

Test Matrix

In this study, following components were evaluated for assembly and thermal cycling survivability. COTS components were selected to analyze reliability trend with size and type. Components were assembled on 100 mils thick polyimide board (figure 6) with CTE in the range of 16 ppm, with typical surface mount assembly using eutectic SnPb solder. Assembly was done in two phases, in the 1st phase build and testing was done with CLCC and J-lead packages and 2nd phase of the testing included CBGA and CCGA area array packages.

CLCC Components (Figure 5)

- 6 LCC – 6.22x4.32 mm, 1.27 mm pitch
- 16 LCC – 6.35 mm sq, 1.27 mm pitch
- 24 LCC – 8.41 mm sq, 1 mm pitch
- 28 LCC – 11.43 mm sq, 1.27 mm pitch
- 32 LCC – 11x14 mm , 1.27 mm pitch

Ceramic J-Lead: 28lead–11x14 mm, 1.27 mm pitch

Area Array Components

- 399 CBGA–21 mm sq, 1 mm pitch
- 483 CBGA–21 mm sq, 1 mm pitch
- 484 CCGA-23 mm sq, 1 mm pitch

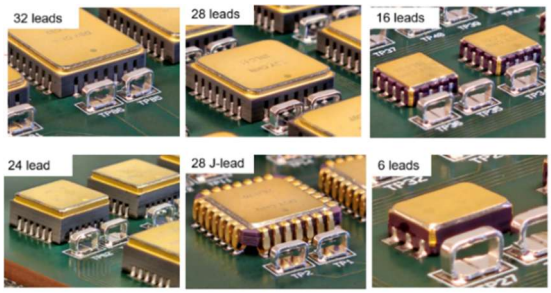


Figure 5:Components on Board

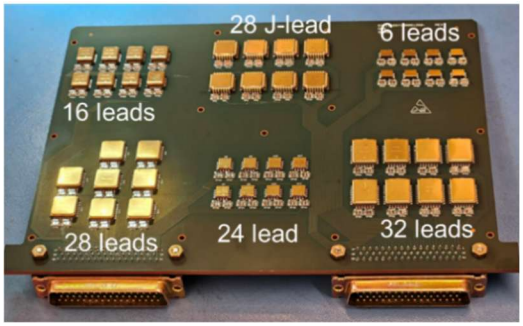


Figure 6: Assembled LCC and J-lead mounted board

LCC and J-lead Assembly and Manufacturing Considerations

Board assembly was performed with SnPb solder paste that was printed on the board and several dimensions of printed solder was recorded to analyze the process variation. One of the critical dimensions that affects thermal cycling life is solder standoff, which is the distance between the PWB and component body. Variation in solder deposit can affect standoff thickness thus affecting the thermal fatigue reliability. All the components showed typical variation and even solder distribution (figure 7). Figure 8 shows solder X-section for one of the components with standoff in the 5 mil range after assembly.

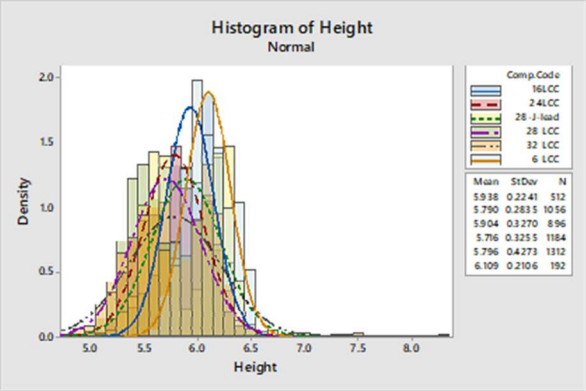


Figure 7: Solder height(mils) before reflow

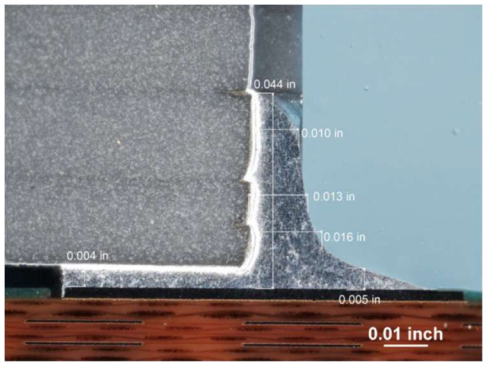


Figure 8: Solder joint after reflow

Post assembly inspection of J-lead component showed open corner joint on one of the components (figure 9), a typical mechanism which should be monitored during J-lead assembly.

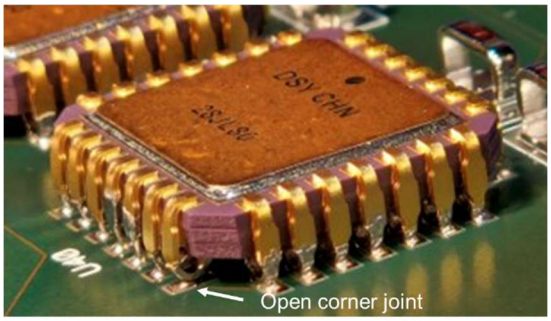


Figure 9: Optical Inspection of J-lead component showing open corner joint

Thermal Cycling Life testing

Boards were thermal cycled in air to air thermal chamber with application specific typical peak temperatures with 130 deltaT between low and hot termpature maintaining 15 min dwell at temperature extremes and 5C/min ramp rate (figure 10). Thermal cycling failures were plotted using Weibull distribution (figure 11) and showed 6LCC to have a superior performance > 1000 cycles compared to all the other CLCC. Testing indicated a significant correlation between reliability and component size with largest 32 pin LCC failing earliest. Testing was stopped by 3000 cycle and no failure of J-lead component was observed indicating significant reliability improvement with compliant J-lead.

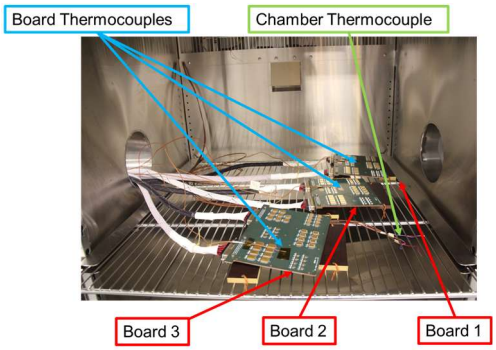


Figure 10: Thermal Cycling Test Setup

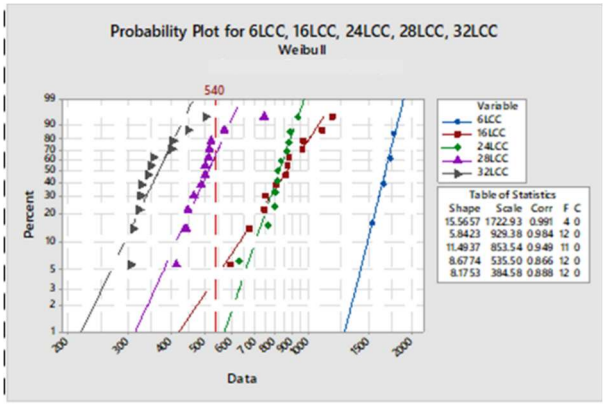


Figure 11: Thermal Cycling Result for CLCC

Conclusions: CLCC and J-lead

For high reliability applications, for smaller I/O devices smaller LCC packaging should be selected whereas, where higher I/O are needed J-lead packaging should be considered.

CBGA Test Vehicle

Although, J-lead packages provide significant reliability gains, but are limited by number of I/O that can be accommodated without increasing package size significantly. Need for higher >100's I/O triggers the need for area array components like CBGA followed by even higher I/O enabled by CCGA technology.

Figure 12, shows assembled board with area array components.

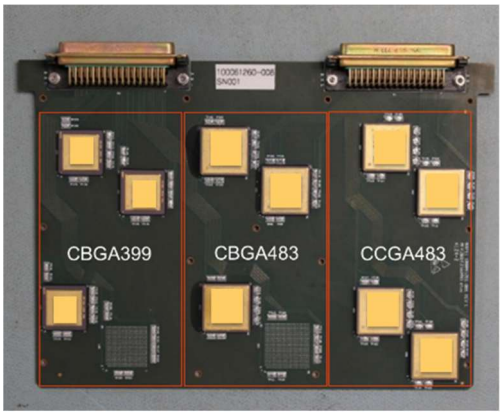


Figure 12: CBGA and CCGA Assembled Board

Manufacturing Considerations with CBGA

COTS CBGA components with 90Pb/10Sn non collapsible balls were used for testing. Solder balls were attach to HTCC ceramic body with eutectic SnPb solder paste. Inspection revealed voiding in solder fillet area (Figure 13). Presence of excessive voiding could lead to crack initiation resulting in early failures.

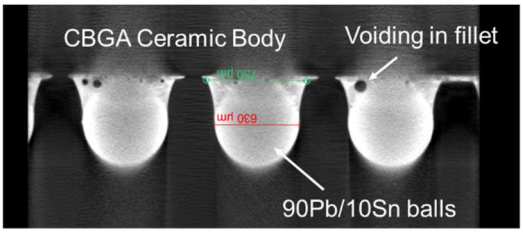


Figure 13: Voiding in SnPb solder fillet - as received COTS

CBGA assembly process relies on self alignment, being a heavy component there is a tendency to get misalignment that can affect solder joint fatigue life. Figure 14 shows aligned joints whereas Figure 15 shows misalignments. Misalignment specs would be required to be tighter for high reliability hardware.

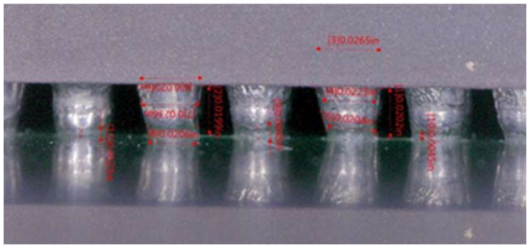


Figure 14: Aligned CBGA Solder joints

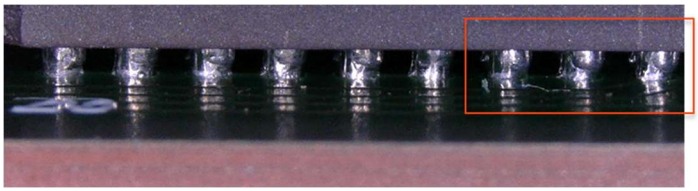


Figure 15: Misaligned CBGA Solder joint

Figure 16 shows a typical symmetric solder joint that was achieved in this work after developing a controlled soldering process.

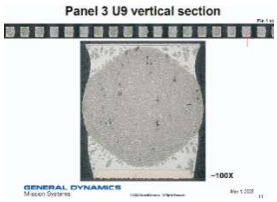


Figure 16: Solder joint for CBGA after assembly

Thermal Cycling Testing for CBGA

Solder joints of CBGA components are susceptible to thermal fatigue due to high CTE mismatch between ceramic body (CTE:~7 ppm/C) and PWB (CTE:~16 ppm/C)**.** By dispensing a liquid epoxy resin under the component and allowing it to capillary flow into the gap, the underfill encapsulates the solder bumps and distributes the mechanical stress uniformly across the entire package area. Once cured, this material is intended to significantly enhances the structural integrity and thermal fatigue life of the CBGA assembly, while also providing protection against moisture, environmental contaminants, and mechanical shock or vibration. Baseline test was run without underfill to evaluate thermal cycling life. Figure 17 shows fatigue life comparison for CBGA 399 (21 sq mm) and CBGA 483 (23 sq mm) component. Even though both CBGA didn't meet high reliability without UF, smaller CBGA showed better life inline with DNP principle that shorter the distance to neutral point better life would be realized.

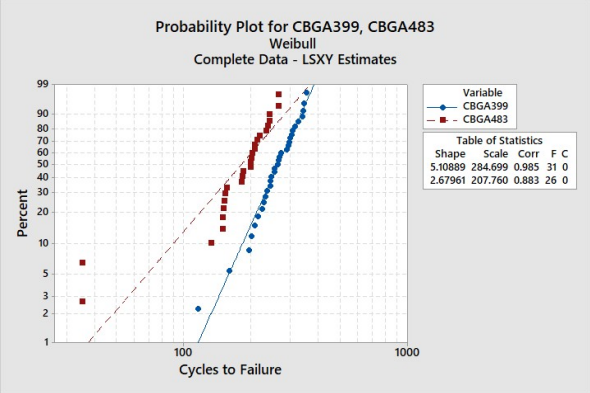


Figure 17: Thermal Cycling life CBGA without UF

Further testing was conducted after underfilling the parts. Several UF material were screened and one of them was selected for underfilling. It was observed that early delamination occurred between the ceramic and UF interface. Analysis through Ansys simulation revealed presence of high stress in the fillet area resulting in delamination (figure 18).

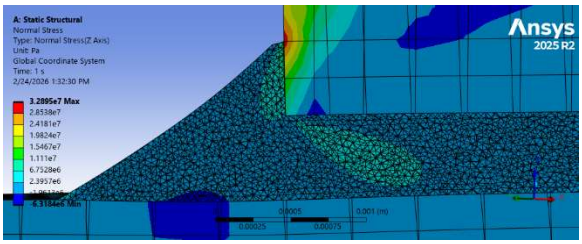


Figure 18: High stress area near fillet of UF to CBGA substrate

Table 1 shows, with 25% fillet stresses dropped down significantly, normal stress went from 18 MPa tensile to 3.2 MPa compressive, whereas Von Mises stress dropped from 61.3 MPA to 16.2 MPa.

Table 1: Effect of UF fillet on Interfacial Stress

Model ID	Normal $\sigma_{interface}$ [MPa]	Von Mises $\sigma_{interface}$ [MPa]
CBGA483_A – No Fillet	18.0	61.3
CBGA483_D With 25% Fillet	-3.2	16.2

Several factors were identified that contribute to increasing life of CBGA and are being verified by testing. *Type of Underfill – CTE Matched to Ceramic*

- *Underfill fillet – 25 to 50% Minimum*
- *Smaller CBGA size – 12 sq mm and 18 sq mm (Reduce distance to neutral point)*
- *PWB CTE – 6 ppm, 10 ppm and 16 ppm (Lower CTE plays a significant role in increasing life)*
- *Ball height – 0.635 mm, 0.75 mm (large ball increases standoff thus resulting in increased life)*
- *Substrate thickness (Thinner substrate results in higher life), not always applicable due to component routing requiring thicker substrate.*

Although, CBGA components provide high I/O counts, they are hard to rework as several UF providing higher life are non-reworkable and pose a repair concern. For expensive components, preferred approach would be to select CCGA those don't require UF can be replaced and reworked.

CCGA Thermal Cycling Testing

For even higher >500 I/O counts CCGA components provide higher life. We have completed 2 rounds of testing with CCGA483 with shorter 1.6 mm Cu wrapped columns and have observed superior reliability compared to CBGA and are being considered for high reliability packaging option for higher I/O counts.

Manufacturing Considerations for CCGA

Although CCGA components provide reliability advantage there are several manufacturing challenges. Couple of observations were realized while assembly of CCGA. This study used Cu wrapped columns.

1) Bent pins and uneven solder fillet on as received COTS components (figure 19)

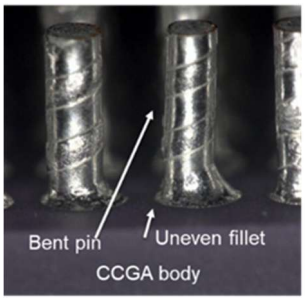


Figure 19: As received Cu Wrapped CCGA columns

2) Similar to CBGA assembly, CCGA components also depend on self alignment and have tendency to offset during assembly. Figure 20 a good

aligned joint, where as , Figure 21 shows bent leads.

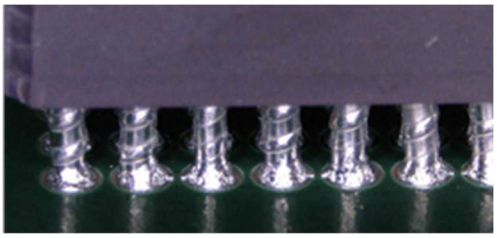


Figure 20: CCGA Assembly



Figure 21: CCGA Assembly with bent columns

Future work is ongoing to test Shock and Vibration life for CCGA components.

Conclusion

The program demonstrated that package selection must be driven by the required I/O count and the reliability level of the target application.

- For low-I/O, high-reliability designs the smaller lead-frame LCC packages (e.g., 6-LCC) provide the longest thermal-cycling life, exceeding 1000+ cycles, while larger 32-pin LCCs fail earliest.
- When higher I/O counts are needed, compliant J-lead components outperform LCCs, showing no failures after 2000 cycles, making them the preferred choice for medium-density boards.

Area-array technologies extend the I/O capability further, but introduce new reliability considerations:

- CBGA devices achieve higher pin counts but are susceptible to thermal fatigue because of the ceramic-to-PCB CTE mismatch. Applying an underfill that dramatically reduces interfacial stresses and improves fatigue life. Smaller CBGA die sizes, lower PCB CTE, and taller solder balls also contribute to longer life.
- CCGA packages combine very high I/O (> 500 pins) with superior thermal-cycling reliability without requiring underfill, but they pose manufacturing challenges such as bent columns, misalignment, and solder-fillet irregularities that must be controlled. Ongoing work will evaluate their shock and vibration performance.

Overall, the study illustrates by selecting smaller package, using appropriate underfill, or employing low-CTE substrates—enhances solder-joint fatigue resistance. For high-reliability applications, the hierarchy of preferred packages is:

1. Small-LCC for low-I/O,
2. J-lead for moderate-I/O,
3. CBGA with optimized underfill for higher-I/O, but affect reworkability.
4. CCGA for the highest I/O density and offers reworkability option.

These guidelines provide a roadmap for designers to balance I/O requirements, assembly cost, and long-term reliability in advanced electronic systems

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