Reverse Laser Thermo-Compression Bonding (R-LTC) for Simultaneous Thermal Uniformity and Thermomechanical Stress Mitigation in Heterogeneous Chiplet Integration

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Abstract

Chiplet-based heterogeneous integration has become a key packaging approach for high-performance artificial intelligence systems; however, assembly-induced warpage, stand-off height (SOH) non-uniformity, and accelerated intermetallic compound (IMC) growth remain major challenges in large-area modules. These issues are primarily driven by a mismatch in the coefficient of thermal expansion (CTE) and non-uniform heat distribution during solder bonding.

This study introduces a Reverse Laser Thermo-Compression bonding (R-LTC) scheme based on thermal inversion, in which heat is delivered from the substrate side rather than the chiplet side. This approach fundamentally modifies the heat flow path in heterogeneous structures, mitigating thermal gradients induced by mismatches in thermal conductivity.

A systematic comparison of reflow, Top Laser-Assisted Bonding (T-LAB), Reverse Laser-Assisted Bonding (R-LAB), Thermo-Compression Bonding (TCB), and R-LTC was conducted under conditions where the edge Cu-pillar bump temperature reached 245 ± 5 °C. The results demonstrated that conventional approaches have difficulty simultaneously achieving thermal uniformity and minimizing thermomechanical stress in heterogeneous structures, highlighting a critical limitation in current bonding technologies.

Under the same conditions, R-LTC demonstrated a significant reduction in temperature non-uniformity (ΔT reduced from 52 °C to 4 °C) and suppressed IMC thickness by ~26% compared to TCB, while maintaining comparable SOH control and warpage behavior. This substrate-driven heat flux homogenization, together with reduced thermal exposure time, minimizes diffusion-driven interfacial reactions and is expected to reduce thermomechanical stress, as supported by simulation results showing decreased von Mises stress.

This study demonstrates that thermal inversion is a promising design approach for bonding processes, enabling scalable and reliable heterogeneous integration for next-generation 2.5D/3D packaging.

Keywords

2.5D/3D packaging, heterogeneous integration, reverse laser thermo-compression bonding (R-LTC), stand-off height (SOH) uniformity, warpage control.

I. Introduction

The rapid expansion of artificial intelligence (AI) workloads continues to intensify demand for high-performance semiconductor systems, positioning chiplet-based architectures as a key enabler for scalable integration. Unlike monolithic scaling - where a single defective functional block can render an entire die unusable while driving up design complexity and cost - chiplet modules enable the partitioning of logic, memory, analog, RF, and I/O functions into separately optimized dies. Such heterogeneous integration provides flexibility and yield advantages and has become widely adopted in advanced 2.5D and 3D packaging [1][2].

Despite rapid advances, achieving simultaneous control of thermal gradient, mechanical deformation, and interfacial

reaction kinetics remains a fundamental challenge in heterogeneous integration. Mismatch in coefficient of thermal expansion (CTE), combined with dissimilar thermal conductivities among stacked materials, induces severe warpage and non-uniform thermal profiles during solder interconnection. These effects degrade stand-off height (SOH) uniformity, reduce interconnect yield, and compromise long-term reliability, particularly as chiplet and substrate sizes continue to increase [3][4][5][6].

Various bonding approaches have been used to address these issues, each with inherent limitations. Reflow provides uniform heating through hot-air convection; however, long dwell times and large thermal budgets exacerbate CTE-driven warpage and promote excessive intermetallic compound (IMC) growth [7]. Laser-assisted bonding (LAB) reduces thermal exposure through localized and rapid heating, and results in thinner IMC formation [8]. Yet, as module size scales, warpage control becomes increasingly difficult, and heterogeneous assemblies tend to suffer from temperature non-uniformity [9][10].

Thermo-compression bonding (TCB) employs vacuum-assisted clamping using a bond head and stage block, enabling precise Z-axis control and mitigating warpage. However, direct top-side heating of the chiplet module induces asymmetric heat flow within the heterogeneous stack [11].

Owing to the orders-of-magnitude disparity in thermal conductivity between silicon (~150 W/m·K) and epoxy molding compound (EMC, ~0.5–1 W/m·K), heat propagation becomes highly non-uniform, resulting in large temperature gradients across the chiplet as shown in Fig. 1

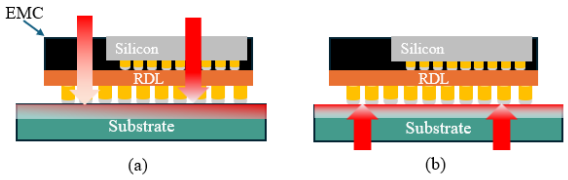


Fig. 1. Heat flow direction and thermal uniformity in heterogenous stack : (a) top side heating with non-uniform temperature - large ΔT, (b) bottom side heating with uniform temperature – small ΔT.

This gradient generates local thermomechanical stress and promotes non-uniform interfacial reactions, and the growth of intermetallic compounds (IMCs) during the bonding process follows diffusion-controlled kinetics:

$$x = k * t^n = k_0 \exp(\frac{-Q}{RT}) t^n$$

where x is the IMC thickness, k is the growth rate constant, t is the bonding time, T is the absolute temperature, Q is the activation energy, and R is the gas constant [12][13] .

In heterogeneous stacks, the significantly lower thermal conductivity of epoxy molding compound (EMC) compared to silicon limits heat dissipation, particularly near the chip edges. This results in pronounced temperature non-uniformity (ΔT) across the chiplet.

The temperature difference can be expressed as:

$$\Delta T \propto \frac{q \cdot L}{k}$$

where q is the heat flux, L is the material thickness, and k is the thermal conductivity. This relationship indicates that low thermal conductivity regions, such as EMC, act as thermal bottlenecks, leading to steep temperature gradients.

These temperature gradients generate non-uniform thermomechanical stress and variations in interfacial reaction kinetics, thereby accelerating localized IMC growth and degrading interconnection reliability.

Consequently, an effective bonding approach must simultaneously minimize thermal gradients, reduce chiplet-side thermal stress, suppress CTE-induced deformation, and shorten thermal exposure time.

We demonstrate that the direction of heat flow, rather than simply thermal magnitude, fundamentally determines temperature uniformity, stress evolution, and interfacial reaction kinetics in heterogeneous integration.

This work introduces a reverse laser thermo-compression (R-LTC) bonding architecture that addresses these requirements. In R-LTC, a transparent quartz stage enables substrate-side laser irradiation, establishing an inverted heat path in which the peak temperature is localized at the substrate rather than the chiplet module. A bond head applies mechanical force from the top to control the Z-axis and ensure uniform SOH, while providing only supportive heating. This configuration allows laser power to be minimized and cooling rates to be controlled.

The key contributions of this work are summarized as follows. First, chiplet-side thermal stress is significantly reduced by shifting the thermal peak away from the chiplet module, compared with conventional technologies. Second, substrate-side laser heating promotes uniform heat flow into solder interconnects, even in heterogeneous stacks. Third, vacuum clamping of both the chiplet module and substrate, combined with Z-axis control, effectively suppresses warpage and improves SOH uniformity. Finally, the large-area reverse laser enables simultaneous chiplet module and component attachment, simplifying process flow, reducing cycle time and equipment footprint, and suppressing excessive IMC growth through a short, well-controlled thermal profile.

This study aims to experimentally and analytically verify how inversion of heat flow direction affects temperature uniformity, thermal stress, and IMC growth in heterogeneous

chiplet integration.

II. Experimental procedure

2.1 Chiplet Module Fabrication

The chiplet module used in this study consists of two chiplets with areas of 14 mm x 14 mm and 15 mm x 14 mm, respectively, mounted on a redistribution layer (RDL), resulting in a total molded module area of 32 mm x 16 mm. Cu pillar bumps with a height of 60 µm were employed as the interconnection structure.

Following assembly, the chiplet module was encapsulated using an EMC and subsequently subjected to a grinding process until the chiplet surfaces were exposed.

The substrate used for bonding had a total area of 50 x 32 mm. Multi-layer ceramic capacitor (MLCC) pads were designed and positioned around the chiplet module to enable simultaneous passive component integration. A schematic illustration of the overall structure and key information are shown in Fig. 2 and Table I.

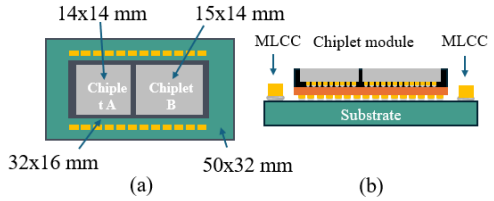


Fig. 2. Chiplet module configuration:
(a) Top view, (b) Side view.

Table I. Test vehicle information

Category	Parameter	Value
Module	Chiplet A size	14 mm x14 mm
	Chiplet B size	15 mm x14 mm
	Size	32 mm x16 mm
	Cu pillar	60 um
Substrate	Size	50 mm x 32 mm
	Pad finish	SOP (Sn-based) on ENEPIG

Fig. 3 shows that the chiplet module exhibited significant warpage change during thermal cycling, decreasing from approximately 370 µm at 25°C to -100 µm at 250°C, and increasing to 400 µm upon cooling. In contrast, the substrate showed relatively small variation, ranging from -30 µm to -65 µm and recovering to -50 µm. This behavior indicates pronounced thermal hysteresis in the chiplet module, while the substrate remains relatively stable.

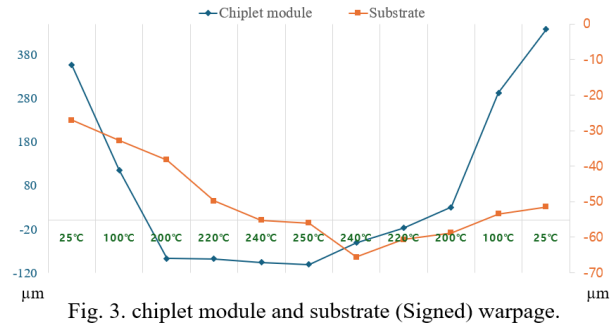


Fig. 3. chiplet module and substrate (Signed) warpage.

2.2 Simulation Conditions

To analyze the thermal and mechanical behavior of the package, a 3D 1/4 symmetric finite element model was developed. This model includes the die, EMC, RDL, and substrate layers, with an overall size of 25 mm × 16 mm.

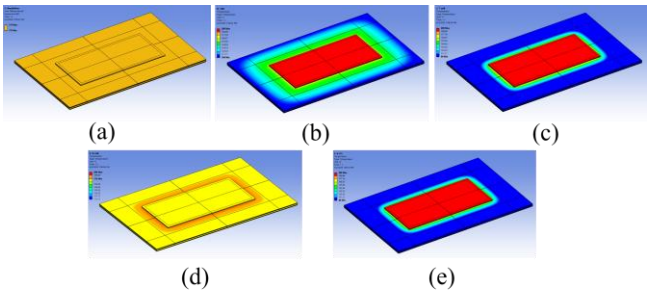


Fig. 4. Comparison of temperature distributions for different bonding technologies obtained by finite element analysis:
(a) MR, (b) TCB, (c) T-LAB, (d) R-LAB, and (e) R-LTC.

For model simplification, as shown in Fig. 4, underfill fillets were ignored, and copper filler interconnects were approximated as equivalent underfill layers. The RDL and substrate trace layers were modeled using effective material properties considering metal area coverage of 60% and 75%, respectively.

A stress-free reference temperature of 175°C was assumed, corresponding to the approximate solidification temperature of the solder under reflow conditions. Above this temperature, the solder remains in a liquid or semi-liquid state and cannot effectively transfer mechanical loads between the chiplet module and the substrate. As a result, thermomechanical stresses are considered to develop primarily during cooling below this temperature due to CTE mismatch.

Although the chiplet module appears nearly isothermal owing to the high thermal conductivity of silicon, significant thermal gradients are concentrated in low-thermal-conductivity regions, particularly within EMC.

The simulation results in Fig. 5 show that the warpage behavior strongly depends on the thermal gradient induced by the heating configuration.

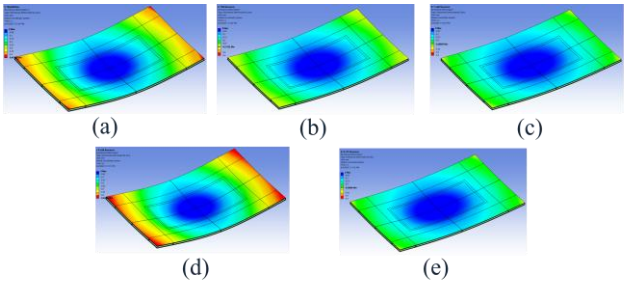


Fig. 5. Simulated warpage contours based on exaggerated out-of-plane (Z-direction) deformation for various bonding processes under a dead-bug configuration: (a) Reflow, (b) TCB, (c) T-LAB, (d) R-LAB, and (e) R-LTC.

As shown in Figs. 6 and 7, using the reflow process as the baseline, the R-LTC and Top Laser Assisted Bonding (T-LAB) processes exhibited the lowest warpage, and the die stress was evaluated using von Mises stress.

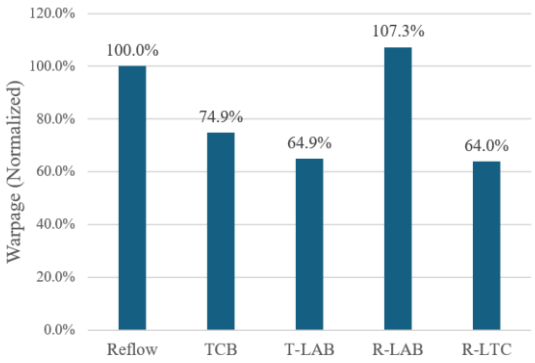


Fig. 6. Comparison of normalized warpage at room temperature for different bonding processes.

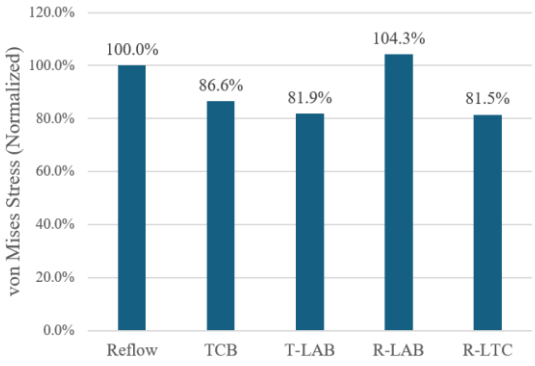


Fig. 7. Comparison of normalized die stress at room temperature for different bonding processes.

2.3 Bonding Process Conditions

To compare different bonding technologies, all processes were conducted under controlled thermal conditions, where the temperature at the edge of Cu pillar bumps reached 245 ± 5 °C. The bonding process endpoint was defined as the point at which the temperature decreased to 170°C during cooling.

A total of thirty samples were fabricated across two experimental runs, with fifteen samples fabricated in each run. Evaluation of subsequent experimental conditions was discontinued once interconnection failure was observed.

For comparison of bonding technologies, reflow using hot-air convection, T-LAB (top-side laser heating), Reverse Laser Assisted Bonding (R-LAB; substrate-side laser heating), TCB, and R-LTC were investigated. The corresponding structures are shown in Fig. 8.

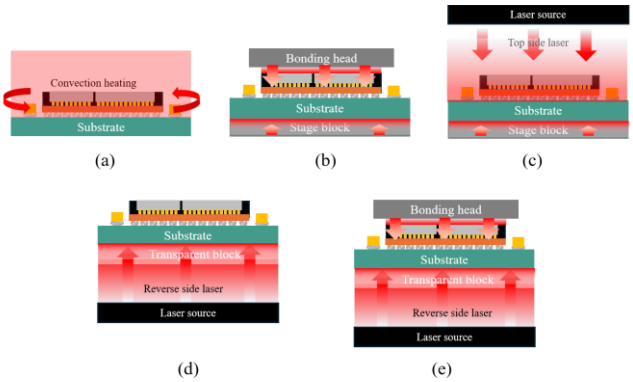


Fig. 8. Schematic illustration of thermal pathways for bonding technologies: (a) Reflow, (b) TCB, (c) T-LAB, (d) R-LAB, (e) R-LTC.

2.4 Temperature Uniformity Measurement

Test samples equipped with thermocouples at the center and edge of the chiplet module were fabricated using TCB bonding to evaluate temperature uniformity during each bonding process, as shown in Fig. 9.

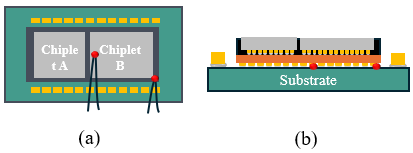


Fig. 9. Thermocouple kit position for bumps temperature: (a) Top view, (b) Side view.

The temperature difference (ΔT) between these two locations was used as a quantitative metric for evaluating the uniformity of thermal distribution across the chiplet module for each bonding condition.

2.5 Structural Analysis and SOH Evaluation

To assess the SOH of the joints, gap uniformity and interconnection morphology were evaluated. The target

SOH was set to 60 μm, and cross-sectional analysis was performed on five samples per process, focusing on both the central and outer regions of the chiplet module.

The stand-off height (SOH) was measured using an optical microscope (STM6, Olympus).

2.6 Warpage Characterization

Warpage of the bonded structures was measured using a shadow moiré system after bonding and underfill process, a non-contact optical metrology technique that quantifies out-of-plane deformation by analyzing interference fringe patterns generated from a reference grating.

The maximum displacement and curvature were extracted as key parameters to compare thermomechanical deformation induced by each bonding process.

2.7 IMC Growth Analysis

The IMC growth was characterized by cross-sectioning the Cu pillar bump interconnections, followed by SEM observation (Regulus 8220, HITACHI) at a magnification of 5000×. IMC thickness was measured at the same locations as those used for SOH evaluation to ensure consistency.

To investigate the influence of heat flow direction, the IMC thickness was measured separately on the chiplet side and the substrate side. The average thickness was determined from five points in both the center and edge regions.

2.8 Process Simplification Evaluation

To evaluate process integration capability, MLCC components (0402 size, 1.0 mm × 0.5 mm) were simultaneously attached to the substrate pads around the chiplet module during bonding.

Flux was applied prior to placement, and the bonding of both the chiplet module and MLCC components was performed using the R-LTC process.

The bonding quality was assessed via cross-sectional analysis, and IMC thickness at the solder joints and failure modes were classified into ductile and brittle types based on fracture surface characteristics.

2.9 Reliability Testing

Thermal cycling (TCG) was conducted to evaluate the reliability of the interconnections under thermomechanical stress. The test conditions ranged from -40 °C to 125 °C, with a dwell time of 10 minutes at each temperature and a ramp rate of 15 °C/min during thermal cycling. Samples were inspected at intervals of 500 and 1000 cycles to monitor degradation.

Following each interval, cross-section analysis was performed to examine the solder joints using SEM at various magnifications (e.g., 1500× ~ 5000×) to identify crack initiation and propagation caused by CTE mismatch.

III. Results and Discussion

The discrepancy between the simulation results and the experimental bonding yield can be primarily attributed to differences in mechanical constraint during the bonding process. In particular, the presence or absence of vacuum clamping significantly affects the bonding performance.

While clamping dominates global warpage behavior, thermal gradient primarily governs local thermomechanical stress. The simulation did not consider vacuum clamping conditions and did not reflect the mechanical constraints present during the bonding process.

In the case of T-LAB, direct top-side heating without chiplet module clamping resulted in bonding failure despite a temperature difference of ΔT = 40 °C. In contrast, TCB achieved 100% yield, which can be explained by the application of mechanical clamping on both the top and bottom sides, effectively suppressing warpage even in the presence of a large temperature gradient (ΔT = 52 °C).

Although the bonding yield of both the TCB and R-LTC processes was 100%, R-LTC resulted in a 26% thinner IMC layer due to the shorter bonding time and exhibited the lowest temperature difference among the successful bonding processes. A summary of the bonding conditions and corresponding results is provided in Table II.

Table II. Interconnection results by bonding technology

Bonding technology	R-LTC	TCB	R-LAB	T-LAB	Reflow
Temperature (ΔT, °C)	4	52	22	40	1
Vacuum clamping	Top Bottom	Top Bottom	Bottom	Bottom	-
Interconnection Result (Yield)	Successful (100%)	Successful (100%)	Failed (25%)	Failed (0%)	Failed (15%)
Bonding time(s)	Short	Long	Short	Very short	Very long
IMC thickness (%)	-26%	baseline	-	-	-

3.1 Temperature Uniformity Measurement

When the edge bump temperature reached 245 ± 5 °C under the conditions summarized in Table III, distinct differences in temperature distribution were observed depending on the bonding process. Achieving complete melting of the entire bump for reliable interconnection requires higher temperatures, depending on the direction of the heat source.

Although bonding failures were observed due to severe deformation during the bonding process, separate samples were fabricated using the TCB process for thermocouple measurements, enabling analysis of their thermal characteristics.

TCB exhibited a significantly larger temperature difference of 52 °C between the center and edge bumps.

This discrepancy is attributed to the heterogeneous thermal conductivity of the chiplet structure, particularly between the EMC and silicon regions, where limited heat conduction across dissimilar materials leads to pronounced temperature gradients when heating is applied from the chiplet side.

In contrast, R-LTC reorients the thermal gradient by introducing substrate-side laser heating, and, in combination with controlled top-side support heating from the bond head, effectively minimizes vertical temperature gradients.

Consequently, the substantial reduction in ΔT suggests that thermal inversion alleviates heat accumulation at low-conductivity EMC regions, mitigating major thermal bottlenecks in heterogeneous structures.

Table III. Process conditions and thermal response for each bonding technology

Bonding technology	**R-LTC**	**TCB**	**R-LAB**	**T-LAB**	**Reflow**
Conditions					
Bond head temp(°C)	<220	>220	N/A	N/A	N/A
Stage temp(°C)	Low	High	Low	Low	N/A
Bonding force(N)	Same	Same	N/A	N/A	N/A
Bonding time(s)	Short	Long	Short	Very short	Very long
Heating configuration					
Heating direction (Heat source side)	**Bottom** (main) + Top	**Top** (main) + bottom	Bottom	**Top** (main) + bottom	Top + bottom
Thermal response					
Bump temperature (center/edge,°C)	249/245	297/245	267/245	288/248	249/250
Bump temp ΔT (center – edge,°C)	4	52	22	40	1

3.2 SOH Evaluation

Both R-LTC and TCB achieved the target SOH of 60 µm with no statistically significant difference (t = -0.41, p = 0.679), with a 95% confidence interval of -1.77 to 1.16 µm.

These findings suggest that SOH is primarily governed by Z-axis mechanical control provided by the bond head rather than by the heating direction, as shown in Fig. 10. Therefore, the thermal inversion in R-LTC does not compromise geometric uniformity of the solder joints.

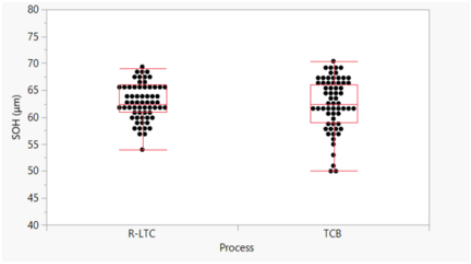


Fig. 10. Comparison of SOH (µm) between R-LTC and TCB

3.3 Warpage Characterization

Fig. 11 compares the warpage of R-LTC and TCB during thermal cycling. A two-way ANOVA revealed no significant interaction between "Process" and "Thermal Stage" (F = 0.96, p = 0.482), suggesting that there is no significant difference in warpage behavior between the two processes during thermal cycling. These results indicate that, under the given bonding conditions, the R-LTC process exhibits thermomechanical deformation behavior similar to the TCB process.

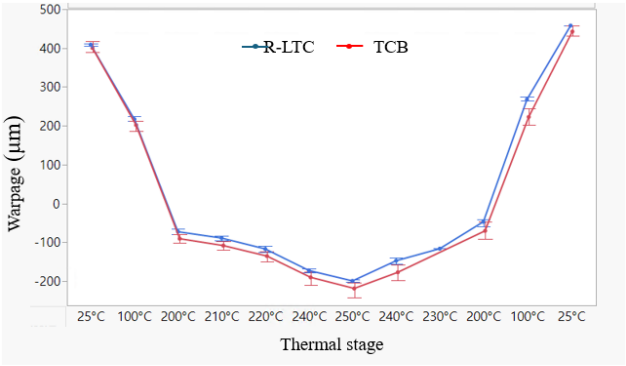


Fig. 11. Comparison of warpage (µm) between R-LTC and TCB after bonding.

3.4 IMC Growth Analysis

Fig. 12 shows that the IMC thickness of R-LTC was approximately 26% thinner than that of TCB (t = 9.3, p < 0.001) with a 95% confidence interval of 0.60 to 0.92 µm, after bonding. This reduction in thickness is primarily attributed to the shortened thermal exposure time resulting from localized heating on the substrate side. According to diffusion control kinetics, IMC growth is highly dependent on both temperature and time, making it important to minimize the thermal budget.

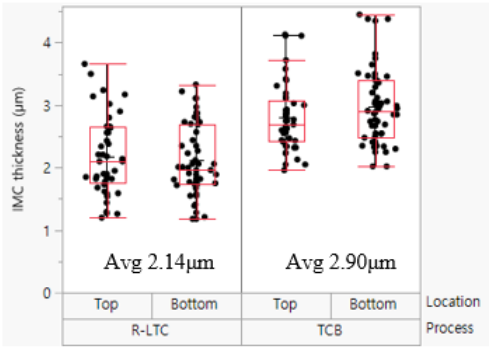


Fig. 12. Effect of Process and Location on IMC Thickness

Additionally, IMC thickness was measured on both the chiplet and substrate sides to evaluate the effect of heating direction on IMC growth. Measurements were performed at both center and edge bumps. No statistically significant difference in IMC growth was observed with respect to the heating direction. The R-LTC showed $t = 0.54$, $p > 0.59$ with a 95% confidence interval of -0.17 to 0.30 μm and TCB showed $t = -1.54$, $p > 0.13$ with a 95% confidence interval of -0.40 to 0.05 μm. These results indicate that IMC growth is primarily governed by temperature and dwell time rather than the direction of heat flow.

Fig. 13 shows that the TCB process results in more coarsened IMC formation than R-LTC. The IMC formed by TCB exhibited a thicker and coarser morphology than that formed by R-LTC. This difference is attributed to enhanced atomic diffusion during high-temperature, long-duration bonding, which accelerates IMC growth and promotes coarsening via Ostwald ripening. In contrast, R-LTC results in a finer and more uniform IMC layer due to suppressed diffusion under lower bonding temperature and shorter processing time.

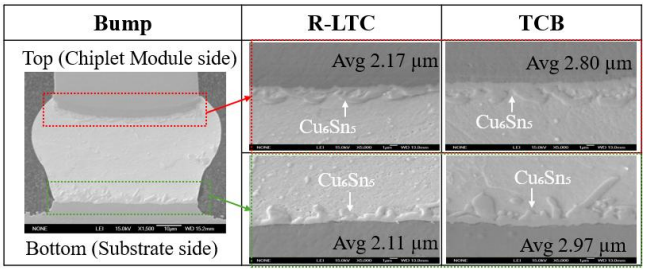


Fig. 13. Cross-sectional SEM images of bump interfaces for R-LTC and TCB processes at chiplet module side and substrate side.

3.5 Process Integration Capability

The R-LTC process successfully enabled simultaneous bonding of chiplet modules and passive components (MLCCs), demonstrating its capability for process integration. Fig. 14 shows that the dominant failure mode was ductile failure (>50% of the fracture area), which indicates that IMCs were well formed.

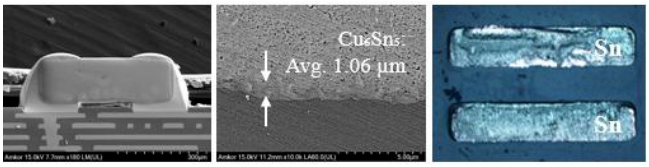


Fig. 14. MLCC attachment using the R-LTC : (a) cross-sectional image, (b) IMC growth, (c) fracture surfaces after shear test.

3.6 Reliability Testing

No defects, such as delamination or cracks in the solder joints, were observed in either the R-LTC or TCB process during the TCG test up to 1000 cycles.

During TCG cycling, IMC growth was observed in both bonding processes. However, no growth of Cu_3Sn formation was observed, and only the growth of Cu_6Sn_5 was detected. This is shown in Fig. 15.

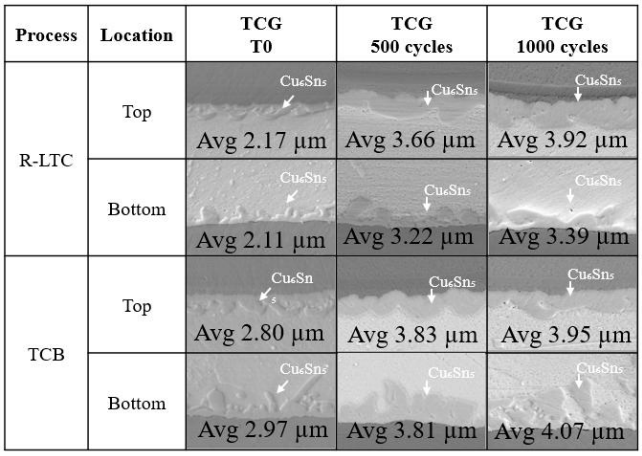


Fig. 15. Cross-sectional SEM images of bump interfaces for R-LTC and TCB processes at TCG T0, 500 and 1000 cycles.

The IMC growth rates were calculated separately for the T0 to 500 cycle and 500 to 1000 cycle intervals. The R-LTC process showed a higher IMC growth rate than TCB in the early stages of thermal cycle (T0 to 500 cycle), but the growth rate of both processes decreased significantly in the later stage (500 to 1000 cycle). This behavior can be explained by diffusion-controlled kinetics: when the IMC layer is thin, the diffusion path is shorter, facilitating faster atomic transport, whereas thicker IMC layers impose a longer diffusion path, thereby reducing the effective growth rate. Consequently, the difference in IMC thickness between the two processes decreases over time. This is summarized in Table IV.

Table IV. Comparison of IMC growth ratios under different TCG cycles for R-LTC and TCB process

Process	Location	TCG cycles	
		T0 → 500 cycles	500 →1000 cycles
R-LTC	Top	68.7 %	7.1 %
	Bottom	52.6 %	5.3 %
TCB	Top	36.8 %	3.1 %
	Bottom	28.3 %	6.8 %

Conclusion

This study establishes that heat-flow direction is a critical governing factor in heterogeneous integration, strongly influencing temperature distribution and indirectly affecting interfacial reaction kinetics through the resulting thermal exposure condition.

By implementing thermal inversion through substrate-side laser heating, R-LTC fundamentally modifies heat distribution within the structure, leading to enhanced interconnect uniformity and maintaining interconnection reliability.

Experimentally, R-LTC significantly improved thermal uniformity (ΔT: 52 °C to 4 °C) and reduced the as-bonded IMC thickness by approximately 26% compared with TCB, while simulation results suggested mitigation of localized thermomechanical stress concentrations during bonding. Furthermore, no cracks or delamination were observed in solder joint cross-sections after up to 1,000 thermal cycles.

This improvement is attributed to the mitigation of thermal bottlenecks in low-thermal conductivity regions such as EMC, enabling more uniform heat propagation across heterogeneous structures in the chiplet module.

Notably, these results indicate that heat-flow direction is a key design parameter, in addition to mechanical constraint and thermal exposure time, for governing bonding performance in heterogeneous chiplet integration. These findings provide new insights into bonding design strategies, positioning thermal-path engineering as a key enabler for scalable chiplet integration.

Taken together, these findings demonstrate that the proposed approach overcomes a key limitation of conventional bonding technologies, which have been unable to simultaneously achieve uniform thermal distribution and reduced thermal stress at the die and bump levels within the chiplet module in heterogeneous structures.

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