Takeaway & Assignment of Packaging Technology for Heterogenous + Large Body Packages

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Abstract

For decades, Moore's Law has driven semiconductor scaling by improving transistor density, performance, and cost efficiency. However, as technology approaches sub-1 nm nodes, physical and economic limitations—including rising design complexity, mask cost, and yield challenges—have slowed this trend, making large monolithic SoCs increasingly unsustainable. Consequently, advanced packaging has emerged as a key driver of system-level scaling, with heterogeneous integration extending Moore's Law in a "More than Moore" paradigm. This shift enables chiplet-based architectures that integrate logic, memory, and specialized functions within a single package, but also drives rapid increases in package size and complexity. AI and HPC applications demand extreme bandwidth, power, and compute density, relying on technologies such as HBM, 2.5D interposers, and 3D stacking. These advancements introduce significant challenges, including interconnect scaling, thermal management, power delivery, mechanical stress and warpage, yield management, and supply chain constraints. Addressing these issues requires close co-design across silicon, package, and system domains. This work presents an overview of heterogeneous integration and large-body packaging and outlines key technical and economic challenges as future "homework" for enabling scalable solutions in the post-Moore era.

Key words

Moore's Law, More than Moore, Heterogeneous Integration, Large body FCBGA, CoWoS (Chip on Wafer On Substrate), Substrate warpage management, Thermal management/heat dissipation, Supply chain resilience

I. Introduction

Advanced packaging has emerged as a primary driver of system performance and value, shifting the focus from transistor-level scaling to system-level integration. In this new paradigm, packaging enables heterogeneous integration of multiple dies, allowing continued performance scaling beyond the limits of traditional device scaling.

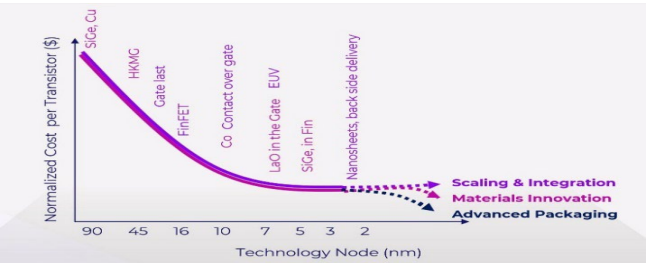


Fig. 1. *Moore's Law slow*

In response, the industry is transitioning toward heterogeneous integration, where multiple dies—including logic, memory, and specialized functions—are integrated within a single package. This "More than Moore" paradigm enables chiplet-based architectures that provide greater flexibility and improved cost efficiency compared to monolithic designs.

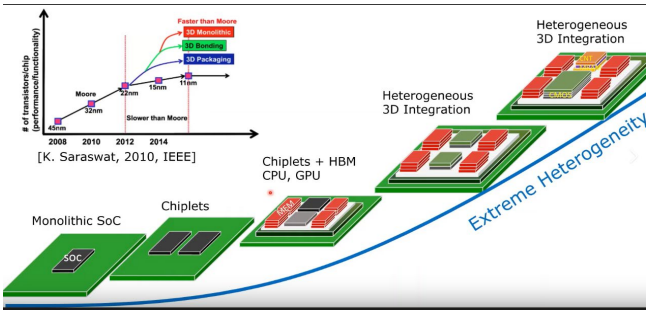


Fig. 2. *Extreme Heterogeneity.*

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A direct consequence of this trend is the rapid growth in package size and complexity. AI and HPC systems demand high compute density, memory bandwidth, and power delivery, driving the adoption of large-body packages with 2.5D interposers, 3D stacking, and multi-die integration. HBM enables TB/s bandwidth, while system power approaches the kilowatt scale. These advancements introduce challenges in interconnect density, signal integrity, thermal management, power delivery, mechanical stress and warpage, yield (KGD), and escalating cost. Heterogeneous integration is expected to accelerate, supported by hybrid bonding, co-packaged optics, and open die-to-die interfaces, requiring tight co-design across silicon, package, and system levels with strong ecosystem collaboration.

This work presents an overview of heterogeneous integration and large-body packaging, and identifies key technical gaps and industry priorities for sustainable scaling beyond Moore's law

II. General Takeaways for Heterogeneous Packaging

1. **Packaging Becomes the New Scaling Driver**
   As Moore's Law slows, system-level integration replaces transistor scaling as the primary innovation lever. Advanced packaging is now critical for performance, cost, and time-to-market, not just a backend process.

2. **Shift from Monolithic SoC to Chiplet Architecture**
   Large monolithic dies are no longer economically viable due to yield loss and escalating cost. Chiplet-based design enables modular integration, optimizing each function at the best process node.

3. **Heterogeneous Integration Enables System Optimization**
   Combines logic, memory (HBM), analog, and specialty dies within a single package. Enables performance scaling beyond reticle limits, especially for AI/HPC.
   Chiplet-bearing modules:

   a. Products without HBM
      Chips-last HDFO dominates current development and customer inquiries
      Bridge-based solutions for very large modules.
   b. Products with HBM
      Currently 2.5D TSV silicon interposers
      Trending Bridge-based solutions for > 4-5x reticle sized modules

4. **Large Package Size is Inevitable**
   Driven by: Extreme memory bandwidth (TB/s level) & High-power density (hundreds of watts to kW). Results in large-body FCBGA / interposer-based architectures

5. **Interconnect Becomes the New Bottleneck**
   Performance depends more on die-to-die communication than transistor speed. It requires:
   Ultra-fine pitch interconnect, High-density RDL / interposer, Signal & power integrity co-design

6. **Thermal and Mechanical Challenges Dominate**
   Key risks: Hotspot management in 3D/2.5D structures & warpage and stress in large substrates. Thermal and mechanical design become first-order constraints

7. **Yield Strategy Shifts to System-level**
   Yield is no longer wafer-only: KGD (Known Good Die) is mandatory. Multi-die integration increases compound yield risk. Packaging strategy directly impacts total system cost

8. **Cost Structure Shifts from Silicon to Packaging**
   Advanced packaging (interposer, HBM, substrate) can account for a significant portion of total cost. Cost-per-function optimization replaces cost-per-transistor

9. **Strong Ecosystem Dependency**
   Requires tight collaboration across: Foundry, OSAT Substrate suppliers, System companies. Co-optimization across the supply chain is essential.

III. Tireless Problem Solving

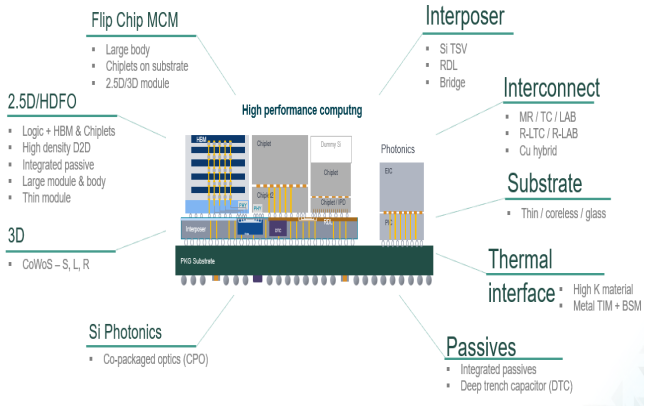


Fig. 3. *Technology Toolbox*

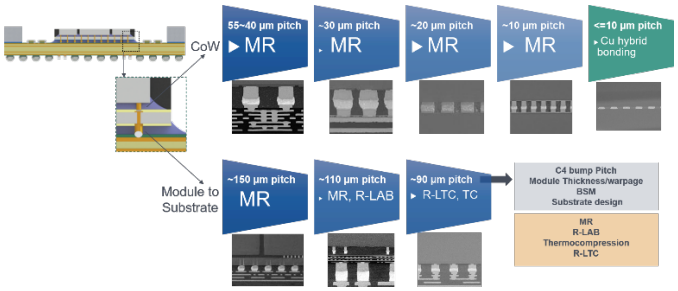
1. Bump Interconnection

Fig. 4 represents which bonding methodology emerged upon bump pitch getting finer. Equally important are advancements in interconnect technologies, where micro-bump scaling (MR/TC/LAB), advanced RDL processes, and copper hybrid bonding enable increasingly fine-pitch connections and improved signal integrity. These

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innovations are essential to sustain bandwidth scaling as the number of integrated dies increases.

Sidenote for R-LTC (Reverse Laser Thermal Compression), as integration evolves toward RDL-based (CoWoS-R) and hybrid structures, where mechanical compliance is higher but process sensitivity increases, the use of R-LTC becomes even more advantageous.



MR – Mass Reflow
R-LAB: Reverse-Laser Assist Bonding
TC: Thermal Compression

Fig. 4. *Bump Interconnect for Chiplets Module*

2. Wafer Grooving Perspective

The necessity of **picosecond** and **femtosecond laser grooving** for sub-5 nm wafers is driven by the fundamental mismatch between thermally induced damage from nanosecond processing and the extreme fragility of modern semiconductor materials. Ultrafast laser processes eliminate or minimize heat-affected zones, prevent microcrack formation, and preserve nanoscale structural integrity, which are essential for achieving acceptable yield and reliability in advanced nodes. Fig 4 showcases correlation between roughness and ramification to mechanical sawing blade as part of reasonability for Picosecond laser grooving.

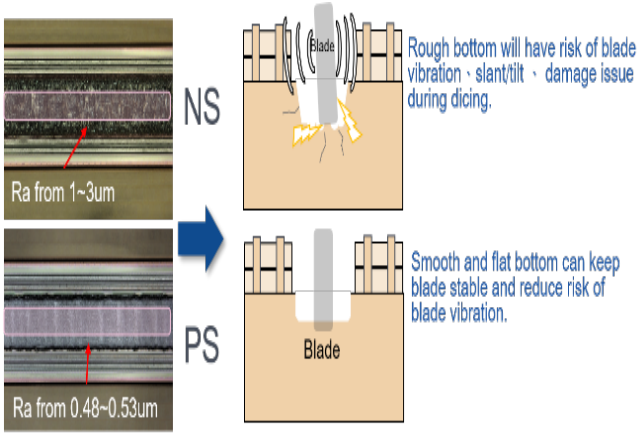


Fig. 5. *Nano vs Pico second after grooving*

Table 1 represents comparison of current nano vs advanced laser grooving.

Parameter	Nanosecond Laser	Picosecond	Femtosecond
Pulse duration	~10^{-9} s	~10^{-12} s	~10^{-15} s
Interaction mechanism	Thermal ablation	Mixed thermal/non-thermal	Athermal (cold ablation)
Heat-affected zone (HAZ)	Large (10–50 µm)	Moderate (2–5 µm)	Minimal (<1 µm)
Edge quality	Poor (chipping, recast)	Good	Excellent
Subsurface damage	Significant	Reduced	Negligible
ULK dielectric compatibility	Poor	Moderate	Excellent
Residual stress	High (tensile)	Reduced	Near-zero
Crack initiation risk	High	Moderate	Low
Throughput	High	High	Moderate
Cost	Low	Medium	High
Suitability for <5nm nodes	✕ Not suitable	☑ Baseline	☑ Best option

Table. 1. *Nano vs Pico/Femto second comparison*

3. Influencers for interposer wafer/module warpage

Material-Driven Warpage Mechanisms in CoW Structures: In CoWoS architecture, warpage is fundamentally governed by the interaction between structural stiffness and material CTE mismatch across multiple layers, including:

- Silicon interposer (low CTE, high modulus)
- RDL (Cu/polymer composite, moderate modulus)
- Organic substrate (high CTE, low modulus)
- Mold compound (EMC)
- Underfill (UF)
- Interconnect materials (solder, Cu pillar, hybrid bond)

At the CoW module level, the interposer stack and bonding materials dominate deformation behavior, while at the package level, mold compound, substrate, and backside metallization (BSM) further amplify or compensate for residual stress.

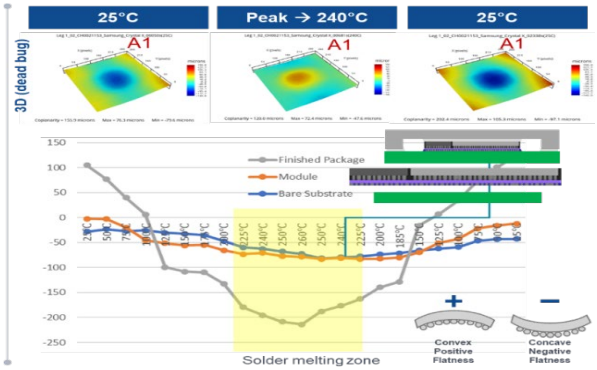


Fig. 6. *Example of compound warpage, 72 mm x 72 mm CoWoS-S*

Unlike conventional approaches, chiplet-based integration necessitates comprehensive warpage analysis across bare substrate, module, and package levels. This multi-hierarchical evaluation increases complexity and requires significantly longer development and qualification cycles. Refer to Fig 6, how to describe warpage variation over dynamic temperature in a single shot diagram.

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Even with simulation to prediction of module warpage, it remains homework how to make closer to hands-on warpage. Figure 6 shows an example of time-dependent behavior and prediction uncertainty after module mounting on a substrate and lid attachment for package warpage measurement.

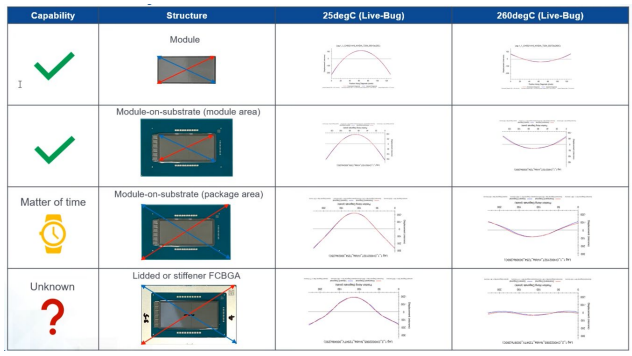


Fig. 7. *Warpage simulation limitation, (example of 4L RDL interposer module size 53 mm x 92 mm)*

Unlike conventional FCBGA, warpage evaluation of CoW (Chip-on-Wafer) structures is fundamentally different in CoWoS packaging (see Fig. 9).

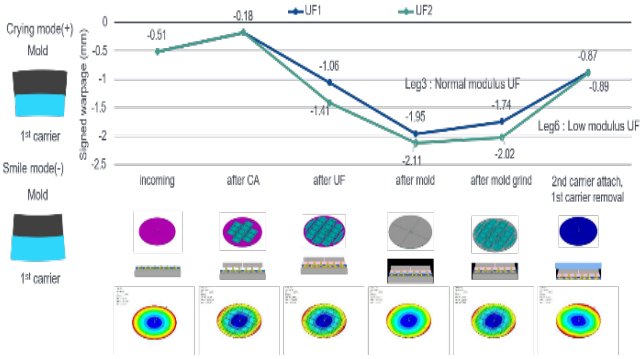


Fig. 8. *Example of Wafer warpage analysis before wafer sawing. (4L RDL, module size 64 mm x 40 mm on 12-inch wafer)*

4. Thermal Solution with TIM1 (Package Level)

The selection of TIM (Thermal Interface Material) is therefore a key design variable that directly impacts not only thermal performance but also mechanical reliability and package-level warpage. TIMs can be broadly categorized into metal-based, composite, and polymer-based materials, each representing a distinct trade-off between thermal conductivity, mechanical compliance, and process complexity.

Table. 2 illustrates CONS/PROS between performance and cost.

Category	Metal TIM (e.g., Liquid metal, solder, sintered Ag)	Composite TIM (filled polymer)	Polymer TIM (grease, pad)
Thermal Conductivity	30–200+ W/m·K	3–20 W/m·K	1–5 W/m·K
Thermal Resistance	Lowest	Medium	Highest
Reliability (long-term)	Medium (oxidation, pump-out risk)	Good	Fair
Mechanical Compliance	Low (stiff)	Medium	High (soft)
Warpage / Stress Impact	High (adds stress)	Medium	Low (stress absorber)
Process Complexity	High (handling, oxidation control)	Medium	Low
Cost	High	Medium	Low
Reworkability	Poor	Moderate	Good
Application Fit	HPC / >500W / AI	High-end packaging	General / mid-power

Table. 2. *Performance/cost comparison for TIM types*

OSAT-driven solutions focus on minimizing thermal resistance through the stack, including TIM1 (die-to-lid interface), interposer/substrate thermal paths, and underfill/mold compound optimization. However, as module power levels exceed hundreds of watts and approach kilowatt-class regimes, these package-level optimizations alone are insufficient. The effectiveness of heat removal becomes strongly dependent on system-level thermal interfaces and cooling architecture, where TIM2 (lid-to-heat spreader or lid-to-cooling solution interface) plays a critical role. One-line message for thermal message is “Thermal solution = Package (OSAT) + System (TIM2 + cooling) → must be co-designed”

5. Low CTE Core Evaluation with Multiple Glasses

The global shortage of low-CTE glass (T-glass) is primarily attributed to its highly concentrated supply base, limited to a small number of qualified manufacturers, combined with rapidly accelerating demand from AI-driven heterogeneous integration. The situation is further exacerbated by the intrinsic complexity of T-glass fabrication and the long lead time required for capacity expansion. Glass is contracted in CCL (Copper Clad Laminate) structure. See figure 5.

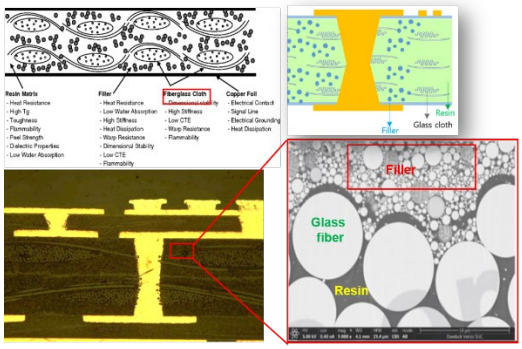


Fig. 9. *CCL structure*

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Historically, OSATs had limited visibility into the sourcing of low-CTE glass (T-glass), as supply was largely confined to Japan within the CCL ecosystem, and geographic concentration was not viewed as a major risk. However, with ongoing shortages and recent capacity expansion into Taiwan and China, OSATs must now account for material variability across sources. Differences in CTE and material properties directly affect substrate and package warpage, with impacts amplified by larger die sizes and module scaling. As a result, additional characterization—covering warpage, die attach interactions, and material compatibility—is required, increasing engineering complexity, reliability risk, and qualification time.

6. Lage Body/Heterogenous Package Beyond 120 mm x 120 mm

This section focuses on infrastructure considerations beyond package warpage concerns. The transition to large-body heterogeneous packages requires not only advances in materials and design, but also a fundamental reconfiguration of handling infrastructure and process carriers. Substrate panels, trays, and matrix boats must be co-optimized with package architecture to maintain mechanical integrity and process uniformity."

6.1. Substrate Panel Scaling

The transition to larger package bodies necessitates the use of larger substrate panels, which introduce several difficulties:

- Increased warpage sensitivity due to larger dimensions
- Reduced mechanical rigidity, particularly for thin or coreless substrates
- Handling challenges during:
  - lamination
  - bonding
  - singulation

6.2. Tray (Carrier) Design Limitations

Current JDEDC A tray (322.6 mm x 136.0 mm) cannot exceed 120 mm on dimension Y. 120 mm x 150 mm thetically deems as max body size and allocable max 2 units a tray.



Fig. 10. *JEDEC A tray size*

6.3. Assembly Perspective

6.3.1 Matrix boats used in assembly processes (e.g., reflow for die attach and ball attach and curing after Underfill) must also be adapted as it becomes enlarger.

- Challenge: Larger modules increase causes to gravitational sagging, thermal expansion mismatch between boat and package, and non-uniform heating across large footprints
- Implications: Die shift and misalignment. Non-uniform bonding quality, and Yield degradation.
- Required Improvements: Low-CTE, high-stiffness materials for matrix boats and enhanced thermal uniformity design (zoning, airflow control)

6.3.2. Existing OSAT equipment is typically designed for standard package sizes, leading to: Mechanical size constraints (handling arms, chucks, alignment tools), Limited process windows for bonding pressure distribution and thermal uniformity. Actions to be taken:

- Equipment redesign or upgrade
- Expanded process margin development

IV. Conclusion

The continued evolution of heterogeneous integration and chiplet architecture is driving unprecedented demands on semiconductor packaging technologies. As interconnect pitch scales below conventional micro-bump limits, advanced bonding solutions such as R-LTC, fine-pitch RDL, and copper hybrid bonding become critical enablers for achieving higher bandwidth, increased I/O density, and improved electrical performance. Simultaneously, ultrafast laser-roving technologies are emerging as essential processes for preserving yield and reliability in advanced-node wafers.

Beyond interconnection challenges, package scalability is increasingly constrained by warpage behavior across wafer, module, and package levels, requiring comprehensive multi-physics optimization of materials, structures, and assembly processes. Thermal performance has likewise become a system-level challenge, where successful heat dissipation depends on the co-design of package technologies, TIM solutions, and cooling architectures. Furthermore, material supply constraints, particularly for low-CTE glass substrates, and growing infrastructure limitations associated with package sizes beyond 120 mm × 120 mm introduce new risks in manufacturing scalability.

Future advancements in AI and HPC systems will therefore depend not only on continued innovations in package architecture, but also on the holistic optimization of interconnect, materials, thermal management, warpage control, and manufacturing infrastructure across the entire semiconductor packaging ecosystem.

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