Copper Pillar Patterning Using Digital Exposure Technology with Dry Film Resists for 2.5D PLP

Ksenija Varga[1], Lisa Berger[1], Tobias Zenger[1], Hajime Furutani[2], Masayuki Kishino[2]
EV Group, St. Florian am Inn, Austria
Asahi Kasei Corporation, Shizuoka, Japan
K.Varga@EVGroup.com; furutani.hc@om.asahi-kasei.co.jp

Abstract

Fan-out panel-level packaging (FO-PLP) is a growing segment in heterogeneous integration, gaining importance as a cost-efficient solution for advanced packaging. Panel formats of 310×310 mm² demonstrate technical advantages over wafer substrates while avoiding the process complexities associated with larger panel sizes.

In this work, a novel dry film resist (DFR) was patterned using digital exposure lithography for high aspect ratio (high A.R.) Copper pillar (Cu pillar) application. CD uniformity confirmed a deviation within ±4.00%. Patterning of both, round and square via geometries proving straight side wall profiles with a VIA and L/S resolution of 30 µm was demonstrated in 120 µm-thick DFR.

Subsequent electroplating and resist stripping enabled the successful fabrication of Cu pillars with A.R. of 1:3 and 1:4, respectively. In addition, newly developed equipment software features effectively addressed the challenges associated with 2.5D and 3D integration, supporting the requirements of next-gen AI and HPC devices.

Key words

2.5D packaging, heterogenous integration, digital exposure technology, copper pillars, dry film resist

I. Introduction

As semiconductor devices advance toward higher I/O density and performance driven by AI and HPC applications, continued innovation in equipment, materials, process integration, and packaging design is essential. In parallel with achieving stringent technical specifications, yield improvement and cost reduction – relative to established processes of record – remain critical. Accelerated R&D cycles and shortened tape-out timelines further necessitate flexible, scalable manufacturing solutions [1].

In the context of 3D integration, high-throughput digital lithography is a key enabler for fine-pitch interconnect formation, supported by advanced hardware, adaptable software platforms, advanced process control, and optimized patterning performance. This technology must address increasingly complex surface topography while enabling seamless scalability [2].

Recent publications have demonstrated the critical role of 2.5D packaging development and optimization. It was reported that large-size 2.5D packages with organic RDL interposers represent promising technology for next-gen AI processor applications due to their high integration density, scalability, excellent signal and power integrity, and cost effectiveness [3].

The significance of advanced packaging where multiple chips are integrated into a single package is growing as conventional transistor scaling in semiconductor devices reaches its limits.

As a result, technologies such as Package on Package (PoP), silicon bridge interposers, and vertically stacked DRAM are gaining prominence. In these approaches, Cu pillars play a key role in enabling vertical interconnections, as illustrated in Figure 1.

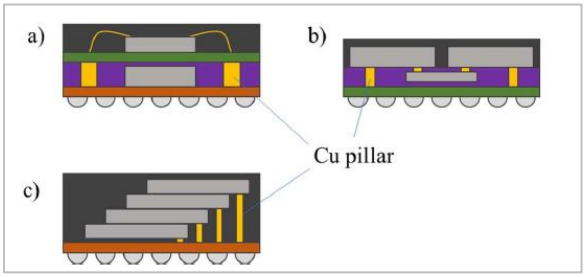


Figure 1: Advanced packaging technology using Cu pillars: (a) PoP, (b) Si bridge embedded interposer and (c) vertically stacked DRAMs [2].

For such applications, high A.R. Cu pillars are essential to

achieve improved integration density and play a role in enhancing device heat dissipation.

Recent progress in materials engineering has positioned dry film photoresists as an important contributor to yield enhancement in both wafer-level and panel-level packaging [4].

In the present paper, the digital patterning of the newly developed high thickness DFR for 2.5D packaging was evaluated.

As a substrate, the panel dimensions 310×310mm^2 was used in this investigation. By scaling from round substrates 300mm to panel size, there is significant advantage in yield improvement when using the complex die packages, as illustrated in Figure 2.

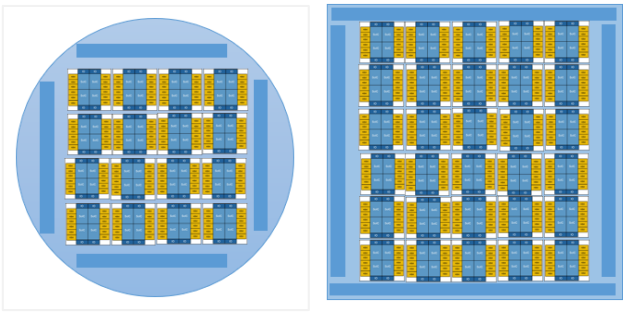


Figure 2: Left – 16 packages on round substrates; Right – 30 packages on square substrate

II. Experimental

A. Digital Exposure Technology

Digital lithography has experienced transformation through the integration of advanced software and hardware technologies. These developments allow for the direct exposure of resist and dielectric materials from layout data files, eliminating the need for reticles. This shift offers exceptional flexibility in material processing.

A key advantage of "digital nature" is its ability to adjust layout data in real time. This enables configuration modifications that can compensate for substrate distortions arising from pre-processing steps such as thermal treatments and mechanical stresses, ensuring high pattern fidelity and improved yield in advanced packaging [2].

B. DFR Processing

The process conditions were systematically optimized to define the appropriate focus, exposure dose, and wavelength matrix for the dry film resist patterning.

The objective of this study was to achieve electroplated Cu pillars with A.R. in the range of 1:3 to 1:4. The lithography, development, stripping, and electroplating parameters are summarized in Table 1.

In parallel with the evaluations on square glass panel substrates, equivalent processes were established for 300 mm Si and glass wafers using the same material.

Table 1: Processing Conditions

Process	Materials / Parameters
Dry Film Roll Laminator 70 °C	CX-series, 120 µm Film Thickness
Substrates	Panel: 310×310mm^2, glass Panel: 300×300mm^2 Cu–sputtered, glass (Mitsui–Kinzoku HRDP) Wafer: 150mm Cu-sputtered, Si
Digital Exposure Parameters	Wafer: Wavelengths 375nm, 405nm 150–300 mJ/cm^2; Focus range –30 to –80 µm Panels: Wavelengths 375nm, 405nm Dose range 100–250 mJ/cm^2; Focus –30 to –80 µm
Development EVG120	Wafer: 20 °C; combined puddle and spray Panel: 20 °C; immersion bath (1% Na_2CO_3).
Descum	O_2 plasma
Plating	SC–50 (MacDermid), 25 °C, 5 ASD
Stripping	SPR-920 (KANTO-PPC Inc.), 75 °C

II. Results and Discussion

The characterization approach included CD uniformity measurements, optical macro- and microscopic assessments, and SEM cross-sectional analysis of the patterned dry resist structures and the resulting Cu pillars.

A. Critical Dimension Uniformity on Glass Panel

CD uniformity was evaluated using vertical 37 µm line/space (L/S) features incorporated within an L-shaped CD target structure (Fig. 4), featuring equal line and space dimensions. Measurements taken from representative points across the substrate were interpolated to construct a continuous CDU distribution map. The relative CDU, determined using Michelson contrast, was ±4.00%, and values remained consistently below 150 nm across all inspected wafer edge locations (measured using the EVG®40NT).

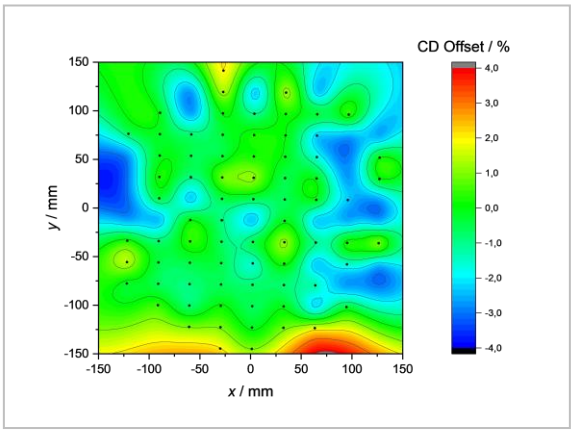


Figure 3: CDU contour plot for the 300×300 mm² panel, derived

using the measurement and analysis workflow described above

B. SEM Images on DFR Lithography Patterns

Figure 4 represent cross-sectional SEM images of the patterned DFR structures corresponding to a 30 µm layout design. As observed, both the square via array and the line/space (L/S) patterns exhibit well-defined, nearly vertical sidewall profiles (~88°) at a film thickness of 120 µm, indicating strong anisotropic pattern transfer and effective process control.

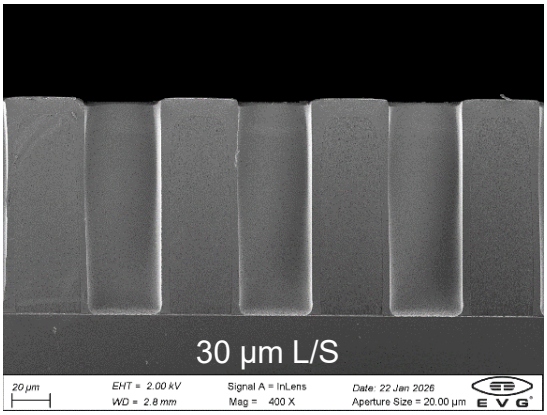


Figure 4: Cross–section image of 30µm L/S pattern

C. SEM Tilted View Images of Cu Pillars

As outlined in the process flow, the DFR structures first underwent an O_2 plasma descum treatment, followed by electrolytic copper plating and subsequent DFR removal under the conditions specified in Table 1. Tilted view SEM images of the resulting Cu pillars are presented in Figures 5–6. Copper pillars with a height of 110 µm were successfully fabricated, exhibiting straight sidewall profiles. No defects such as voids, residual DFR, or pillar collapse are observed.

These findings confirm that digital lithography facilitates not only accurate resist patterning but also the production of high A.R. Cu pillars, underscoring its strong potential for panel-level advanced packaging applications.

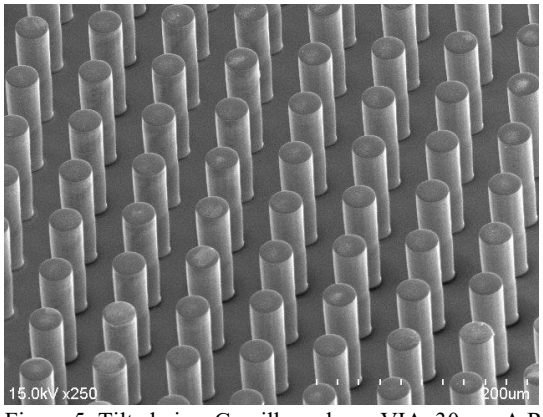


Figure 5: Tilted view Cu pillars, dense VIA, 30µm, A.R. 1:4

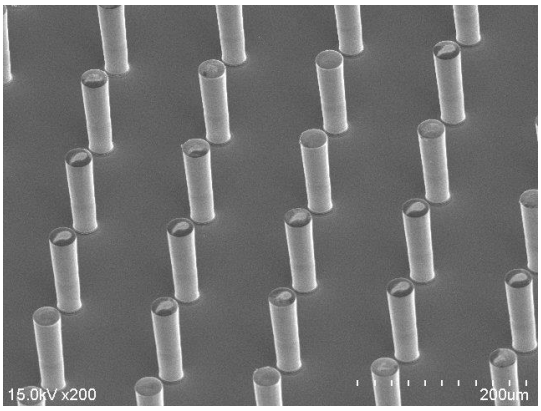


Figure 6: Tilted view Cu pillars, isolated VIA, 30µm, A.R. 1:4

III. Conclusions and Outlook

This study presents the results of investigations of digital exposure of DFR for both wafer- and panel-level applications. Digital patterning of various VIA and L/S designs using novel DFR materials demonstrated reliable resolution of features down to 30 µm at a film thickness of 120 µm.

Key system capabilities including real-time autofocus, extended depth of focus, dynamic distortion compensation, and comprehensive process control—confirm the suitability of the exposure platform for Cu pillar fabrication, enabling high-aspect-ratio structures (up to 1:4) on 310×310 mm² glass substrates.

The flexible digital lithography platform represents a high-throughput exposure solution specifically designed to meet the complex patterning requirements of advanced semiconductor packaging. Its integrated hardware–software architecture has been systematically developed to achieve the high levels of performance, stability, and process integration demanded by advanced packaging technologies.

Overall, these developments establish a new benchmark in digital patterning performance, supporting both 2.5D integration and 3D heterogeneous stacking.

The demonstrated capabilities highlight the high throughput LITHOSCALE® XT platform as a key enabler for addressing the patterning and integration challenges of next-gen AI and HPC device integration.

In the future work, the focus will be placed on DFR of thickness >300µm achieving Cu pillars with A.R. 1:7 for HBM applications.

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