Improving HDI Substrate Reliability by Suppressing Void Growth in Electroless Cu Plating at Microvia Bottoms

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Abstract
High-density interconnect (HDI) packaging substrates rely on stacked microvias for vertical electrical connection between build-up layers. However, the microvia bottom remains a critical reliability weak point during field use because repeated temperature variations can promote crack initiation near the electroless Cu plating layer. Voids formed in the electroless Cu layer have been suspected to contribute to weak-microvia failure, but the connection between void-growth mechanism, plating process control, and substrate-level reliability evaluation has not been fully clarified.

This paper integrates two related studies on electroless Cu voiding and HDI substrate reliability. First, based on our previous mechanistic study, model multilayer Cu structures simulating the microvia-bottom region were prepared, and the effects of Ni concentration and bath temperature on electroless plating rate and void formation were investigated. TEM observation and quantitative image analysis showed that the largest voids and highest void fractions were formed in the initial deposition region. These results indicate that void growth is strongly governed by the initial plating stage, where Pd catalyst sites remain exposed and locally enhance the electroless Cu reaction and hydrogen generation. Under higher initial plating-rate conditions, hydrogen bubbles are more readily retained and coalesced, resulting in larger voids.

Second, HDI substrates with identical designs but different electroless Cu voiding levels at the microvia bottoms were evaluated by thermal cycling tests (TCTs). The substrate with higher voiding exhibited lower reliability when the upper temperature (T_{high}) of thermal cycling was near but below the glass transition temperature, T_g, of the insulation film. However, when T_{high} exceeded T_g, the reliability difference between substrates became less distinguishable. These results indicate that suppressing the initial electroless Cu plating rate is an effective process guideline for reducing void formation and improving microvia reliability. They also show that reliability test conditions must be selected carefully with respect to insulation film T_g because excessively severe thermal cycling can obscure differences in interconnection quality.

Key words
Electroless Cu plating, HDI substrate, Initial plating rate, Microvia reliability, Thermal cycling test, Void formation

I. Introduction
The demand for compact, multifunctional, and high-performance electronic devices has accelerated the development of HDI packaging substrates. In these substrates, microvias provide vertical electrical interconnections between build-up layers and are essential for achieving high wiring density [1]. As microvia dimensions continue to decrease, the cross-sectional Cu area supporting the interconnection becomes smaller. Therefore, local defects that were previously less critical, such as nanovoids in the plated Cu structure, can have a larger influence on mechanical strength and long-term reliability.

A typical microvia fabrication process includes drilling, desmear and surface cleaning, Pd catalyst activation, electroless Cu plating, and subsequent electrolytic Cu filling. The electroless Cu layer acts as a conductive seed layer for electrolytic Cu deposition. However, this layer is also known to be a weak region in microvia structures. Cracks that cause

electrical failure frequently initiate at or near the electroless Cu layer at the microvia bottom. This failure is widely recognized as the weak-microvia issue [2][3][4].

During electroless Cu deposition, hydrogen is generated as a reaction byproduct. Part of this hydrogen can be trapped in the growing Cu deposit and become incorporated as voids. These voids reduce the effective metallic cross section and may also act as crack-initiation or crack-propagation sites during thermal cycling [5][6][7]. Therefore, reducing void formation in the electroless Cu layer is important for improving HDI substrate reliability.

In our previous work, a model Cu multilayer structure was used to clarify the void-growth mechanism in electroless Cu plating. The results showed that voids preferentially grew in the initial deposition region and that the initial plating rate strongly affected both void fraction and maximum void size [8]. These findings identify the initial electroless Cu deposition stage as a key process window for suppressing void formation and improving microvia integrity.

TCTs are commonly used to evaluate microvia reliability. In many cases, higher test temperatures are considered to provide stronger acceleration. However, in organic packaging substrates, the thermomechanical response of the insulation film changes significantly near its glass transition temperature, T_g. When T_{high} of the TCT exceeds T_g, the dominant deformation and failure behavior of the substrate may change. Under such conditions, the test may no longer clearly distinguish reliability differences caused by interconnection quality.

This study integrates two related findings to provide a practical guideline for improving HDI substrate reliability. First, void growth in electroless Cu plating is governed mainly by the initial deposition stage, before Pd catalyst sites are fully covered by deposited Cu. Second, substrate-level reliability evaluation shows that differences in electroless Cu voiding can affect microvia reliability, but that the sensitivity of the reliability test depends strongly on T_{high} of TCT relative to the insulation film T_g. Therefore, this paper focuses on the connection between process control and reliability evaluation: suppressing void formation by controlling the initial electroless Cu plating rate, and selecting T_g-aware TCT conditions to correctly reveal interconnection reliability differences.

II. Experimental

A. Model Cu structure for analyzing void-growth mechanism

The detailed preparation procedure and image-analysis method for the model Cu multilayer samples have been reported previously [8]. In brief, an electrolytic Cu/electroless Cu/electrolytic Cu structure was fabricated to simulate the microvia-bottom region. In this structure, the electroless Cu layer was located between the underlying electrolytic Cu layer, corresponding to the Cu pad, and the upper electrolytic Cu layer, corresponding to the subsequent Cu filling.

After surface cleaning and Pd catalyst activation, electroless Cu plating was performed using a non-cyanide bath. To investigate the effect of plating conditions, Ni concentration and bath temperature were varied independently while keeping the other bath constituents and process conditions constant. The standard condition was defined as Ni 100% at 27 °C. Additional Ni levels of Ni 50% and Ni 200% were used to examine the effect of Ni concentration. Bath temperatures of 22, 27, 32, and 37 °C were used to examine the effect of plating bath temperature.

The electroless Cu thickness was controlled to approximately 300 nm for all conditions by adjusting the plating duration based on preliminary plating-rate measurements. After electroless Cu deposition, a final electrolytic Cu layer was deposited to complete the multilayer structure. Cross-sectional samples were prepared, and the electroless Cu layers were observed by transmission electron microscopy. Void fraction and maximum void size were quantified by image analysis. To evaluate the location dependence of void formation, the electroless Cu layer was divided into three regions: the initial deposition region near the Cu pad, the middle region, and the upper region.

B. HDI substrate samples for reliability evaluation

To connect electroless Cu voiding to actual substrate reliability, two types of HDI packaging substrates were prepared. The two substrates had identical design, material structure, and circuit layout, but different electroless Cu plating processes were used at the microvia bottoms to intentionally create different voiding levels.

The substrates measured 45 mm × 45 mm and contained daisy-chain circuits and external pad regions. The microvia structure consisted of three-layer stacked microvias on both sides of the prepared substrates. The electroless Cu process used for selected microvia layers was varied so that Substrate A contained higher voiding at the microvia bottoms, while Substrate B contained lower voiding. The second microvia layer was prepared using a common intermediate process in both substrates. This sample design allowed the influence of electroless Cu voiding to be evaluated independently because the substrate design and constituent materials were kept identical.

FE-SEM cross-sectional observation of the electroless Cu layers confirmed the difference in voiding level between the substrates. Substrate A showed higher voiding, whereas Substrate B showed lower voiding. Therefore, Substrate A was expected to show lower microvia reliability than Substrate B if voiding contributes to failure.

C. TCT and failure analysis

TCTs were performed between -55 °C and three different upper temperatures, T_{high}: 125, 150, and 175 °C. Each cycle included a 15 min dwell at the low temperature and a 15 min dwell at the upper temperature. These T_{high} values were selected with respect to the T_g of the insulation film, approximately 153 °C. Thus, 125 °C represents a condition well below T_g, 150 °C represents a condition slightly under T_g, and 175 °C represents a condition above T_g.

Electrical resistance was monitored during thermal cycling. A circuit was defined as failed when its resistance exceeded twice the initial value. After TCT, selected failed circuits were analyzed by electrical continuity measurement and cross-sectional observation to identify the failure location. This procedure was used to determine whether failures occurred in the daisy-chain regions or pad regions and whether cracks were associated with the electroless Cu plating layers at the microvia bottoms.

III. Results and Discussion

A. Initial plating rate controls void growth in electroless Cu plating

The model Cu experiments showed that both Ni concentration and bath temperature affected the electroless Cu plating rate. Higher Ni concentration and higher bath temperature generally increased the plating rate. TEM observation further showed that the void fraction and maximum void size increased under higher plating-rate conditions.

A particularly important result was the location dependence of void formation. The largest voids and highest void fractions were consistently observed in the initial deposition region near the Cu pad. In contrast, the middle and upper regions showed lower voiding, even though the plating rate during later deposition stages was not always lower. This indicates that the initial stage of electroless Cu deposition has a special role in void growth.

This behavior can be explained by the presence of Pd catalyst sites at the initial surface, as schematically illustrated in Figure 1(a). At the beginning of electroless deposition, Pd catalyst particles remain exposed and locally promote the electroless Cu reaction. Because hydrogen is generated as a byproduct of this reaction, local hydrogen generation is enhanced around the catalyst-rich surface. Under a lower initial plating-rate condition, the accumulated bubbles remain relatively small, resulting in smaller voids in the initial deposit. Under a higher initial plating-rate condition, larger hydrogen bubbles can accumulate near the exposed Pd catalyst sites and become incorporated as larger voids.

As shown in Figure 1(b), once the Pd-rich initial surface becomes buried by deposited Cu, the, the influence of the catalyst sites decreases, and the reaction surface becomes smoother and more uniform. Hydrogen bubbles are then more spatially separated and less likely to coalesce. In addition, the increased deposition rate during the later stage can encapsulate small bubbles before they coalesce and grow into larger voids. Therefore, large voids were less likely to develop in the middle and upper regions, even when the plating rate during later deposition was relatively high.

These results identify the initial deposition stage as the key process window for void suppression. In practical terms, reducing the initial electroless Cu plating rate before the Pd catalyst-rich surface is fully covered is an effective approach

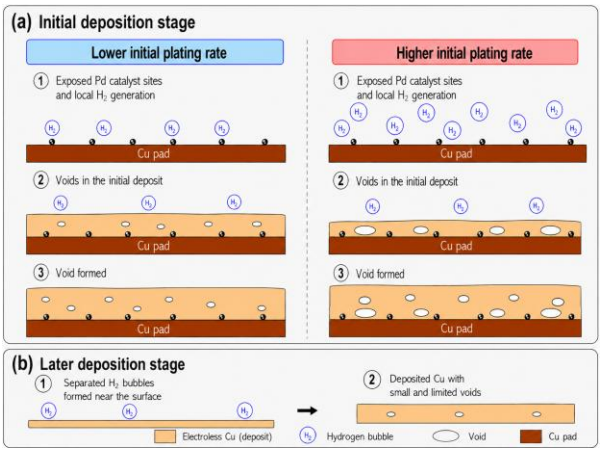

Figure 1 Void-formation mechanism during the initial and later stages of electroless Cu deposition.

for suppressing large void formation at the microvia bottom.

B. Higher electroless Cu voiding decreases HDI substrate reliability

The reliability evaluation using actual HDI substrates indicated that electroless Cu voiding is not only a local microstructural issue but also affects substrate-level reliability. Substrate A, which had higher voiding at selected microvia-bottom layers, showed lower reliability than Substrate B under an appropriate thermal cycling condition. In particular, when TCT was performed with T_{high} = 150 °C, slightly under the insulation film T_g, the reliability difference between the two substrates was clearly observed. Substrate B, with lower voiding, maintained higher reliability than Substrate A.

Failure analysis supported this relationship. Electrical discontinuities were detected in pad regions, and cross-sectional observation revealed cracks near the electroless Cu plating layers in failed microvias. These observations indicate that void-rich electroless Cu layers are more susceptible to crack initiation and propagation under cyclic thermal stress, leading to reliability degradation at earlier cycle numbers.

These reliability results indicate that reducing void formation in the electroless Cu layer is important for enhancing microvia interconnection reliability. From this viewpoint, the void-growth mechanism discussed in Section III-A provides a process guideline for void suppression. Because large voids preferentially form during the initial electroless Cu deposition stage, controlling the initial plating rate before the Pd catalyst-rich surface is fully covered is expected to reduce void formation at the microvia bottom. This process control can help improve the mechanical integrity of the electroless Cu layer and enhance the reliability of HDI substrate interconnections.

C. Tg-aware TCT conditions are necessary for revealing interconnection reliability differences

The TCT results also showed that the ability to distinguish the reliability difference between the high-voiding and low-voiding substrates depends strongly on the selected T_{high}. Figure 2 summarizes the cumulative failure-rate behavior of Substrate A and B at each Thigh relative to the insulation film glass transition temperature, Tg.

At T_{high} = 125 °C, which is well below T_g, no failure was observed in either substrate even after prolonged thermal cycling, as shown in the left panel of Figure 2. This indicates that the thermal stress generated under this condition was therefore too mild to induce interconnection failure.

At T_{high} = 150 °C, which is near but below T_g, the cumulative failure rate curves of the substrates were clearly separated. Substrate A, which contained higher electroless Cu voiding, began to fail at fewer cycles and exhibited a higher cumulative failure rate than Substrate B. IN contrast, Substrate B, which contained lower voiding, maintained higher reliability over a greater number of cycles. This condition therefore provided sufficient thermal stress to reveal the influence of microvia interconnection quality while preserving sensitivity to the difference in electroless Cu voiding. As indicated in the center panel of Figure 2, T_{high} = 150 °C provided good reliability differentiation.

In contrast, at T_{high} = 175 °C, which is above T_g, both substrates failed rapidly and at similar cycle numbers, as shown in the right panel of Figure 2. Under this condition, the reliability difference associated with interconnection quality became less distinguishable. This suggests that once the test temperature exceeds T_g, the thermomechanical response of the insulation film changes significantly. The resulting deformation and stress state may become dominated by the substrate material system rather than by the local interconnection quality. As a result, an overly severe TCT condition may obscure the true influence of microvia interconnection quality.

This finding is important for reliability test design. Higher test temperature does not always provide better information. For evaluating process-related differences such as electroless Cu voiding, TCT should be selected not only for acceleration but also for sensitivity to the intended failure mechanism. In HDI substrates using organic insulation films, T_{high} near but below T_g may be more suitable than T_{high} above T_g for distinguishing interconnection reliability differences.

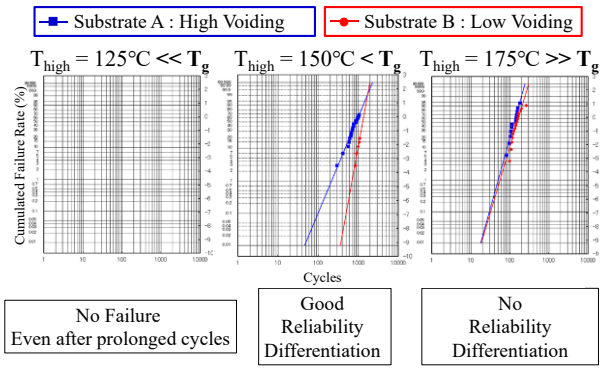

Figure2 Schematic summary of TCT sensitivity relative to the insulation-film glass transition temperature, T_g

IV. Summary

This paper connected electroless Cu void-growth behavior with HDI substrate reliability and reliability test design. The main conclusions are as follows.

1. Voids in electroless Cu plating layers mainly grew during the initial deposition stage, where Pd catalyst sites remained exposed.
2. Higher initial electroless Cu plating rate increased the void fraction and maximum void size. Therefore, controlling the initial plating rate before Pd catalyst coverage is an effective process guideline for suppressing void formation.
3. HDI substrates with higher electroless Cu voiding at the microvia bottoms exhibited lower reliability than substrates with lower voiding when evaluated under suitable thermal cycling conditions.
4. TCT conditions must be selected with respect to the insulation film T_g. A condition near but below T_g clearly distinguished the reliability difference caused by voiding, whereas a condition above Tg caused rapid failure in both substrates and obscure the interconnection-related difference.
5. These results indicate that improving HDI substrate reliability requires both manufacturing control of the initial electroless Cu plating process and T_g-aware reliability test design that can properly reveal interconnection reliability, as summarized in Figure 3.

Acknowledgment

This work was supported by the Japan Society for the Promotion of Science (JSPS) through the “Grant-in-Aid for JSPS Fellows” (Grant Number 25KJ1804), and by the Ministry of Education, Culture, Sports, Science and

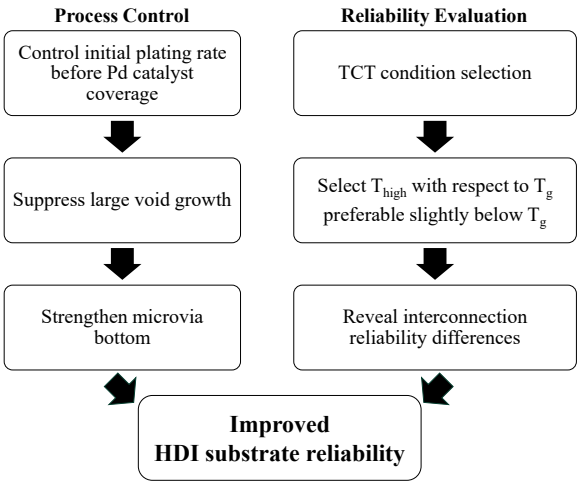

Figure 3 Integrated guideline for improving HDI substrate reliability.

Technology (MEXT), Japan through the "Crossover Alliance to Create the Future with People, Intelligence and Materials" (Grant Number 2024Y006). We gratefully acknowledge the technical support provided by the Comprehensive Analysis Center, SANKEN, The University of Osaka.

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