Accelerating Advanced Packaging and Interposer Design with AI-Based 3D Full-Wave Optimization

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***Abstract*— The rapid evolution of microelectronic technologies has led to increasingly compact, high density package designs that must accommodate for multiple high-speed die-to-die interconnects. With modern high-speed package deigns becoming increasingly complex, this presents a significant challenge in achieving the optimal path planning to maintain routing and signal integrity. This paper explores an advanced methodology of how Artificial Intelligence (AI) is being leveraged to help evaluate the best tradeoffs more efficiently. The approach enables designers to optimize inter-die connections in heterogenous multi-die packages, mitigating insertion loss, ensuring impedance matching, and reducing cross talk.**

Keywords—Signal Integrity, Optimality Intelligent System Explorer, Universal Chiplet Interconnect Express, Cadence Design Systems, Clarity 3D FEM, Interposers, Semiconductors, Topology Workbench, Artificial Intelligence (AI), Machine Learning (ML), SystemSI, Die-to-die interconnect.

I. Introduction

The increasing complexity and evolution of semiconductors technologies have resulted in increasingly complex advanced packages. The Semiconductor industry is rapidly transitioning toward heterogenous integration, where multiple chiplets are combined in advanced packaging to deliver higher performance and increased functionality. These designs must accommodate high-density interconnects while maintaining strict performance targets driving new challenges in routing, signal integrity, and even simulation times. Traditional methodologies struggle to keep pace with this level of complexity, creating the urgent need for a more intelligent and automated approach.

This paper presents a AI based methodology to improve performance times in simulation. The paper begins by establishing industry context, highlighting UCIe as the emerging interface standard for die-to-die communication on interposer-based designs. Next traditional methods and the limitations of current design practices will be outlined. It then introduces a new AI/ML-driven methodology to address these challenges. Finally simulation results using this methodology will be presented and analyzed.

II. Ease of Use

UCIe has emerged as the industry standard for die-to-die communication and has enabled the next generation of semiconductor design by addressing scaling challenges [1]. Instead of solely relying on transistor scaling, UCIe extends Moore's Law, so that system performance and complexity can now be increased at the package level. It enables the ability of multiple package dies from various sources to coexist into one board, however the strict requirements imposed by UCIe also increases design challenges. Concerns include functional reliability and quality, which necessitates ongoing research and developments in ensuring dependable high-speed interconnects between chiplets [2]. Fig.1 shows standard and advanced packaging 2D and 2.5D scenarios.

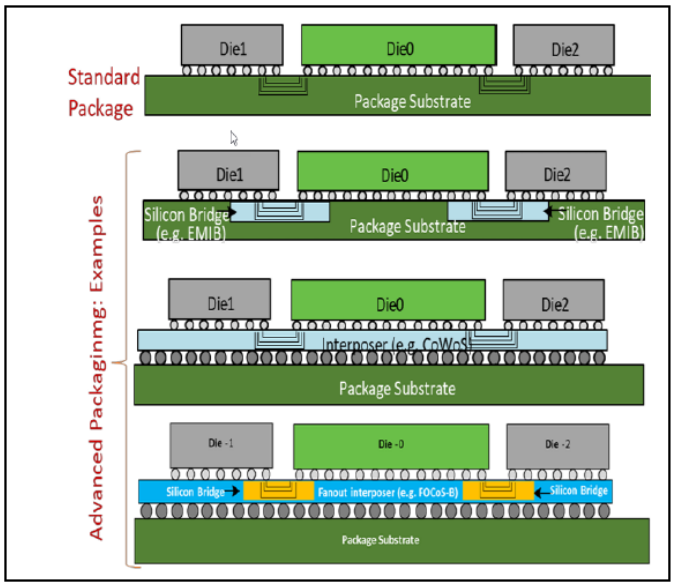

Fig. 1. Multi-Die Advanced Package Module

III. Traditional Methods

With advances in electronic design automation (EDA), package design workflows remain heavily reliant on manual iteration. To achieve compliance with performance targets and industry standards, the design of high-speed interconnects often requires multiple cycles of manual routing, simulation, analysis, and redesign. Each iteration is computationally expensive and time-consuming. For complex multi-die systems, this process may take weeks, and engineers often find themselves repeating this cycle. One challenge lies in the design of via-structures used to transition high-speed signals across layers of an interposer. Vias that have not been optimized create

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impedance mismatches, which directly result in ringing, reflections, and insertion loss. This causes the overall signal integrity to degrade which can compromise eye diagrams and timing margins. Even when simulation results are acceptable, engineers must ensure compliance with strict interface standards. This methodology relies heavily on engineer expertise and there is no guarantee the optimal solution can be found within the available time limit. This manual approach not only extends development time but also increases the risk of overlooking optimal design tradeoffs. While traditional methods can eventually achieve compliance, they do so at the expense of speed, scalability, and consistency.

IV. Introducing A New AI/ML Base Metheodology

While traditional methods rely on heuristic techniques, Optimality Intelligent System Explorer is an AI/ML based optimization framework that integrates with multiphysics solvers to accelerate high speed interconnect design and analysis. Rather than sweeping millions of parameter combinations or relying on trial-and-error routing cycles, Optimality utilizes machine learning to converge on a compliant solution with a fraction of the effort. Fig 3. is a visual representation of the Optimality workflow.

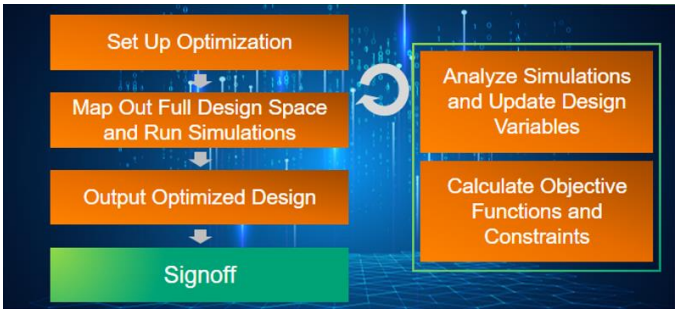

Fig. 2. Optimality Workflow

The workflow begins by defining the design space in terms of controllable parameters, such as via dimensions, trace widths, spacings, and layer transitions. Designers also specify objectives and constraints, which may include insertion and return loss limits, impedance targets, and compliance with UCIe or PCIe standards. These definitions establish the boundary conditions for exploration. Optimality does not perform physics-based calculations, instead it couples directly to sign-off solvers like Clarity 3D solver for electromagnetic analysis or Sigrity for signal and power integrity. Fig. 3. Illustrates an example workflow where Optimality is coupled with Clarity 3D Solver inside the Topology Workbench environment.

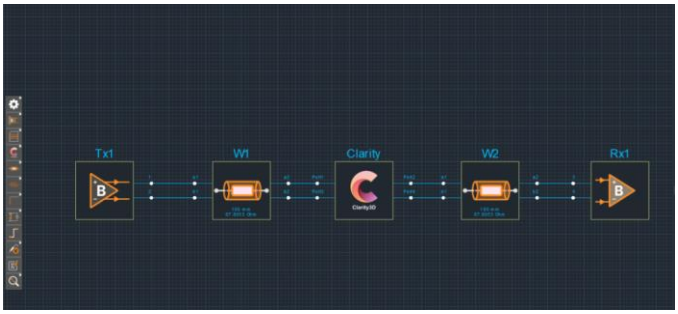

Fig. 3. Topology Workbench Block Diagram

In this example configuration Clarity serves as the high-fidelity electromagnetic solver that evaluates candidate design geometries, while Optimality manages the optimization loop. Once an initial set of simulations are performed, the results are used to build a predictive model that approximates how design parameters influence performance metrics. As more simulations are ran, this model is refined and used to predict accurate results for the overall design. By combining physics-based solvers with AI-guided exploration, Optimality can converge to a suitable solution using fewer steps than any traditional method. Optimality also supports multi-objective optimization which is particularly important for high-speed interconnects where parameters often conflict with each other. For example, minimizing insertion loss may increase far-end crosstalk. With these parameters the tool identifies trade-offs between different constraints enabling designers to assess alternative configurations and their associated compromises. This process is especially relevant for via structure and interposer optimization, where small geometric changes can introduce impedance mismatches, reflections and insertion loss that degrade high speed performances. By explicitly incorporating these effects into the optimization objectives, Optimality enables automatic refinement of designs without repeated manual iteration. In the next section, a UCIe interposer case study is optimized with Optimality.

V. UCIe Interposer Design Description

One prerequisite for the large-scale adoption of chiplet based systems is the availability of standardized die to die interposer design interconnect protocols, such as UCIe, along with robust design tools and flows capable of addressing the challenges unique to advanced packaging. In this paper we present a high-density UCIe compliant die-to-die interposer design. The chosen design reflects the growing complexity of modern heterogeneous integration, where signal integrity, electromagnetic coupling, and manufacturing constraints must be addressed simultaneously. The interposer is implemented as an 8-layer polyimide structure, within an integrated fan out Ball Grid Array package configuration. Two chiplets are interconnected through the interposer with trace lengths ranging up to 2mm, enabling high-speed die-to-die communication while maintaining compliance with UCIe electrical requirements. In total, the structure contains 4,398 blind and buried vias and 7,581 microvias, resulting in just under 12,000 vias across the full interposer. These vias serve as a combination of signal, power, and ground functions, contributing to a highly coupled electromagnetic environment. Via density introduces significant electromagnetic complexity, including impedance discontinuities, parasitic coupling, and reflection behavior that directly influence UCIe channel performance. At UCIe data rates, channel performance becomes highly sensitive to via geometry, layer transitions, and reference plane continuity. Minor geometric variations can produce measurable degradation in return loss, insertion loss, and receiver eye opening.

VI. Full Optimization Workflow

To enable focused evaluation of via-level optimization behavior within this environment, a representative signal via structure connecting the two chiplets were isolated and used as

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the primary optimization target. This via structure captures the dominant electrical characteristics relevant to UCIe signaling while allowing systematic exploration of geometric design variables. The isolated via structure was incorporated into Cadences SystemSI based channel configuration to enable time-domain analysis and seamless integration with the Optimality optimization framework. SystemSI provides a system-level environment in which transmitter, interconnect, and receiver components can be evaluated together while maintaining sign-off accuracy through direct coupling to full-wave solvers. The channel configuration consists of two Clarity 3D Solver blocks, each modeling the via structure associated with each of the chiplets. These blocks capture the full electromagnetic behavior of the via transitions, including parasitic inductance, capacitance, and coupling effects arising from the dense interposer environment. By relying on Clarity for electromagnetic evaluation, the channel response is computed using a sign-off-quality solver rather than simplified circuit-level approximations. On the transmit side, the first Clarity block is connected to a CTRL block, which represents the UCIe transmitter and generates the time-domain transmit (TX) waveform. On the receive side, the second Clarity block is connected to a MEM block, modeling the UCIe receiver (RX). A PCB block is placed between the two Clarity blocks to represent the routing segment connecting the two chiplets. While being physically implemented within the interposer, this abstraction allows the interconnect characteristics to be parameterized and evaluated consistently within the SystemSI environment. This configuration models a complete die-to-die channel, including transmitter, via transitions, routing segment, and receiver. The corresponding SystemSI schematic is shown in Figure 4. Embedding the channel within SystemSI enables direct access to Optimality, which is natively integrated into the environment and capable of automatically controlling design variables and invoking simulations during the optimization process. SystemSI provides a system-level environment in which transmitter, interconnect, and receiver components can be evaluated together while maintaining sign-off accuracy through direct coupling to full-wave solvers. An additional benefit of using SystemSI with Optimality is that the optimization targets can be system-level metrics such as eye height and eye width. This goes beyond traditional s-parameter-based goals—like return loss, insertion loss, or crosstalk—and enables exploration of design combinations that conventional 3D electromagnetic optimizers may miss.

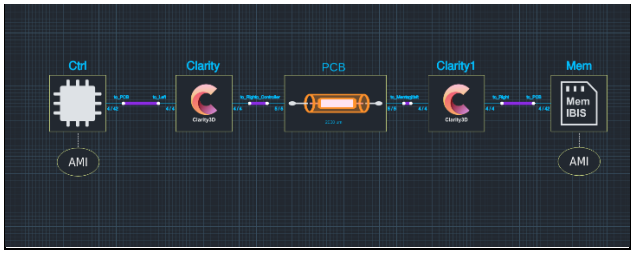
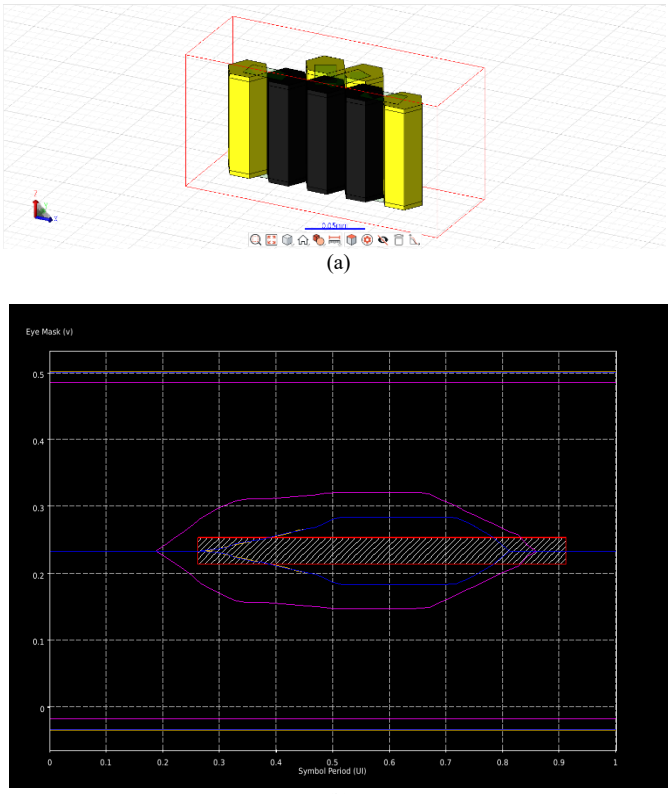


Fig 4. SystemSI Block Diagram Representing Die-To-Die Interconnect Path

VII. Simulation Baseline and Results With Optimality

Using the channel configuration described in the previous section, an initial set of simulations was performed using default design parameter values for the isolated via structure. These baseline simulations were run within SystemSI, and the resulting time domain waveforms were evaluated using the UCIe compliance kit. The receiver eye contour obtained from this baseline did not meet the UCIe compliance criteria, indicating insufficient margin under the default parameter settings. Figure 5 shows an image of the baseline via structure configuration (Fig 5a) and UCIe Compliance Masks for Eye Diagram (Fig 5b). These results were used as the reference point for the optimization results presented in the following section.



(a)

(b)

Fig 5. Baseline Via Structure and UCIe Compliance Kit Eye Diagram

VIII. Results With Optimality

Following the baseline simulations results, the channel configuration was integrated into Optimality to perform parametrized optimization, targeting time-domain UCIe compliance metrics. Within the Optimality environment, a set of geometric parameters was identified and parameterized based on their expected influence on eye contour characteristics. The selected optimization parameters describe key aspects of via geometry and spatial relationships within the isolated interposer structure. This included the via radius of each individual structure, signal to signal via spacing, signal to ground via spacing, and trace width. To reduce the number of independent design variables of the optimization problem while preserving sensitivity to dominant effects, expressions were defined within Optimality to group related geometric

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parameters i.e. via radius and trace width. This resulted in four primary optimization variables: S_S_spacing, G_S_spacing, Y_ground_spacing, and via_radius. These grouped parameters enable systematic exploration of via geometry and spacing relationships while maintaining consistency across layers. Each variable was then assigned a bounded range consistent with interposer and advanced packaging design rules to capture practical layout limitations. Finally, optimization objectives were defined in the function table to maximize eye contour height and width. Using this configuration, Optimality iteratively generated candidate designs, executed SystemSI simulations and evaluated eye performance.

Parameter	Range(um)	Step Size	Initial Result (um)	Final Result (um)
S_S_spacing	10-100	1	0	31
G_S_spacing	10-100	1	0	78
Y_ground_spacing	10-100	1	0	70
Via_radius	5-20	.5	13	5

Fig 6. Table Summary of Parameter Values and Final Results

In total a manual sweep of the four optimization variables over their defined range would require evaluating more than 23 million parameter combinations, rendering such an approach impractical for sign-off-level simulations. Using the proposed optimization approach, a UCIe-compliant solution was identified within 100 simulation iterations. Figure 7 presents the optimization results as displayed within the Optimality user interface, including the convergence history and result table. The best performing configuration is highlighted in red, illustrating how the AI/ML-based optimization iteratively improved the design toward UCIe compliance.

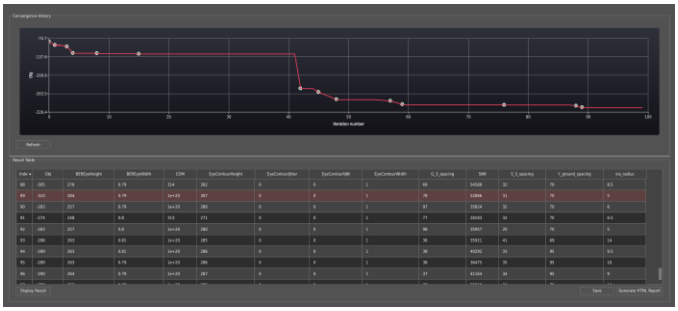

Fig 7. Optimality Convergence History and Result Table

The optimized configuration satisfied the UCIe compliance criteria achieving a receiver eye high of 40mV and an eye width of .65 UI. Figure 8 shows the resulting via geometry (Fig 8a) and the corresponding receiver eye diagram with the UCIe eye mask overlaid (Fig 8b). These results demonstrate the benefits and capabilities of an AI/ML-based optimization framework, which can rapidly explore complex via design spaces, optimize critical parameters, and achieve UCIe compliance with minimal simulation effort.

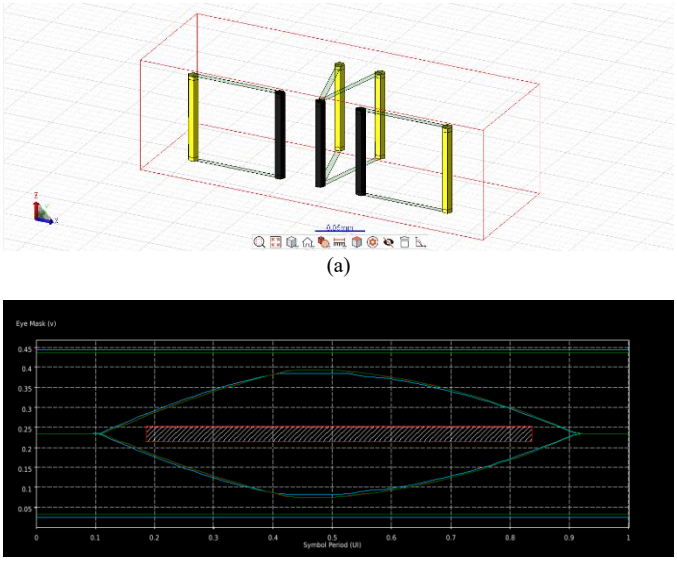

Fig 8. Optimized Via Structure and UCIe Compliance Kit Eye Diagram.

IX. Conclusion

This work presents a methodology for applying AI/ML-based optimization to a UCIe-compliant die-to-die interposer. A representative via structure was analyzed using a sign-off-quality simulation flow integrating SystemSI, Clarity, and the SystemSI UCIe compliance kit. By parameterizing key via geometry and spacing variables, the optimization process was formulated directly in terms of time-domain compliance metrics. The results show that a UCIe-compliant solution can be achieved within a small number of simulations when guided by AI/ML-based optimization, compared to the prohibitive cost of exhaustive parameter sweeps. This approach enables efficient exploration of complex via level design spaces while maintaining consistency with sign-off analysis requirements. As interposer density and signaling rates continue to increase, such methodology driven optimization techniques provide a practical path toward meeting stringent die-to-die compliance targets in advanced packaging designs.

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