Heterogeneous Integration for Direct RF Digitization: Packaging Strategies for Wideband Software Defined Sensor Systems

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***Abstract*—Direct RF digitization is reshaping the architecture of radar, EW, and wideband sensing systems by enabling direct sampling of multi-GHz to millimeter-wave (mmW) signals. However, translating the performance of advanced data converters and digital processing ICs into deployable, size-weight-and-power (SWaP)-constrained modules requires better packaging architecture to gain improved module signal integrity power delivery and thermal performance. Today's heterogeneous-integration (HI) ecosystem imposes additional constraints that complicate module co-design: chiplets arrive with fixed I/O functions, pre-defined bump maps and power-pad distributions; interposer technologies offer limited routing granularity in redistribution layers (RDLs) and insufficient freedom to separate RF, digital, and power domains and to extract module heat efficiently; and packaging Process Design Kit / Assembly Design Kits (PDKs/ADKs) models remain immature, preventing robust co-simulation of RF, mechanical, and manufacturing effects such as warpage, CTE mismatch, and process variation. These ecosystem limitations restrict the available "tuning knobs" needed to optimize wideband RF signal paths, mixed-signal interfaces, high-speed SerDes data movement, and multi-hundred-watt thermal extraction.**

To address the above HI system-driven challenge exacerbated by current business models and manufacturing realities, an improved HI RF digitation module architecture is proposed—including function-sensitive RDLs for RF/mmW routing, low-loss power-delivery architectures, multi-tier thermal paths, and EDA/PDK innovations. Analytical modeling calculations and simulations demonstrate significant improvements compared to traditional HI architecture, including ~27 dB lower RF-digital isolation, ~45°C peak module junction temperature reduction and ~640 mV maximum module IR voltage drop improvement. These enhancements in signal integrity, thermal and power performance is crucial to stabilize data converter linearity, reduce clock-jitter coupling, and improve FPGA digital timing closure, and enable next generation scalable, deployable direct-RF digitization modules.

Keywords—RF, heterogeneous integration, direct sampling, EW, radar, SWaP, mmW, ADC, FPGA, SiP, PDN, ADK, OSA, RDL, HI.

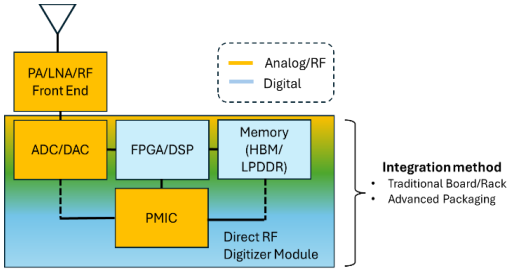

Fig.1. Conceptual block diagram of an direct RF digitizatoin module

I. Introduction

Direct RF digitization eliminates multiple analog frequency-conversion stages and enables highly flexible, software-defined signal-processing pipelines [1-3]. As illustrated in Fig. 1, a typical end-to-end RF direct digitization module is composed of building blocks from Analog-to-Digital Converters/Digital-to-Analog Converters (ADCs/DACs), Field-Programmable Gate Arrays (FPGAs), memory blocks and power management chiplets (PMICs). Modern ADCs/DACs operating at 20–250 GS/s and wideband RF sampling capabilities are enabling architectures that were previously incompatible with SWaP-constrained deployments [4,5]. Yet while device-level data converter and digital-processing performance has accelerated rapidly, packaging technologies, business practices, and EDA ecosystems have not evolved at the same pace [6].

A significant portion of the integration challenge arises from the fact that packaging engineers seldom control the full set of required HI parameters to achieve optimal performance [7]. For example, commercial IC vendors deliver dies or chiplets with fixed I/O functions/geometries/bumps, and predetermined mechanical/thermal/power constraints. These fixed interfaces—set for generic markets rather than high-performance RF digitization—limit the ability to tune interconnect impedance, transition parasitics, equalization structures, or return-current pathways needed for multi-GHz to mmW signal chains.

Similarly, current 2.5D/3D packaging techniques [8-11] provide limited flexibility in RDL assignment, stack-up profiles, thermal vias density/locations and backside power distribution

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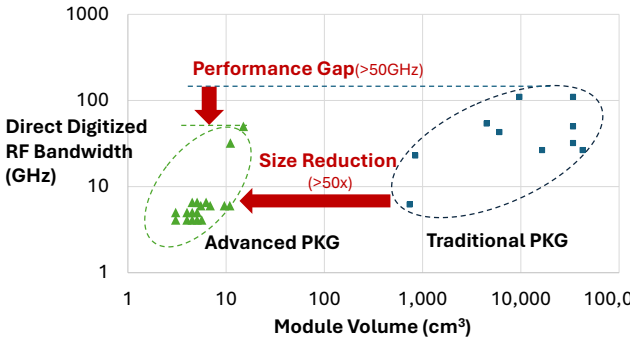

Fig. 2, Performance gap (e.g direct digitzed RF bandwidth) and module size reduction between advanced packaging-based direct-RF digitization modules and traditional board/rack-based direct-RF digitzation modules [17,18]

options. Instead of routing RF signals, digital SerDes, clock lines, and power networks through optimized, function-specific stack-ups to mitigate loss, crosstalk, and thermal issues, packaging designers must crowd them into a few shared metal layers. Consequently, packaging engineers face a heavily constrained design space that compromises overall module performance.

Equally important, today's packaging ADKs/PDKs do not yet offer mature, HI-layer-sensitive co-simulation-ready models that span electromagnetic, mechanical, thermal, and manufacturing physics [12]. This gap will widen as function-specific stacking HI modules become more broadly adopted in future designs. Consequently, these EDA limitations directly impact manufacturability and yield—particularly for modules that combine RF front-ends, multi-GHz data converters, FPGAs, HBM stacks, and high-density power regulation in a single volume-constrained SiP.

Although direct-RF digitization promises major architectural advantages, today's HI implementations still fall short of the performance (e.g. direct digitized RF bandwidth) achieved by traditional rack-mount or board-level direct-RF systems, as shown in Fig. 2 [17,18] due to the above mentioned integration challenges. A more unified, system-driven HI packaging approach that overcomes both technology gaps and ecosystem fragmentation is required. Over the past decade, despite rapid improvements in device-level ADC/DAC and FPGA performance, today's HI ecosystems impose fixed chiplet interfaces, limited RDL freedom, immature multi-physics PDK/ADK models, and constrained thermal/power pathways. These limitations prevent direct RF digitization modules from achieving the bandwidth, isolation, and reliability of traditional rack-level systems. To address this gap, this work contributes: (1) a system-driven HI architecture with function-specific RDL partitioning, (2) a backside power-delivery and multi-tier thermal-management framework, (3) analytical RF, PDN, and thermal models validating first-order performance improvements, and (4) full-wave EM, CFD, and PDN simulation results demonstrating substantial isolation, IR-drop, and junction-temperature gains over traditional HI packaging.

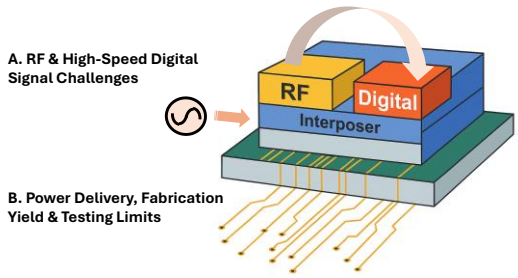

Fig. 3, Multi-domain integration challenges under SWaP Constraints : a) RF & high-speed digital signal challenges; b) Power delivery , fabircation yeild & testing limits, and c) analytical modeling frameworks and proposed HI module performance evaluation

II. Multi-domain Integration Challenges Under SWaP Constraints

Direct RF digitization requires integrating RF, mixed-signal, and high-performance digital subsystems within an ultra-compact module volume (typically less than 10 – 50 cm^3). HI faces severe technical interconnected bottlenecks across the following two core pillars (also illustrated in Fig. 3).

A. RF and High-Speed Digital Signal Challenges

• Insertion Loss & Impedance Discontinuities: Operating up to 40–100+ GHz scales transmission losses rapidly (~0.8–1.5 dB/cm) due to surface roughness and parasitic transitions. Sub-picosecond edge rates turn geometric variations into signal reflections, straining return-loss budgets (< -10 to -20 dB) and degrading spurious-free dynamic range (SFDR). [9,10].

•Interposer & Interface Rigidity: Commercial chiplets feature fixed I/O maps. Lacking fine-grained layer customization, multi-GHz traces are forced through sub-optimal digital substrate layers, requiring parasitic-heavy routing that alters the intended S-parameter response [11].

• Additive Jitter & Latency Budgets: Supporting 20–250 GS/s converters at 7–12 bit resolutions requires clock distribution networks with <50 fs of additive package jitter [15,16]. Real-time digital RF demands deterministic, uninterrupted data streaming over 20–56 Gbps links while maintaining strict 10–100 ns application latencies.

• Cross-Domain Crosstalk: High-frequency clock paths and analog RF inputs are highly vulnerable to digital switching noise. At multi-GS/s rates, this digital logic crosstalk injects phase noise and severely degrades the effective number of bits (ENOB) [15].

• Thermal-Induced Timing Drift: Co-locating FPGAs (150–300 W) [17,18], data converters (10–40 W/chiplet) [4,5], and HBM yields extreme local densities (>8–15 W/cm^3). The resulting temperature drift alters interconnect delays, degrading converter linearity and compromising FPGA timing closure.

B. Power Delivery, Fabrication Yield, & Testing Limits

• Sub-pH PDN Challenges: PDNs must achieve sub-pH scale loop inductances to eliminate reference droop and

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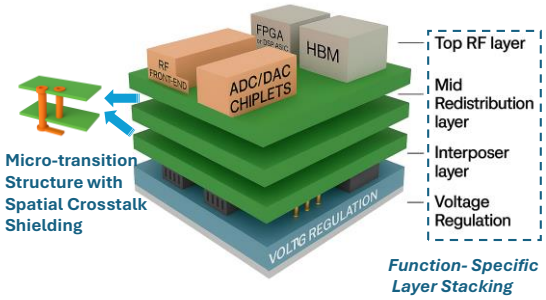


Fig. 4, Fine-grained Domian Function-specific integration architecture for RF and high-speed digital signal integrity, including function-specific layer stacking and micro-transition structure with spatial crosstalk shielding

simultaneous switching noise (SSN) across multi-thousand-lane interfaces [19].

• Thermomechanical Deflection: Coefficient of thermal expansion (CTE) mismatches cause organic interposers to warp during high-temperature reflow, causing microbump cracking or bridging defects within strict ±3–5 µm placement windows [20].

• Testing &Yield Blind spots: High integration density eliminates physical test nodes, rendering mmW joint inspection impossible. Incomplete wafer-level component testing shifts failure detection to the final assembled module level, compounding yield loss [21].

III. Improved HI Solutions

To overcome the multi-domain physical and supply-chain constraints outlined in Section II, a HI architecture is proposed using function-sensitive interposer capabilities, backside power delivery with multi-tier thermal management and AI-driven ADK/PDK ecosystem for automatic stack-up co-design. Please note that the AI-driven ADK/PDK framework described here is conceptual and its full implementation and evaluation remains futurework.

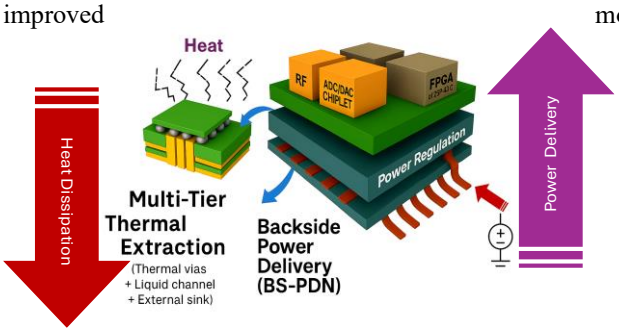
A. Fine-Grained Function-specific Integration Architecture for RF and High-speed Digital Signal Integrity

To resolve COTS chiplet interface restrictions (e.g. fixed I/O functions and locations) and improve the signal integrity of multi-GHz to mmW RF and high-speed signals, a function-specific RDL architecture is proposed with fine granularity and improved cross-domain physical isolation (illustrated in Fig 4).

- Function-Specific Layer Stacking: The interposer features dedicated, thin-film RF layers optimized with low loss tangents and minimized copper surface roughness. This configuration minimizes insertion loss up to 100+ GHz, bypassing standard digital substrate routing limitations [22].
- Micro-transition Structure with Spatial Crosstalk Shielding: Micro-transition structures are customized with sub-micron precision to match the pre-defined I/O maps of COTS chiplets with minimized transition loss. Embedded vertical shielding structures and localized ground walls isolate high-frequency analog RF lines from neighboring digital logic layers [23,24].

B. Backside Power Delivery Network (BS-PDN) & Multi-Tier Thermal Management

To isolate high-current power routing from sensitive signal paths and manage extreme volumetric thermal loads, the improved module



decouples power delivery path and high-speed signal path by introducing a vertically integrated BS-PDN with multi-tier thermal extraction, as shown in Fig. 5.

- Sub-pH Backside Power Delivery: Implementing a BS-PDN routes the high-current power networks through the reverse side of the substrate using ultra-dense, low-resistance through power vias (TPVs). This eliminates SSN and reduce voltage droop by efficiently delivering power through sub-pH loop inductances in dedicated power delivery paths and reduce the coupling between PDN and signal paths [25-26].
- Multi-Tier Thermal Extraction: The improved architecture integrates a multi-tier thermal extraction networks, including direct-attach thermal interface .materials (TIMs) link for high-power FPGAs (150–300 W) and data converter chiplets, vertically integrated thermal vias, micro-channel liquid cold plates and external heat sink [28,29].

Fig. 5, Backside Power Delivery and Multi-Tier Thermal Management: a vertical BS-PDN architecture suppresses SSN and mitigates IR drop. Thermal dissipation is optimized via a multi-tier extraction framework, a low-resistance thermal pathways using integrated thermal vias, microfluidic channels, and external heat sinks.

C. AI-Driven PDK/ADK Ecosystem for Automated Stack-Up Co-Design

An AI-driven ADK and PDK design automation conceptual framework is introduced here to bridge the gap in predictive modeling and accelerate multi-domain, customized function-specific layer stacking development. Its full implementation and evaluation remains futurework.

- Automated Metal Stack Profiling: The AI engine dynamically modifies the interposer metal stack profile inside ADK/PDK to simultaneously optimize high-frequency electromagnetic performance, thermal dissipation paths, and mechanical strain vectors. This will greatly reduce the development cycle of function-specific layer stacking development to optimize RDL deign parameters in Section III-A [30,31].

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- Multi-Domain Predictive Simulation and Yield improvement: The framework replaces traditional fragmented simulation workflows with integrated, automated blocks that accurately predict frequency-dependent loss up to 100+ GHz, dynamic substrate warpage during reflow, and localized electrical-thermal-mechanical couplings. By running predictive manufacturing-tolerance models, the AI-driven ADK/PDK optimizes die placement windows and thermal/power via geometries prior to physical tapeout, mitigating CTE mismatch defects, assembly yield and other key module performance metrics [32,33].

IV. Analytical Modeling Framwork for Multi-domain HI Module Performace Evalatuion

To quantify the impact of the proposed heterogeneous-integration architecture for the first-order estimation of insertion loss, crosstalk, supply-rail droop, and junction-temperature reduction, analytically derived models were developed for three primary physical domains: (A) RF/mmW signal integrity, (B) power-delivery performance, and (C) thermal conduction efficiency. The analytical modeling approach is shown below [34,35]:

A. RF and High-Speed Signal Integrity Analytical Model

A1. RF Insertion-Loss Model

Insertion loss α was estimated using standard thin-film transmission-line equations combining conductor attenuation, dielectric attenuation, and surface-roughness effects:

$$\alpha_{tot}(f) = \alpha_c(f) + \alpha_d(f) + \alpha_{rough}(f) \quad (1)$$

where α_c is conductor loss, approximated using skin-depth approximated using skin-depth $\delta_s = (2/\omega\mu\sigma)^{1/2}$, $\alpha_d = (\pi f/c)\epsilon_r{}^{1/2} tan\delta$ models dielectric loss, and α_{rough} incorporates the Hammerstad-Jesen roughness correction for organic and thin-film metal.

A2. Crosstalk Analytical Model

Near-end (NEXT) and far-end (FEXT) crosstalk were estimated using coupled-line equations:

$$V_{NEXT} \cong j\omega K_{NEXT} M\, I \quad (2)$$

$$V_{FEXT} \cong j\omega K_{FEXT}(M - L_{EVEN})\, I \quad (3)$$

where I represents aggressor line current where M is mutual inductance, L_{EVEN} is even-mode inductance, K is a constant and ω is the angular frequency.

B. Power-Delivery Network Analytical Model

B1. Loop-Inductance Model

PDN was estimated through a lumped L–R model:

$$V_{droop}(t) \approx L\frac{di}{dt} + I(t)R \quad (4)$$

B2.Transient Droop Model

A load transient representing FPGA switching activity (di/dt ≈30–60 A/ns was applied.

$$\Delta V_L(t) = L\frac{di}{dt}, \Delta V_R = I_{PEAK}R \quad (5)$$

B3. PDN Impedance Envelope

The frequency-domain PDN impedance was approximated using $Z(j\omega) = R + j\omega L + 1/j\omega C$.

C. Thermal Management Analytical Model

C1. Thermal Resistance Network

Heat-flow performance was modeled using a vertical thermal-resistance chain:

$$R_\theta = \sum_i \frac{t_i}{k_i A} \quad (6)$$

where t_i is layer thickness, k_i thermal conductivity of layer, A is die-footprint area. Baseline configuration includes die→ Thermal interface material (TIM)→interposer→PCB, while the proposed multi-tier thermal architecture varies vertical thermal-via array, improved TIM, thinner RF routing layers with higher k, and more direct conduction path to lid/heat-exchanger [36].

C2. Steady-State Gradient Model and PDN Impedance

A load transient representing FPGA switching is modeled below*:*

$$\Delta V_L(t) = L\frac{di}{dt}, \Delta V_R = I_{PEAK}R \quad (7)$$

The frequency-domain PDN impedance was approximated using $Z(j\omega) = R + j\omega L + 1/j\omega C$. (8)

V. HI Module Performace Evalatuion

To evaluate the benefits of the improved module architecture, simulations of three key performance indicators — RF-digital signal isolation, peak module junction temperatures, and maximum module IR voltage drops—were conducted and compared with analytical model calculations. The improved module is configured with a stacking profile featuring two function-specific layers and one backside power distribution layer, with three different configurations (Config 1, 2, and 3) and parameters enumerated in Fig. 6, while the traditional module is configured with one redistribution layer and without the layer for backside power distribution and multi-tier thermal extraction. The simulations, performed under Full-wave EM (HFSS) [37], thermal CFD (Icepak) [38], and PDN (RedHawk) [39], showed digital-RF isolation strengthening from -35 dB to -62 dB, junction temperature decreasing from 125 °C to 78 °C, and DC IR drop reducing from 650 mV to 80 mV, and demonstrated the synergistic benefits of function-specific RDL layer partitioning, coaxial shielding, and high-density backside power delivery. To validate these simulation insights, we also benchmarked the results against first-order analytical calculations described in Section IV and plotted in Fig 6. While the analytical models correctly capture the scaling trends, deviations emerge due to second-order physical effects. Specifically, simulations consistently predict 2–5 °C higher junction temperatures, 1–7 mV larger IR drops, 4-5dB worsening isolation, compared to analytical models, attributed to non-uniform hotspot clustering, current crowding at via

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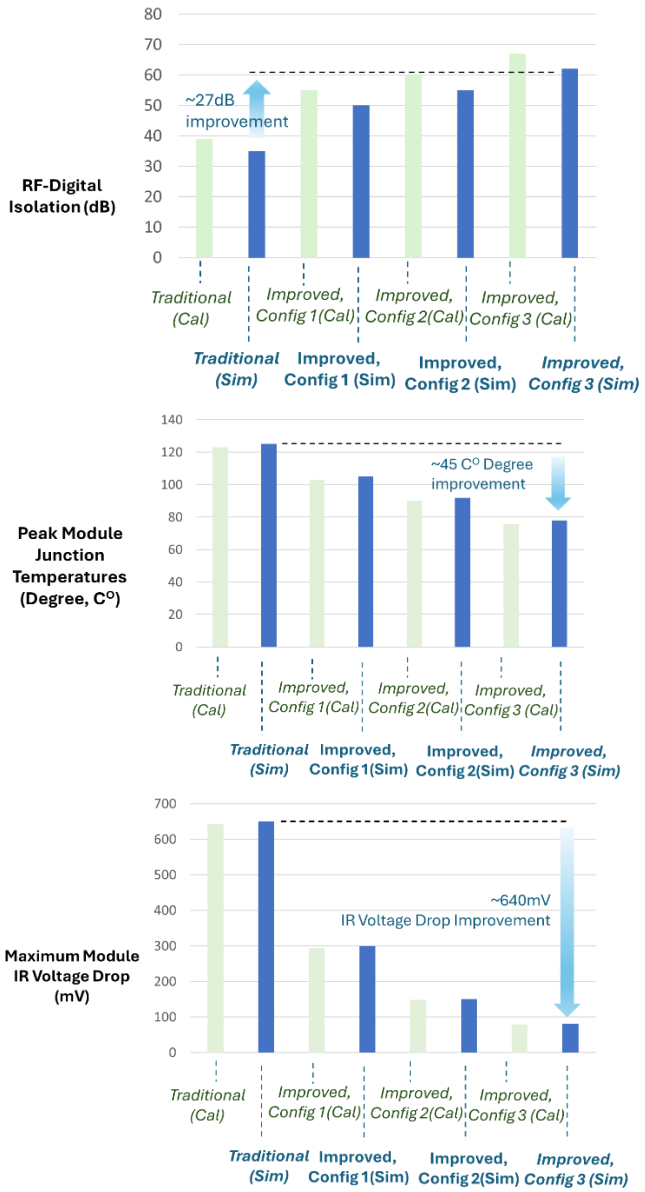

Fig. 6, The key module performance (RF-digital isolation, peak module junction temperatures and maximum module IR voltage drop) comparison between traditional architecture (single RDL , no thermal vias, no RF shielding, no backside power distribution) and three improved architecture configurations Config. 1,2, and 3. Config. 1 introduces a fundamental architectural shift by partitioning RDL functionality into two frontside layers and a dedicated backside layer; while the backside power layer is with 3 µm thickness and a 150 µm pitch , the shielding remains limited to basic coplanar ground-signal-ground (GSG) structures and thermal vias are uniformly distributed at a low 5% density. Config. 2 refines this by implementing targeted coaxial shielding for critical RF interconnects and concentrating thermal via arrays at 10% density beneath predicted power-dense zones, while the backside power layer is with 3 µm thickness and a 100 µm pitch. Config. 3 culminates this layout progression with a fully optimized physical stack: two frontside RDL layers strictly partitioned for digital and analog routing isolation—ensuring that high-speed switching currents never share a plane with sensitive RF waveforms—complemented by a dedicated 3 µm thick backside power layer with a tight 50µm pitch. This is also coupled with integrated coaxial/GSG shielding structures that completely surround sensitive RF lines interconnects. A first-order analytical calculation (described in Section IV, marked in light green) was conducted to validate the simulation results (marked in blue) with good agreement.

corners, and RF return paths in-direct coupling in the high-density 2.5D heterogeneous integration floorplan. In simulation, the proposed architecture shows an isolation enhancement of up to 27 dB, a temperature reduction of 45°C, and a 640mV mitigation in voltage drop, while analytical model closely matches the simulated performance, confirming its validity.

VI. Conclusion and Futurework

This work addresses HI challenges for SWaP-constrained direct RF digitization, analyzing whether rigid chiplet ecosystems, limited routing, and fragmented EDA tools inhibit direct RF digitization HI module to enable next generation wideband sensing systems. The novelty of this work lies in the unified HI co-architecture specifically tailored for direct RF digitization—integrating function-specific RDLs, backside power delivery, and multi-tier thermal extraction into a single optimized module rather than proposing new individual component technologies. To overcome these bottlenecks, the study proposes an improved HI architecture featuring a function-specific redistribution layer, backside power-delivery, and multi-tier thermal management, demonstrating superior RF-digital isolation and thermal/power performance through simulation and analytical modeling calculation. The proposed architecture achieves up to 27 dB of RF-digital isolation improvement, a 45 °C reduction in peak junction temperature, and up to 640 mV IR-drop mitigation compared to traditional HI configurations. This work is limited to analytical models and simulation-based evaluations and does not include fabrication or system-level measurements. Future work includes implementing the AI-driven ADK/PDK optimization engine and experimentally validating the proposed HI module architecture.

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