# Additively Manufactured Module Packaging for Millimeter Wave Applications

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## Abstract

This work focuses on Antenna-in-package (AiP) monolithic RF packaging enabled by additive manufacturing using low-loss, high-temperature ceramic-loaded resins for reduced loss and compact RF front-end integration. Many modern RF ICs, field-programmable gate arrays (FPGAs), and power management ICs are fabricated in advanced high-density packaging formats with fine-pitch array-style contacts. These packaging architectures present significant challenges for additive integration with printed electronics due to their small contact geometries and high interconnect density. To address these challenges, novel additive manufacturing (AM) methods are explored to embed advanced ICs directly alongside printed traces and passive components within resin-printed substrates. This approach leverages engineering grade resins and high-resolution digital light processing (DLP) printing to improve fabrication precision while reducing processing time. These methods involve monolithic printing of multiple resin materials, conductive inks, and embedded components using a fabrication process that supports batch production, enabling multiple devices to be manufactured simultaneously. The workflow consists of repeated cycles of printing, cleaning, pick-and-place, metallization, and milling, all performed without removing the parts from the build plate. This approach enables the layered buildup of a package with conformal features and topologies that are not achievable with traditional manufacturing methods.

## Key words

Additive manufacturing, Antenna-in-package, Embedded, Millimeter-wave, Monolithic, Printed electronics.

## I. Introduction

The demand for high-performance radio frequency (RF) systems in sensing, communications, and radar technologies has driven significant research in packaging methods that outperform traditional wire bonding and flip chip techniques. Additive manufacturing (AM) offers a novel alternative to conventional injection molding, cavity, and wafer level chip scale packaging (WLCSP), enabling faster prototyping, complex features, and material customizability. A key advantage of AM in RF packaging is the ability to fabricate complex three-dimensional structures that are not feasible with conventional subtractive manufacturing, providing greater design freedom for RF performance optimization [1].

Additive processes such as resin-based stereolithography (SLA), fused deposition modeling (FDM), polymer jetting (PolyJet), aerosol jet printing (AJP), direct-write methods, and semi-additive subtractive techniques have been successfully researched and tested to create advanced RF packages [2]. These methods allow for improved control of dielectric properties, electromagnetic performance, and conformal designs, outperforming conventional wire bond-based systems in terms of impedance and parasitics.

Although AM has demonstrated potential for improving the RF performance of interconnects, it has yet to match the size, weight, power and cost (SWaP-C) of traditional packaging techniques. This gap is likely due to the comparatively lower technological maturity of additive manufacturing processes and materials than conventional semiconductor fabrication technologies. Conventional packaging approaches are highly optimized and support the integration of multiple components within complex 2.5D and 3D designs. Techniques such as stacked die multi-layer wire bonding, through-silicon vias (TSVs) [3] and Intel's Embedded Multi-die Interconnect Bridge (EMIB) [4] enhance system-on-chip (SoC) and system-in-package (SiP) capabilities [5],[6]. Despite current limits, AM presents an opportunity to improve future RF packaging. Its ability to customize material properties and geometries offers an option for high-performance RF integration that may complement conventional techniques or be used for low quantity production in the near future.

Prior research has explored embedding not only bare dies but also fully packaged integrated circuits (ICs), WLCSPs, and passives within AM substrates [7-11]. The ability to integrate passive components and printed rf features directly alongside active ICs reduces circuit complexity and enables the construction of module structures tailored for 2.5D or future 3D integration.

This work focuses on monolithic RF packaging enabled by Digital Light Processing (DLP) printing of low-loss, high-temperature ceramic loaded resins. This approach supports integrated structures such as planar and three-dimensional antennas, and embedded components, enabling compact electromagnetic systems. This process is well suited for millimeter-wave applications where performance benefits from tight integration and complex geometries.

The developed process enables a workflow in which both dielectric and conductive elements can be fabricated in a batch process using conductive inks and dielectric resins that are subsequently deposited and solidified into arbitrary printable topologies. This material form factor provides design freedom, enabling complex three-dimensional structures without reliance on pre-formed solids or discrete component assembly.

By leveraging processable materials, this approach enables on-demand fabrication of functional structures directly within the available manufacturing setup, reducing dependence on standardized, off-the-shelf materials and conventional supply chains. As a result, overall manufacturability is improved in resource-constrained environments where access to standardized materials, large equipment, or external vendors may be limited.

The process relies on low-cost, small-form-factor equipment, including a DLP printer, an airbrush-based metal deposition system, and a small milling tool for finishing.

## II. Methods

### *A. Fabrication Process*

The fabrication procedure is illustrated in Fig. 1 and can be summarized as follows: (a) A cavity for the IC is fabricated using an Asiga DLP printer. (b) The IC package is positioned within the printed cavity. (c) A sealing and masking layer is printed over the embedded components (d) Conductive ink is then deposited into the predefined microchannels using either spray coating or doctor blading, followed by surface cleaning. (e) The assembly is reinserted into the Asiga printer, and an encapsulation layer is printed to provide protection while also selectively exposing designated contact points for electrical interfacing.

One of the primary challenges in AM approaches is establishing reliable conductive interconnects. When components are embedded within printed cavities, the component-substrate interface must be properly sealed to prevent conductive ink from wicking into the gap. This issue is typically mitigated by filling the interface with a dielectric material or by using high-viscosity conductive inks that minimize spreading and ensure electrically isolated connections. In this approach, the sealing and masking layer is designed to overlap with the component within the cavity, producing a cured dielectric that directly bridges the gap and bonds to the component surface. This capability is enabled by placing the components during the fabrication process and subsequently reinserting the assembly into the printer to continue printing. Conventional approaches that place components after the substrate has been fully printed cannot form this bonded dielectric seal around the embedded component without introducing additional printing or processing steps.

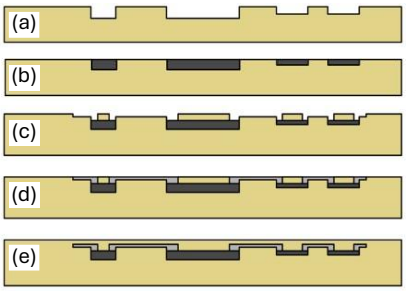



Fig. 1. Fabrication process: (a) fabrication of the integrated circuit cavity and structural layer, (b) placement of the component within the printed cavity, (c) printing of a sealing layer over the embedded component, (d) deposition of conductive ink into the printed microchannels followed by surface cleaning to form conductive features, and (e) printing of the encapsulation layer while selectively exposing designated contact points for electrical interfacing.

### *B. Design and Manufacturing*

The device geometry, including the layer stack-up and conductive features, is first created in CAD software. The RF structures are then modeled and simulated in Ansys HFSS. As shown in Fig. 2, the simulation model incorporates multiple material domains and conductive features to accurately represent the fabricated structure. The complete assembly is then imported into HFSS for simulation and design verification. This design workflow enables iterative optimization between the physical layout and electromagnetic performance prior to fabrication.

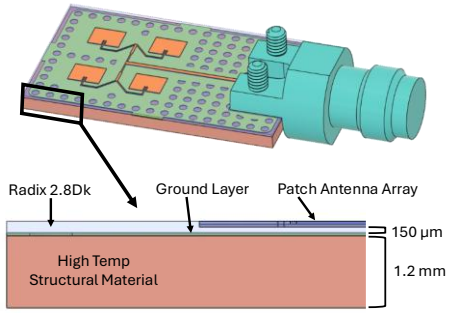



Fig. 2. Design of patch antenna array showing multiple materials and multiple conductive layers.

The final 3D design is then sliced into projected layers for fabrication on an Asiga Max X27 DLP printer. Fig. 3 illustrates the layer features generated from the 3D model. White pixels represent regions exposed to UV light where the resin is cured, while black pixels indicate non-exposed areas in the projection mask.

A high-temperature resin is used to print an initial 1.2 mm-thick structural layer, providing a rigid support for subsequent RF layers as well as additional thickness where embedded components could be integrated. The first metallization layer forms a ground plane and includes small bonding features to promote adhesion between the high-temperature structural resin and the subsequent low-loss dielectric resin. A perimeter sealing structure is also printed to bond the interfaces between polymer layers. Next, a low-loss resin (Rogers Radix 2.8) is printed across the full layer at a thickness of approximately 150 µm. The final RF feature layer, in this case comprising of a patch antenna and feed network, is then patterned to form a 50 µm-deep channel designed for conductive ink deposition.

Throughout fabrication, after each metallization step, surface cleaning is performed to remove approximately 25 µm of material. This process exposes fresh polymer surfaces and removes residual conductive ink from designed regions, ensuring electrical isolation and maintaining high feature resolution.

The proposed fabrication process employs projection-based printing, which cures an entire layer simultaneously to enable batch manufacturing and reduce fabrication time. Using this process, three devices were printed and metalized concurrently. With larger-format printers, this approach can be scaled to enable simultaneous fabrication of many devices. This parallel fabrication capability improves throughput while maintaining design consistency across multiple printed units.

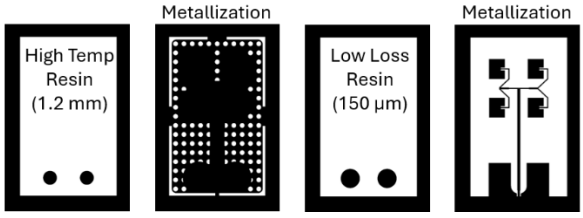



Fig. 3. DLP Layer projection stack up for each feature of a 2x2 patch antenna array

As seen in Fig. 4, after each metallization step, milling is performed to remove conductive ink from the features printed in the previous layer. Designed holes for edge connector mounting, along with features on each side of the structure, enable electrical continuity between the top ground feature, the grounding layer, and the sidewalls, ensuring a continuous ground connection throughout the device.

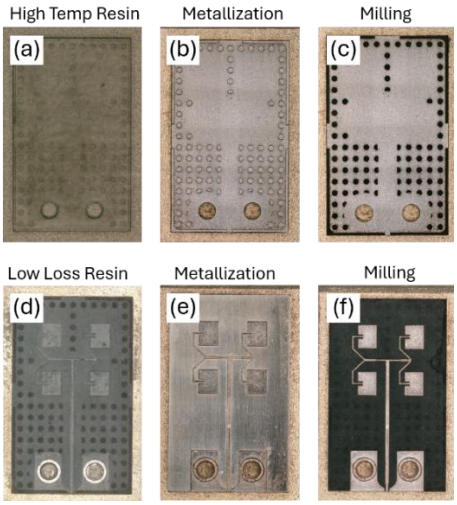



Fig. 4. Manufacturing process steps: (a) high-temperature resin printed for structural rigidity, (b) metallization of the ground layer, (c) milling of the top surface to expose the underlying polymer, (d) deposition of low-loss resin and printing of features to support conductive ink, (e) metallization of RF features, and (f) final surface milling to expose polymer and define RF features.

### *C. Component Integration*

Packaged components with external leads, such as Dual In-line Packages (DIP) and Small Outline Packages (SOP), are readily integrated into printed electronics due to their large contact areas and relatively wide lead pitch. However, many modern RF ICs, microcontrollers, and FPGAs are implemented in much smaller-pitch packages, making integration increasingly challenging as device form factors continue to scale down. Passive components, including resistors, capacitors, and inductors, are essential elements in most RF systems, whether integrated within the package in system-in-package (SiP) implementations or mounted externally on an RF module. AM has shown abilities for similar circuit topology for integrating these components directly into the package, aiming to reduce overall size and simplify circuit architecture. These components are essential for filtering, decoupling, and power management, and must be placed in close proximity to active devices to achieve RF performance comparable to that of conventional packaging technologies.

In this study, component integration was evaluated using a standalone printed structure to verify performance and functionality. The substrates were fabricated using the same process flow as the patch antenna array, with components placed into designed cavities prior to the application of the sealing and masking layers. Conductive ink was then deposited, patterned, and cured, followed by evaluation of RF performance, electrical continuity, and environmental stability.

The Embedded Component testing was initially evaluated using quad flat no-lead (QFN) components with a 0.5 mm pitch between contacts and passive surface-mount components of multiple sizes.

## III. Results

### A. Component Integration

As shown in Fig. 5, each contact on the QFN can be routed with tapered traces and connected to larger, more widely spaced exposed pads. The fine tapered features achievable with this fabrication method enable the realization of impedance-matched transitions and structures for RF packaging. In addition, the approach simplifies component integration by facilitating both precise component placement and seamless electrical interconnection within additively manufactured systems.

Placement of components into the cavities was performed manually using tweezers. Alignment is achieved by appropriately sizing the cavity to securely seat the component, providing mechanical self-alignment during insertion. Prior to returning the assembly to the printer after component placement, resin is manually deposited over the component to eliminate air pockets that would otherwise become trapped during subsequent processing.

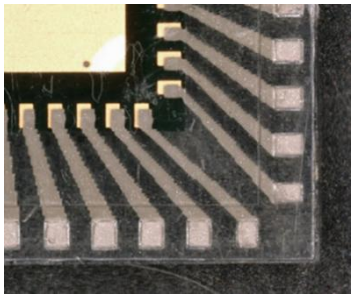


Fig. 5. View of an embedded QFN component with all contacts fanned out, showing exposed contact pads and a sealing layer that protects conductive ink.

Surface-mount components with dimensions of 0.6 × 0.3 mm (0201 imperial) have demonstrated to be the minimum component size capable of reliable electrical interfacing, as shown in Fig. 6. The small footprint and compatibility with AM processes make these methods well suited for high-density designs. Additionally, 85/85 testing (85% relative humidity at 85 °C) for 1,000 hours was performed, demonstrating stable operation of embedded passive and active QFN components.

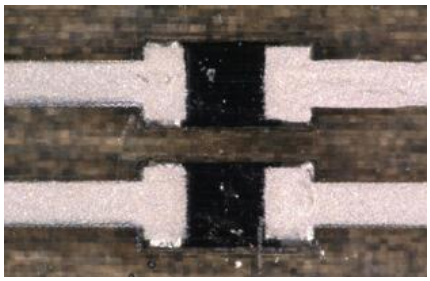


Fig. 6. Surface-mount components with dimensions of 0.6 × 0.3 mm (0201 imperial) embedded inside high-temperature resin.

### B. RF Structures

In modern packaging technologies, Antenna-in-Package (AiP) is a common approach for high-frequency RF systems, resulting in reduced on-board circuit complexity and improved RF performance. In addition to antennas, RF elements such as filters and metasurfaces are commonly integrated within the package to enhance functionality. For high-frequency AM applications, manufacturing antennas alongside RF ICs provides advantages in terms of size, performance, and simplified system design.

As shown in Fig. 7, the complete printed patch antenna array with an edge connector coax launch is demonstrated. The structure was fully fabricated in approximately 20 minutes, with three devices produced per batch. Because the same fabrication workflow is used for both RF structures and embedded component integration, IC integration can be directly combined with fully additive antenna fabrication. This enables the realization of AM monolithic AiP millimeter-wave module.

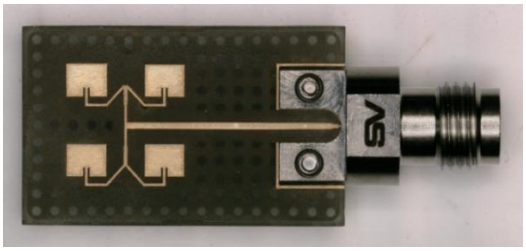


Fig. 7. Patch antenna array with edge connector mounted.

For printed RF structures, performance is strongly influenced by several factors, including conductor conductivity, surface roughness, dielectric thickness, feature resolution, and the ability to accurately realize impedance-matched geometries. As shown in Fig. 8, a small taper at the launch can be implemented due to the 27 µm resolution of the DLP printer. This high-resolution printing enables the fabrication of fine geometric features that improve RF performance. DLP-based AM also provides precise control over layer thickness and provides low surface roughness. Measured average surface roughness of conductive features measured below 1µm on the top surface.

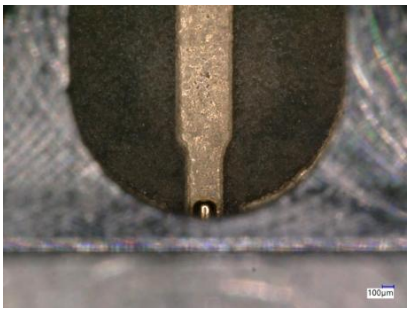


Fig. 8. Coax launch pin alignment and tapered transition used for impedance matching at the input.

Many RF applications require vias for grounding and signal routing. In this design, large vias were fabricated to provide mounting holes for the edge connector as well as electrical connections to the ground network. As shown in Fig. 9, the small scale of the overall antenna array is apparent, along with an X-ray scan highlighting the grounded mounting vias. Additional studies on the minimum feasible via diameter are required to determine practical fabrication limits and to enable reliable implementation of fenced and grounded RF via structures.

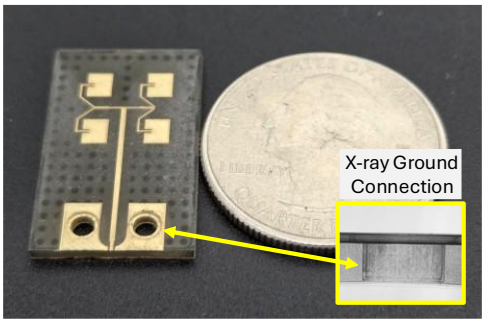



Fig. 9. Antenna array scale and X-ray visualization of grounded mounting vias

Angled features must also be smooth to ensure good RF performance. As shown in Fig. 10, angled geometries can be produced with sub-pixel resolution by implementing anti-aliasing during printing. This approach cures resin using gradient-intensity pixels, resulting in smoother sidewall features. Projected curing also enables the formation of sharp internal and external corners, which improves performance compared to traditional direct-write printing, where corner rounding is typically limited by the minimum printable line width.

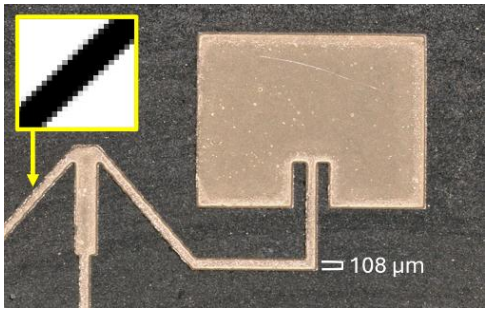



Fig. 10. Anti-aliased sub-pixel fabrication of smooth angled features and sharp corners for improved RF performance.

## C. *RF Performance*

Antenna array performance was simulated and experimentally characterized, as shown in Fig. 11. Three antennas were fabricated simultaneously using the batch manufacturing process and the antennas were measured in a free-space setup at boresight with absorber backing to minimize unwanted reflections. The measured resonant frequency closely matched the simulated results, with a deviation of less than 40 MHz from the simulated center frequency of 33.60 GHz, corresponding to a difference of only 0.12%.

Additionally, the measured bandwidth was wider than the simulated response, likely due to the higher conductivity of the fabricated metallization compared to the experimentally obtained silver conductivity used in the simulations. The measured -10 dB bandwidth was 1.5 GHz (4.5%), extending from approximately 32.8 to 34.3 GHz. In comparison, the simulated -10 dB bandwidth was 0.8 GHz (2.4%), spanning approximately 33.2 to 34.0 GHz.

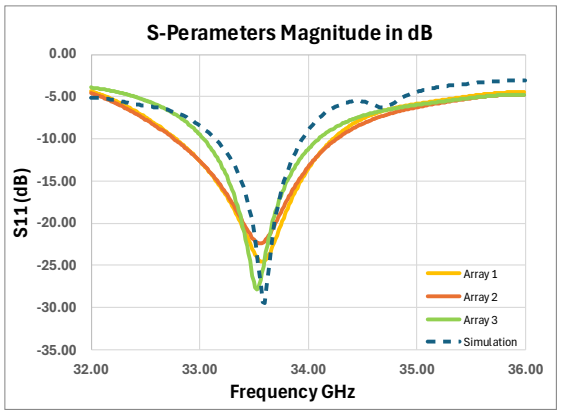



Fig. 11. Simulated and measured resonant frequency response of printed patch antenna array.

Boresight gain was measured and compared to simulation, showing a realized gain of approximately 11.8–12 dBi across the three fabricated samples, closely matching the simulated value of 12 dBi. This performance is consistent with the gain of a single simulated patch element (~6 dBi), with the 2×2 patch array providing an additional ~6 dB gain based on the array factor equation. The gain plot shows a wider bandwidth than the simulated response, as expected based on the reflection results.

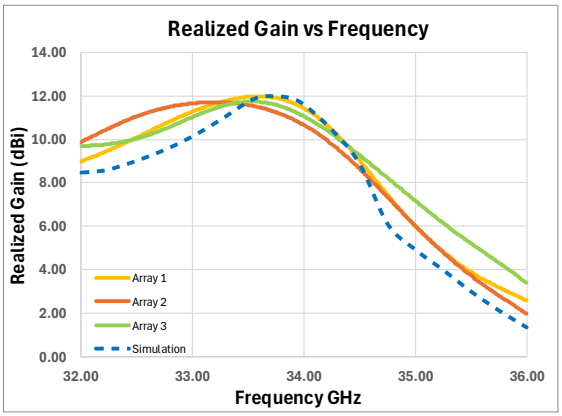



Fig. 12. Simulated and measured realized gain versus frequency of printed patch antenna array.

## IV. Discussion

The results demonstrate that DLP-based additive manufacturing can produce monolithic RF packages with performance comparable to conventional fabrication methods while enabling a high degree of design freedom. The measured resonant frequency differed by 0.12% from simulation, and the realized gain of 11.8–12 dBi closely matched the simulated performance, indicating excellent control of critical dimensions and material properties at millimeter-wave frequencies.

The process also enables fine tapered interconnects capable of interfacing with small-pitch contacts while supporting impedance-matched RF structures. Reliable electrical interfacing was demonstrated for passive components as small as 0201, and embedded passive and active QFN devices remained operational after 1,000 hours of 85/85 testing, demonstrating good environmental robustness and long-term reliability.

The projection-based nature of DLP printing provides precise layer thickness control, low surface roughness, and sub-pixel feature resolution, enabling high-performance RF structures and embedded components to be fabricated in a batch process. The workflow requires only a DLP printer, an airbrush-based metallization system, and a small milling tool, reducing dependence on specialized equipment, external vendors, and long manufacturing lead times. These characteristics make the process attractive for prototyping and field deployment in resource-constrained environments where rapid, on-demand fabrication of integrated RF systems is required.

## V. Conclusion

Additive manufacturing presents a promising future for high performance RF packaging. While traditional techniques remain superior in terms of maturity and scalability, AM offers unique advantages in material customization, rapid prototyping, and the integration of advanced functionalities. The ability to fabricate complex geometries, embed RF components, and incorporate conformal RF features within a package enables novel approaches for RF system design.

In addition to enabling the fabrication of conductive RF components, AM offers the capability to produce more complex electromagnetic structures, such as gradient-index (GRIN) materials for printed lenses [12], [13] and polarizers that enhance radiation patterns, impedance matching, and antenna isolation [14], [15]. Furthermore, AM facilitates the integration of internal cavities and channel-based architectures for thermal management and sensing applications.

The combination of research in materials science, RF engineering, and advanced manufacturing has shown potential for future benefits of additive electronic packaging. A wide range of methods have been researched and developed to optimize performance and form factors, applying various and unique capabilities of AM to take advantage of features not typically achievable with traditional manufacturing. Continued advancements in materials, process resolution, processing speeds, and integration strategies may promote AM to be a common complementary tool in advanced RF packaging.

## Acknowledgment

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