Plasma Dicing Innovations on Film Frame Carriers for High-Bandwidth Memory (HBM) and Heterogeneous Integration Devices

Simon Dawson (1), Janet Hopkins (1), Richard Barnett (1), Tejinder Singh (1), Ksenija Varga (2), Matthias Brunnbauer (2), Alois Malzer (2), Tobias Zenger (2)

(1) KLA Corporation UK Ltd
Celtic Lakes, Unit 3a Celtic Way,
Newport, NP10 8BE, United Kingdom
Ph: +44 1633 832500
Email: Tejinder.K.Singh@kla.com

(2) EV Group
DI Erich Thallner Strasse 1,
A-4782 St. Florian am Inn, Austria
Ph: +43 7712 5311 - 0
Email: K.Varga@EVGroup.com

Abstract

The rapid adoption of AI and high-bandwidth memory (HBM) is increasing the demands on die thinning, singulation quality, and hybrid bonding readiness. This paper demonstrates an integrated digital lithography and plasma dicing process on film frame carriers (FFCs) for advanced packaging and HBM applications. The flow combines spray-coated photoresist, maskless exposure, oxide and silicon plasma etching, and plasma resist stripping to enable precise 8 µm dicing streets on ultrathin wafers. A negative-tone resist achieved excellent coating uniformity (< 10%); plasma etching delivered clean sidewalls and straight etch profiles while maintaining an oxide etch rate of > 1 µm/min and a silicon etch rate of 10 µm/min. The demonstrated process provides a scalable, plasma-based singulation solution for future HBM, hybrid bonding, and heterogeneous integration architectures.

Keywords

Advanced packaging, digital lithography, film frame carriers, high-bandwidth memory, heterogeneous integration, hybrid bonding, plasma dicing, spray coating.

I. Introduction

The recent surge in AI technology and the demand for high-performance computing both require improvements in advanced packaging and high-bandwidth memory (HBM). Traditional 2D structures are now being replaced by 3D vertical stacks (Fig. 1), enabling much more efficient use of space and improving data transmission rates [1].

To overcome the total-stack-thickness limitation while continuing to advance device performance, dies must become thinner while maintaining high die strength, clean edges, and particle-free surfaces and sidewalls. These factors are especially important for hybrid bonding, where surface residues, particles, or defects can prevent core die structures from bonding successfully and achieving complete data transfer [2]. Therefore, the correct combination of patterning and dicing methods is required to enable these structures.

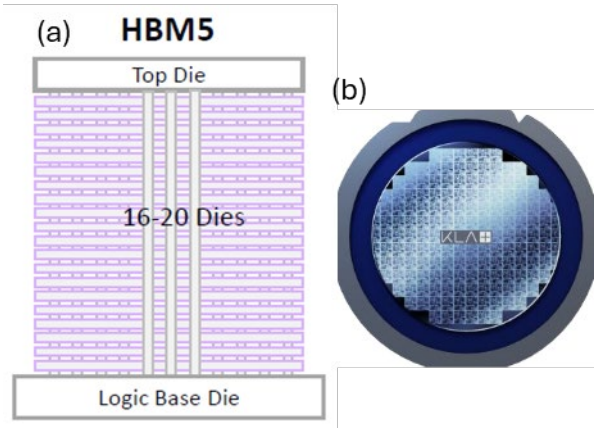


Fig. 1. (a) Illustration of an HBM 3D-stacked structure comprising top, core, and base dies fabricated from (b) 300 mm wafers mounted on FFCs.

Combined film frame carrier (FFC) masking and dicing is an ideal solution for preparing and handling ultrathin dies. Traditional photolithography has not yet been adapted to

FFC systems, primarily because of prohibitive cost [3]. FFC dicing has instead relied on methods such as laser grooving (LG), commonly used in dicing applications [4], to create mask patterns and groove through dielectric layers or non-plasma-etchable materials such as metals or test element groups (TEGs). However, laser grooving typically creates burrs when grooving through dielectrics and can cause delamination when stacks or thick layers are present (Fig. 2), potentially resulting in reduced yields or electrical shorting [5].

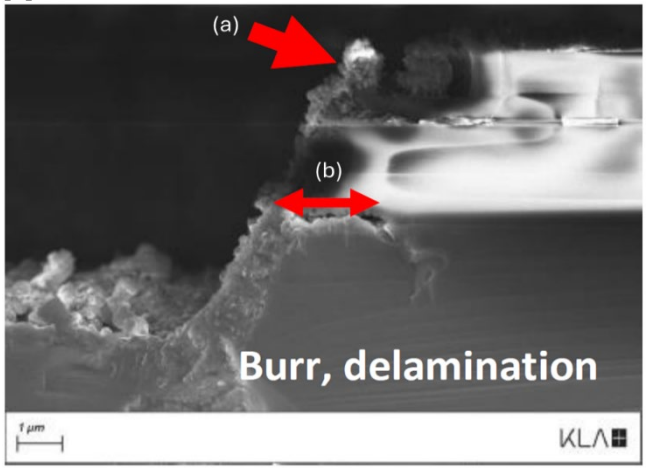


Fig. 2. (a) Burr formation caused by redeposition of recast material at the laser boundary and (b) lateral delamination damage in the dielectric stack, both resulting from laser grooving.

Mechanical dicing is not a viable option for HBM dies because wafers must be thinned to < 150 µm. When dicing such thin wafers, blade dicing is more likely to cause chipping, which reduces die strength and generates particle contamination [6], [7]. Although laser and stealth dicing perform better than mechanical dicing, these techniques typically create rough sidewalls and edge damage and have lower throughput than plasma dicing [8]. The time required for plasma etching through a wafer decreases as wafer thickness is reduced, whereas the processing time remains similar for serial laser processes.

This paper demonstrates the effectiveness of combining digital lithography patterning with plasma dicing and photoresist stripping, all performed on FFCs.

II. Methodology

A. Patterning

A key step in the dicing process is the spray coating of the photoresist. Compared with conventional spin coating, spray coating offers several advantages, including more precise resist deposition and superior coverage of wafers with pronounced surface topography [9]. This performance is achieved by high-precision ultrasonic spray nozzles that deposit the resist in a controlled meander pattern. As a result, a highly uniform distribution of fine resist droplets can be obtained across the wafer or die surface, as illustrated in Fig. 3.

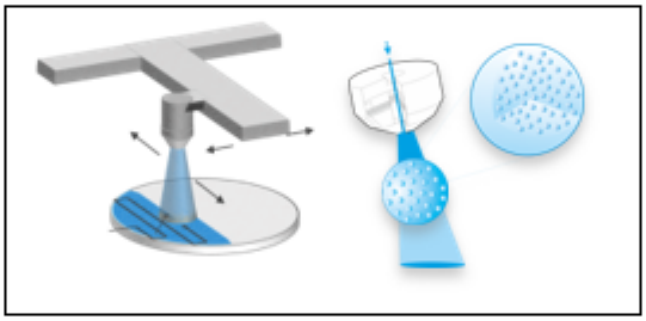


Fig. 3. Schematic of spray coating.

This technology provides excellent surface coverage and coating uniformity, even on substrates with significant topographical variations, while the versatility of spray coating makes it particularly suitable for advanced packaging and dicing applications.

Following spray coating with the various photoresist materials, the dies were patterned using a digital exposure system and subsequently developed. The digital lithography platform supports a wide range of advanced packaging applications. Compared with conventional mask-based exposure systems, digital lithography offers several significant advantages. By eliminating the need for photomasks, development cycles become more flexible, cost-effective, and responsive to design changes, making the technology particularly attractive for R&D and high-volume production. Furthermore, integrated focus–dose–exposure matrices enable efficient process optimization, achieving resolutions of < 2 µm L/S.

The exposure system (LITHOSCALE®) employs dual-wavelength light sources (375 nm and 405 nm), providing greater flexibility in material selection while offering a large depth of focus and advanced autofocus capabilities. In addition, sophisticated software features such as dynamic on-the-fly die annotation and die-shift compensation further enhance patterning accuracy and process robustness, reinforcing the advantages of the digital lithography approach [10].

In this work, a negative-tone resist (AZ 125nXT) was investigated for 8 µm dicing streets and a target film thickness of 15 µm.

B. Plasma Etching

Plasma dicing is a robust parallel process that can deliver high die strength [5], independent of die size and shape. Unlike traditional dicing methods, plasma dicing can securely handle and singulate ultrathin dies (≤ 30 µm)

without introducing chips, notches, or debris, thereby removing the need for additional die-strength enhancement processes.

Endpoint detection is extremely useful for both oxide and silicon etching processes to ensure complete etching of the relevant material with minimal over-etch into successive layers. This approach prevents lateral etching at the base of the die (notching) and potential sidewall damage caused by unnecessary additional processing time, thereby improving die strength and minimizing process time.

Plasma etching was performed in two KLA etch modules compatible with 400 mm film frame carriers. Extensive testing was performed in previous work [11] to ensure that tapes used for high-rate plasma etching did not degrade or lose adhesion during or after etching, deposit material on the dies, or interfere with subsequent pick-and-place steps. Chuck temperature was controlled in the etch chambers throughout all FFC processes to avoid potential thermal damage during high-rate etching.

C. Combined Process Flow

Fig. 4 illustrates the complete patterning and plasma etching process flow, from an incoming silicon wafer with a silicon dioxide (SiO_2) top layer to singulated dies.

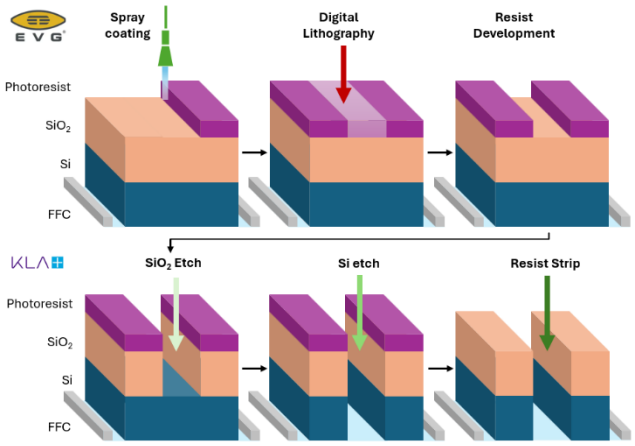


Fig. 4. Schematic process flow for patterning—spray coating, digital lithography, and resist development—and plasma etching—SiO_2 etching, Si etching, and resist stripping—of wafers mounted on FFCs.

III. Process Results

A. Resist Processing

For coating-uniformity measurements, each wafer was measured at 25 locations across its surface, excluding a 3 mm edge zone, using spectral reflectance. The instrument operates over a wavelength range of 200–1700 nm, with a spot size of up to 1.5 mm and a specified measurement accuracy of 0.2% or 2 nm. Spectral reflectance can be used to measure a broad range of planar film thicknesses and materials, including dielectric films.

The negative-tone resist exhibited a film thickness of 16 µm after spray coating, which decreased marginally to 15 µm following exposure and development (Fig. 5). Excellent coating uniformity (< 10%) was achieved, yielding a smooth and continuous resist layer without observable irregularities.

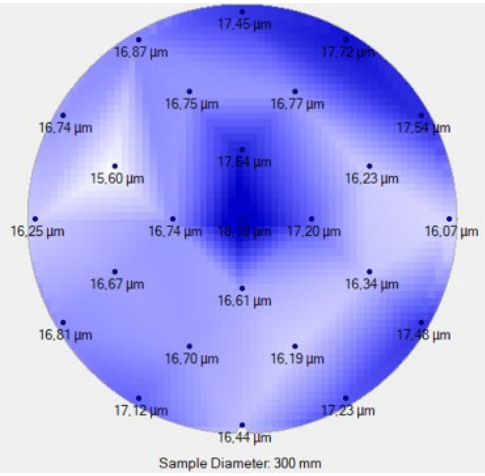


Fig. 5. Uniformity map of negative-tone resist.

B. Plasma Etching

Silicon dioxide etching was performed in a novel etch module designed for high-power, high-rate dielectric etching of 300 mm wafers mounted on FFCs. Multiple gas-injection inlets and a high-ion-density plasma enable a uniform plasma distribution that readily etches dielectric material. An etch rate exceeding 1 µm/min was achieved across the wafer, with a resist-to-SiO_2 selectivity of 1:1, while maintaining a smooth, clean etch front. Tests (Fig. 6) showed consistent profiles after SiO_2 etching, with sidewall angles between 80° and 82° and a thin deposition layer on the sidewalls that was removed during subsequent etching steps.

Silicon etching was performed using the Bosch process in an SPTS Rapier-S module from KLA. This chamber can achieve complete die singulation for wafers with thicknesses ranging from 30 to 750 µm. In this case, a 30 µm partial etch was performed at an etch rate of 10 µm/min and a resist-to-Si selectivity of > 60:1. The process produced a clean, vertical sidewall profile with minimal undercut following silicon etching.

Plasma photoresist stripping was performed in the Rapier-S module at a strip rate of > 0.8 µm/min. This process completely removed the photoresist from the SiO_2 surface and sidewalls, leaving a clean surface suitable for subsequent bonding steps (Fig. 7).

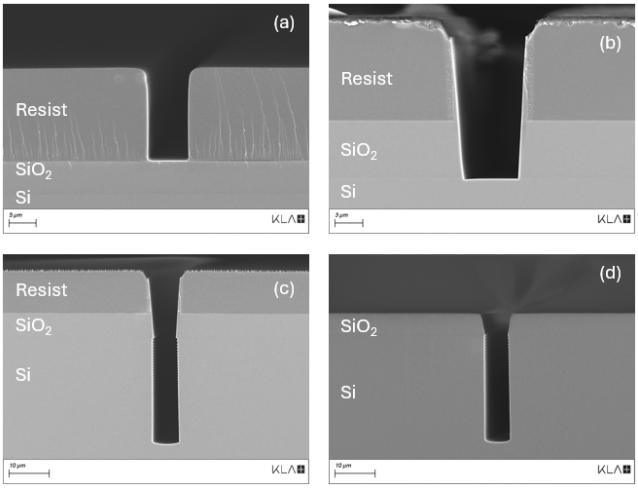


Fig. 6. SEM images showing (a) the incoming wafer, (b) the wafer after SiO_2 etching, (c) the wafer after silicon etching, and (d) the wafer after photoresist stripping.

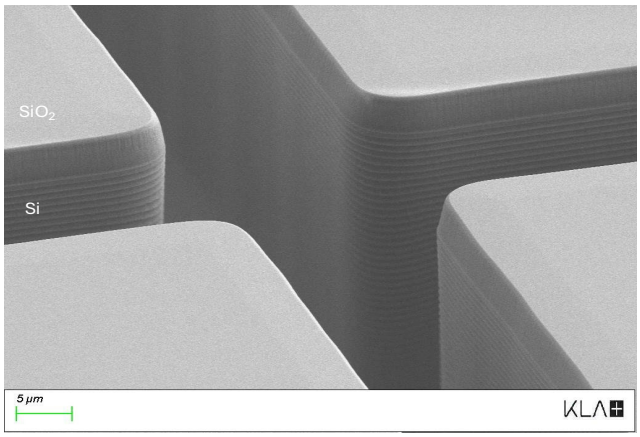


Fig. 7. SEM image at a dicing-street intersection showing a clean SiO_2 top surface after photoresist stripping and well-defined silicon sidewall scallops.

IV. Conclusion

The results presented in this study demonstrate that digital-lithography-enabled plasma dicing is a viable and scalable singulation solution for advanced packaging technologies.

By overcoming key limitations of conventional mechanical and laser-based singulation methods, the proposed approach offers a pathway toward realizing increasingly demanding package architectures, including HBM and future heterogeneous integration platforms for logic devices.

Ongoing development efforts will target enhanced dicing-profile designs and edge-shaping strategies to further improve die strength and package reliability.

The demonstrated cross-industry collaboration underscores the commitment of the semiconductor ecosystem to delivering the manufacturing innovations needed for next-generation AI and HPC devices.

Acknowledgment

We would like to acknowledge the KLA UK team and the EV Group for their support in this collaborative effort.

References

[1] D. Lee, S. Ghose, G. Pekhimenko, S. Khan, and O. Mutlu, "Simultaneous multi-layer access: Improving 3D-stacked memory bandwidth at low cost," *ACM Trans. Archit. Code Optim.*, vol. 12, pp. 1–29, Jan. 2016.

[2] Z. Lian *et al.*, "Suppressing plasma-induced particulate contamination in die-to-wafer hybrid bonding via highly cross-linked and stable UV tape," *Materials Science in Semiconductor Processing*, vol. 210, 110664, Aug. 2026.

[3] A. A. Kryuchyn *et al.*, "And there was light: Prospects for the creation of micro- and nanostructures through maskless photolithography," *ACS Nano*, vol. 11, no. 9, pp. 8537–8541, Sept. 2017.

[4] R. Evertsen *et al.*, "Novel UV-USP laser grooving and plasma dicing separation schemes for next-generation advanced packaging," IEEE 27th Electronics Packaging Technology Conference (EPTC), Singapore, pp. 1–5, Dec. 2025.

[5] W. S. Lei, A. Kumar, and R. Yalamanchili, "Die singulation technologies for advanced packaging: A critical review," J. Vac. Sci. Technol. B, vol. 30, no. 4, 040801, July 2012.

[6] R. Barnett, O. Ansell, and D. Thomas, "Considerations and benefits of plasma-etch-based wafer dicing," *IEEE 15th Electronics Packaging Technology Conference (EPTC)*, pp. 569–574, Dec. 2013.

[7] R. Westerman, G. Grivna, K. Mackenzie, T. Lazerand, and J. Doub, "Plasma dicing: Current state and future trends," *ECS Trans.*, vol. 69, no. 3, 2015.

[8] G. H. See *et al.*, "Enabling beyond-16-layer 3D stacking with ultrathin die hybrid bonding with integrated bonder," *IEEE 76th Electronic Components and Technology Conference (ECTC)*, pp. 1359–1362, May 2026.

[9] J. Rimböck, J. Holzapfel, L. Bouvot, M. Brunnbauer, and T. Zenger, "Ultrasonic spray coating combined with maskless lithography for advanced singulation of wafers with complex bump geometry," *Proc. SPIE*, vol. 13983, Apr. 2026.

[10] A. Malzer, K. Varga, M. Weinhart, A. Spitzer, and T. Zenger, "Lithography digitalization in semiconductor technologies through advanced software development of high-throughput maskless exposure," *Proc. SPIE*, vol. 13982, Apr. 2026.

[11] H. Fulton *et al.*, "A study of integrated circuit dicing tape when used in a plasma dicing environment," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 4, pp. 694–703, Jan. 2020.