Pioneering Bottom-Up Copper Plating: Advanced Pillar-Like Metallization for High Aspect Ratio Through Glass Vias

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Abstract

In integrated circuit substrates (ICS), core thickness is increasing to control warpage and ensure mechanical stability as package sizes, layer counts, and copper density rise—especially for AI and high-performance computing applications.

This paper presents a different approach to filling high aspect ratio (AR) features with electrolytically deposited copper, referred to as bottom-up-filling (BUF). This approach, while still in development, is highly flexible and can fill a variety of feature sizes and aspect ratios. This process can be used with either organic or glass core boards and has been effective at filling both straight (mechanically drilled) and hourglass shaped (laser drilled) through holes.

The BUF system offers numerous advantages over traditional through hole filling methods. As an entirely direct current (DC) electrolytic metallization process, it eliminates the need for costly periodic pulse reverse (PPR) rectifiers and complex waveform engineering. Features are filled from one side, ensuring void-free through holes that are completely filled. Additionally, the BUF process removes the requirement for primary metallization inside the features, streamlining manufacturing by eliminating a difficult step for high AR through holes. BUF also overcomes common bottlenecks associated with seed layers, such as poor coverage and adhesion issues typically encountered with existing physical vapor deposition (PVD) and electroless primary metallization processes.

The BUF approach is not without its challenges. The process is still in development, and our group is partnering with many stakeholders to drive this innovation. In this paper, we discuss many of those challenges, how to overcome them, and the benefits we see by utilizing this approach.

Key words

Artificial intelligence (AI), electrolytic copper, glass core, high density interconnects, high performance computing, integrated circuit substrates

I. Introduction

Integrated circuit substrates (ICS) are the connection between semiconductor chips and the printed circuit boards (PCBs), which are designed at drastically different scales. They also function as a stable base for the overall chip package, playing a critical role in protecting and supporting the chips inside the package as well as providing connectivity between the packaged chips and the PCB. In general, ICS contain higher densities of features, whether that be through holes, lines, pads, or vias, with stricter requirements on the uniformity of each layer.

Devices specifically designed for artificial intelligence (AI) or machine learning (ML) applications are particularly demanding and have pushed manufacturers to make significant advancements in the design and fabrication of all aspects of advanced IC packages [1]. Innovation in front end fabrication is necessary to drive higher performance from devices, though packaging issues are becoming more significant as feature density, power requirements, and heat generation increase [2].

Uniformity requirements and heat management are key factors driving material selection for ICS. In particular, the coefficient of thermal expansion (CTE) mismatch between silicon dies and organic substrates lead to increased warpage, causing process and reliability issues, poor yields in manufacturing, and package failures.

To address these issues, designers are creating thicker core substrates and exploring alternative core materials, like

glass. Glass cores offer benefits such as greater stiffness, better dimensional stability, low dielectric loss, smoother surfaces, panel level processability, and a CTE closer to silicon at reduced thicknesses [3]-[5].

Thicker organic cores provide greater stiffness, reducing deformation during lamination, reflow, and thermal cycling, while improving manufacturability, yield, and reliability, thus enabling higher current delivery through thicker power planes. Although thicker organic cores introduce electrical penalties, such as longer vias and higher inductance, mechanical stability is currently a higher priority than Z-direction electrical optimization. Thick core organic substrates remain the dominant solution until glass core technology matures at scale.

While the thickness of organic cores are increasing, the number and density of through hole (TH) features is also becoming more challenging. Increasing the density of these features and the thickness of the core means the aspect ratios of these features continue to increase, often exceeding 10:1. There are a variety of ways to fill these features, but the periodic pulse reverse (PPR) plating techniques currently used to fill features are nearing their limits due to increasingly challenging geometries and designs. Furthermore, a method that will fill a 6:1 aspect ratio TH, will not necessarily fill a 10:1 aspect ratio TH when using a bridge-and-fill method. This requires constant innovation by teams, manipulating plating parameters and waveform development each time the feature geometry changes [6], [7]. In addition, non-homogeneous distributions of THs across a board can result in successful bridging in one environment, while other THs see no bridging at all, or bridging and pinching.

The combination of these challenges has led companies to seek alternatives to bridge-and-fill processes for filling THs, which are a critical feature for dissipating heat. The process presented in this paper aims to fill these types of features in a variety of densities, aspect ratios, and plating tools.

A typical method for filling THs with electrolytic copper has been to use PPR rectifiers with specially tuned waveforms to form a bridge inside the THs, then switch to a DC cycle to initiate a via fill type of mechanism [7], as shown in Fig. 1. This approach requires specific additives, rectifiers, and waveforms to be successful. A common challenge is the formation of voids within the TH during either the bridging step or the filling step. Cross sections of both defects may be seen in Fig. 2.

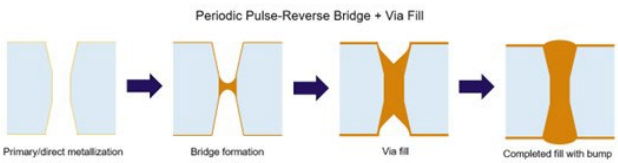


Figure 1: Bridge and fill process for filling TH features.

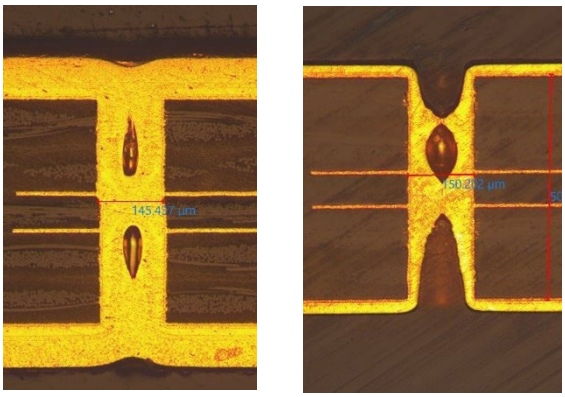


Figure 2: The formation of common defects in bridge and fill processes. (a) The image on the left shows the cross section of a TH that formed voids during the DC filling step. (b) The image on the right is an example of double bridging, where the void is formed during the bridging step.

These issues have been known in PPR applications for many years and teams have developed ways to mitigate them with incremental improvements and modifications to waveforms. However, the rapid and drastic changes that ICS are going through make it impossible to plate them effectively with standard methods. Fig. 3 shows THs with much higher aspect ratios and varying pitches on the same board. This board design makes it far more difficult to form effective bridges in all features at the same time, resulting in inconsistent feature filling.

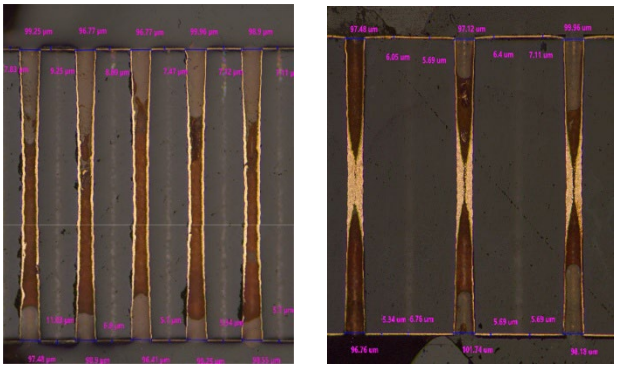


Figure 3: Through holes with varying pitch. Aspect ratio is around 10:1.

The bottom-up-filling (BUF) approach is different from the typical bridge-and-fill process in multiple ways. Starting with the primary metallization step, which must only be deposited on one side, with no deposition into the feature. Ideally, one side of the TH is sealed by the conductive layer of Cu, allowing for one sided copper plating, as demonstrated in Fig. 4. This makes the plating more similar to pillar or stud plating than a bridge-and-fill or via filling process. This approach is far simpler, relying only on DC

plating, and can be used with either organic or glass core boards. But it is not without its own challenges.

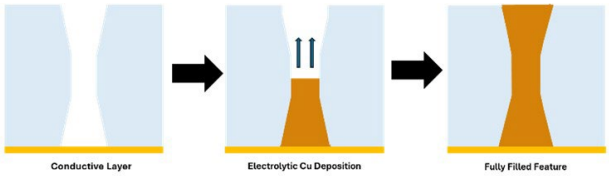


Figure 4: Schematic representation of BUF of laser drilled TH.

The BUF approach is similar to pillar plating, but with extreme feature sizes and filling of the features inside the core of the board. The concept is simple, and has been used in other applications [8], but is particularly challenging to accomplish in an ICS application.

II. Experimental

A. Plating Equipment/Sample Preparation

Samples were prepared for plating by utilizing thorough cleaning and degassing steps in both sonication and vacuum tanks. The vacuum step was conducted in a Vevor vacuum tank, model T5 with a KQ-1K pump. Multiple cleaning solutions were utilized to remove organic and inorganic contaminants on the primary metallization layer.

Plating was conducted in two types of plating tools: an eductor-type tank and a tool with shear-type agitation. The eductor tank is a typical laboratory tool that is used to replicate the performance of vertical continuous platers (VCP). The shear-type agitation tank is a small-scale version of the ASMPT-NEXX P500 plating tool. Both tools are shown in Fig. 5.

Plating baths consisted of acid copper electrolytes and proprietary additives that controlled the deposition of copper in the features. These additives include accelerators that help refine grain structure and suppressors that inhibit uncontrolled deposition. Electroplating was conducted using a KiPrim DC 310S rectifier (30V/10A/300W).

Substrates were provided by commercial partners and consisted of various feature geometries as well as feature densities. Both glass and organic core boards were plated.

B. Sample evaluation

Samples were evaluated by cross section/optical microscopy using a Keyence VHX-x1 optical microscope. Samples were also evaluated for voids using a Nordson/Dage Quadra 7 with Gensys x-ray software.

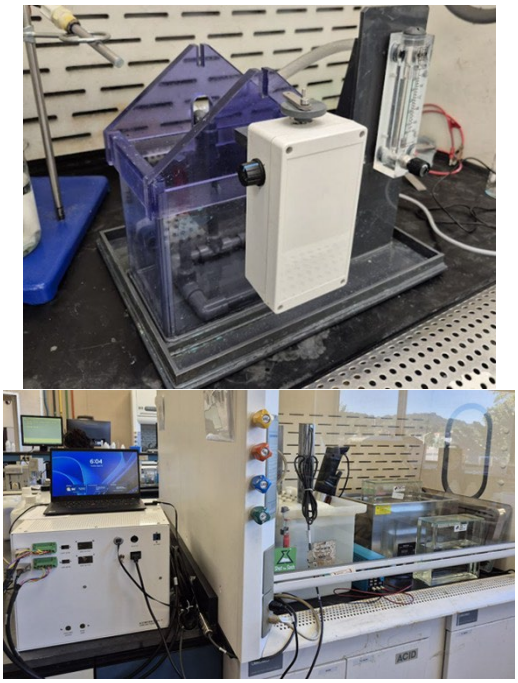


Figure 5: (a) A 3.5L eductor tank (above) and (b) an ASMPT laboratory scale shear agitation tool (below).

III. Results & Discussion

Filled TH features were plated using a proprietary electrolyte with varying degrees of success, depending on multiple factors during the plating process. Challenges primarily consisted of three defects: skip plating, void formation, and inconsistent distribution of deposited Cu.

Skip Plating:

This defect was characterized by features that were devoid of any electrolytic Cu. An example of skip plating is shown in Fig. 6.

A skip plating defect was a single feature, or a small group of features in a cluster had no electrolytically deposited Cu. This was distinctly different than features that were plated, but with lower Cu thickness than other nearby THs. Skip plating was attributed to local areas of poor conductivity during electroplating or poor substrate preparation. This was likely due to copper oxide formation at the bottoms of features or another contamination that was not removed during the cleaning procedure. Excessive cleaning or local damage to the primary metallization layer could also induce skip defects. Therefore, meticulous sample preparation was critical.

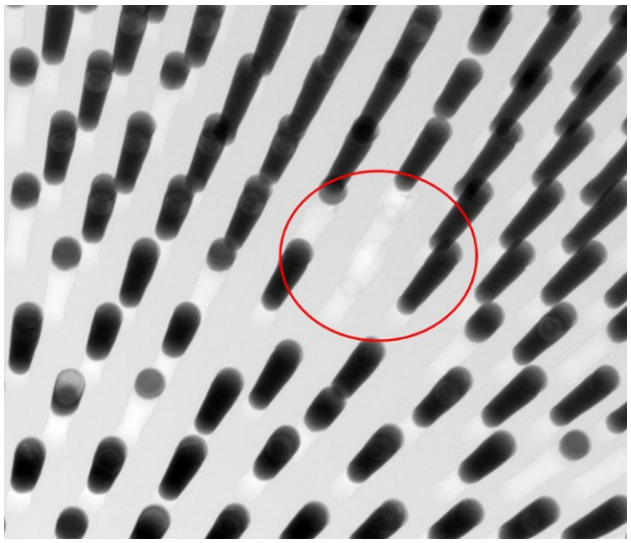


Figure 6: X-ray image of skip plating in a dense feature area. The skipped features are completely devoid of any electrolytic Cu.

Void Formation:

The formation of voids in the filled TH is a critical defect that must be prevented, and we observed multiple mechanisms that lead to voids forming at various points in the TH feature.

The first was the formation of voids at the very bottoms of the features. Although the void closed and became visible after the electrolytic Cu step, we have determined the source of these voids was from feature formation or depositing the conductive layer at the bottoms of the features.

In the case where the conductive base layer was deposited first, then mechanically drilled, the drilling process left tiny amounts of conductive material on the inside of the TH, just enough to allow electroplating to occur above the bottom of the feature. This started as, what appeared to be, nodule growth, until the TH was blocked off, sealing the void at the bottom. The feature then continued to fill normally. Fig. 7 shows a schematic representation of this void formation mechanism.

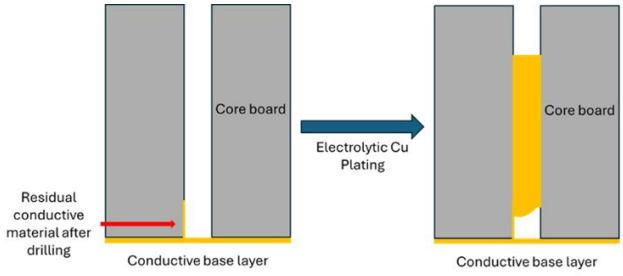


Figure 7: Void formation mechanism of mechanically drilled THs.

The second void formation mechanism observed occurred in features that were laser drilled followed by physical vapor deposition (PVD) of the primary metallization layer. In this approach, the conductive layer extended into the TH features, again creating a point for electroplating to occur above the bottom of the feature. The electroplated Cu initiated from the top of the primary metallization inside the TH and sealed a void in the bottom of the feature. In order for the BUF process to be successful, it is critical that there are no conductive elements inside the THs.

Inconsistent Distribution of Cu:

Even distribution of Cu across a coupon was a consistent challenge through every experiment and was improved through organic additive optimization and process improvement. In particular, the regions of test vehicles with high feature density vs. low feature density always had the greatest difference in Cu thickness. Further, once features plated above the top of the TH, they formed domes, which thieved most of the additional current, thus exacerbating the difference between under- and over-plated features. A cross-sectional image of an over-plated feature is shown in Fig. 8. A certain level of over-plating is acceptable, particularly with glass core boards, which are planarized with chemical mechanical polishing (CMP) after Cu electroplating. The acceptable level of Cu overburden varied between substrate design. In Fig. 9, an example measurement is shown where the overburden was measured using a Keyence profilometer.

Utilizing a plating tool that produced uniform solution movement across the surface of the sample, and uniform current distribution, drastically improved the plating uniformity when compared to a typical VCP type plating cell. For example, a sample was plated with a VCP type tool had Cu overburden variation exceeding 600 µm, whereas the same sample plated in the shear type tool only had variation of 150 µm.

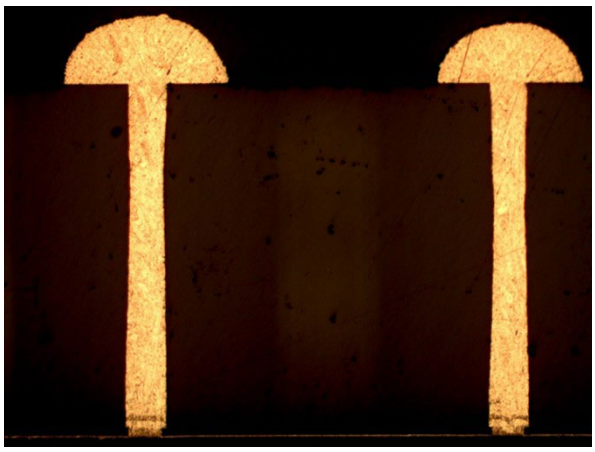


Figure 8: Cross section of multiple filled THs that have been over-plated. Note the domed tops are plated above the surface of the substrate.

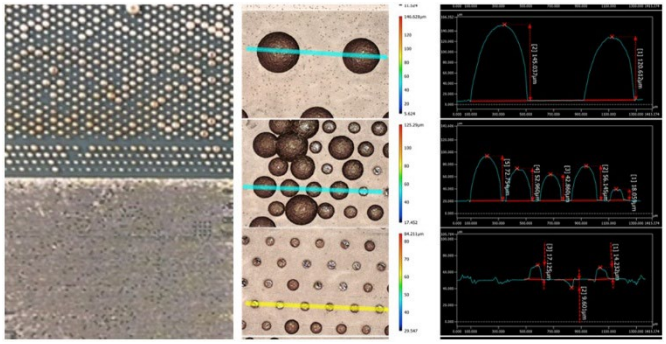


Figure 9: Example profile measurement of Cu overburden. The left part of the figure is a low magnification image of a plated sample, with isolated features in the top half and dense features in the bottom half. The right half of the figure is the profile measurements of the isolated and dense areas.

Conclusion

The BUF process discussed in this paper is in development with various partners and there have been significant improvements made in producing fully filled mechanically drilled and laser drilled THs without voids. Examples of successfully filled THs are shown in Fig. 10. Initially, samples were plated over 24 hours to obtain the best results, but the plating time has been driven down through solution and process optimization to fill 8:1 THs in less than 12 hours.

At this time, coupon level tests have been conducted (coupon maximum size 7 cm x 7 cm) on glass and organic substrates, with panel level testing to begin in the coming months. Panel level testing will present new challenges, particularly when it comes to uniformity control, though the insights from the coupon level testing will aid in the problem-solving process. Ultimately, this conceptual process has shown great results thus far and has enabled filling of features that could not be plated using traditional bridge-and-fill methods. MacDermid Alpha currently has a patent pending related to the BUF process.

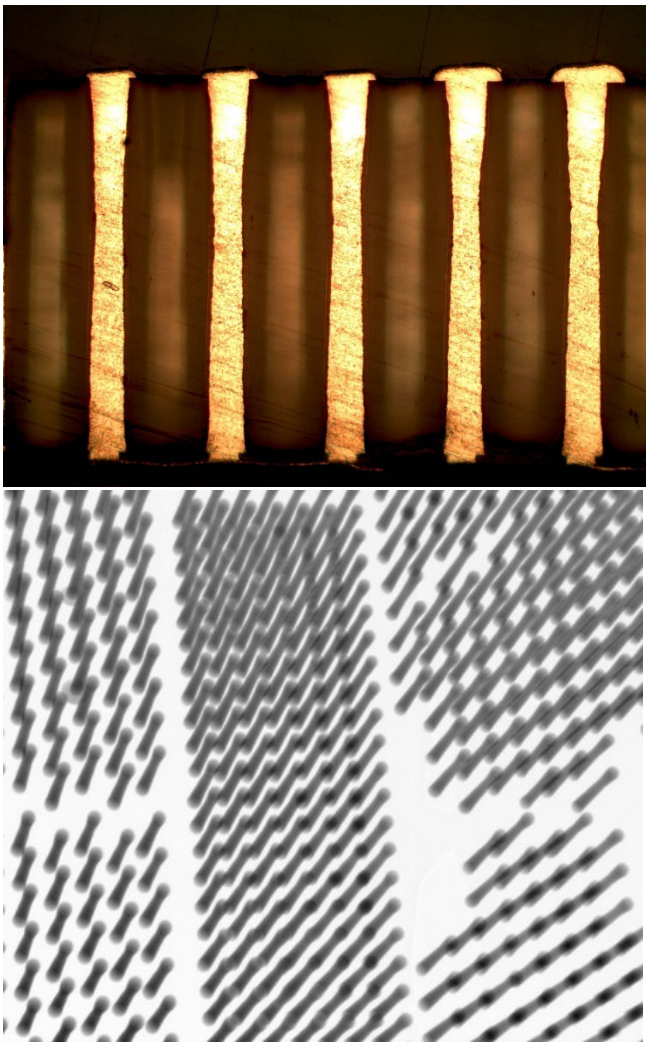


Figure 10: (a) Cross section of fully filled THs with slight over-plating (above). (b) X-ray image of void-free filled THs in a high-density area (below).

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