Advancing Panel-Level Fan-Out Technologies for High-Frequency and Power Devices through Alternative Through-Package Interconnects

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1 Abstract

Future communication, radar, and power management systems require semiconductor components that deliver higher performance, smaller footprints, and lower manufacturing costs. The ongoing transition within the semiconductor industry from wire and clip bonding and wafer-level packaging toward fan-out panel-level packaging (FOPLP) is largely driven by these requirements and by the improved area utilization offered by panel-level manufacturing compared with the maximum 300mm (12-inch) wafer format.

For heterogeneous integration (HI) of multiple components and functions at the panel level, laser drilling is the conventional method used to create three-dimensional vertical interconnects. However, for large panel formats containing an increasing number of high-resolution interconnects, this serial laser-drilling process becomes time-consuming and requires substantial capital investment.

This paper presents two complementary advanced FOPLP technologies based on alternative *vertical through-package interconnect* solutions targeting higher manufacturing throughput, cost-reduction potential, and sustainability benefits:

- *High-aspect-ratio* interconnects formed by conductive polymer pillars fabricated using semi-additive lithographic processing before embedding in an epoxy encapsulant.

- *Lower-resolution* vertical interconnects fabricated using fully additive printing techniques combined with copper electroplating.

This paper concludes with an overview table comparing capabilities and status of these two alternative panel-level fan-out technologies versus conventional FOPLP manufacturing processes, together with an outlook on future development and targeted technology improvements.

Keywords - FOPLP, fan-out, panel-level packaging, additive manufacturing, through-package via (TPV), through-mold via (TMV), vertical interconnects, redistribution layer (RDL), RF, 6G, EMI shielding, discrete power, thin film processing, printed electronics

2 Introduction

Rapid advances in future 6G communications, next-generation radar technologies, and power management applications are driving demand for semiconductor components that provide higher performance, smaller form factors, and lower cost while operating within increasingly complex electronic systems.

Conventional integrated systems, particularly RF components implemented on printed circuit boards (PCBs), present significant limitations in both size and high-frequency (HF) performance. These limitations are primarily caused by interconnection losses, differences in coefficients of thermal expansion (CTE), and manufacturing tolerances that become increasingly critical at millimeter-wave frequencies above 100GHz within D-band spectrum.

For more efficient power management, smaller device footprints and the integration of wide-bandgap (WBG) semiconductor technologies, such as silicon carbide (SiC) and gallium nitride (GaN), are essential.

These WBG materials enable operation at higher temperatures and power densities than conventional silicon (Si) technologies.

Most copper leadframe-based MOSFET power devices still rely on lead-containing solder for die and clip attachment, despite restrictions on lead use in many other electronic applications for more than 25 years in the meantime.

The semiconductor industry is therefore actively pursuing replacement technologies based on silver and copper sintering to satisfy increasingly demanding automotive reliability requirements while supporting the adoption of SiC and GaN devices [1]. Ideally, these alternatives should also achieve comparable or lower manufacturing costs.

The transition from conventional wire- and clip-bonded packaging toward fan-out panel-level packaging (FOPLP) is largely driven by the potential for lower overall manufacturing costs through improved area utilization. Compared with wafer-level processing, panel-level manufacturing offers significantly larger usable processing areas while also providing environmental benefits, including reduced material waste and a lower carbon footprint [2].

For heterogeneous integration at the panel level, laser drilling remains the conventional method for forming vertical interconnects between chips, interposers, redistribution layers (RDLs), and external connections. However, as panel size and interconnect density increase, this serial process limits production throughput and requires substantial capital investment.

This paper presents two advancing FOPLP technologies based on alternative vertical through-package interconnect concepts:

- Panel-level RF system integration using high-aspect-ratio (HAR) vias and coaxial shielding structures to improve high-frequency performance with cost-reduction potential.

- Fully additive fan-out panel-level packaging for discrete power devices using printed cavities and seed layers plus copper plating to achieve significant cost-reduction potential and lead-free solution.

3 Panel level RF system integration

3.1 State-of-the-art (SOTA)

The combination of fine-pitch interconnects, high I/O density, and high-aspect-ratio (HAR) vias makes vertical interconnect technology a key enabler for package miniaturization, three-dimensional integration of fan-out devices, and high-performance RF systems operating beyond 100GHz.

Compared with traditional wire bonding, these HAR vertical interconnects provide a significantly shorter electrical path (typically defined by the dielectric layer thickness), reducing parasitic inductance and associated signal degradation at high frequencies.

Same vertical interconnect technology can also be implemented for shielding structures that mitigate electromagnetic interference (EMI) and support chip-to-antenna connections in antenna-in-package (AiP) architectures [3].

Integration of vertical interconnects in conventional FOPLP packages is mostly based on standard printed circuit board (PCB) laser-drilling processes known as through-mold via (TMV) after typical compression molding process to make the panel (using epoxy mold compound or EMC). The aspect ratio (AR, height divided by diameter) of such drilled vias is typically limited to ~1 by insufficient copper plating quality at the bottom of the vias.

The fabrication of HAR vertical interconnects using through-package via (TPV) approach [4] will be presented in next section. Instead of laser drilling and via plating, first vertical interconnect pillars are formed and then embedded in a dielectric layer (typically epoxy resin based), in combination with FOPLP process.

This TPV technology has many advantages compared to most common laser-drilled TMVs in panels, such as higher AR and density, better sidewall quality and control, faster metallization process due to conformal seed layer, plus cost reduction potential by large-scale parallel fabrication based on lithography process.

The FOPLP fabrication on 352x320mm panel size (‘Gen1’, originated from display production), including TPVs with HAR of ~8 and height ranging from 50µm to 800µm will be described in detail, and is compatible with mainstream FOPLP processes.

Such taller structures, which to the authors' best knowledge represent state-of-the-art technology, can be used for instance as replacement of solder balls to increase the density of interconnects and or EMI shielding structures.

3.2 Fabrication process

Most used process options for FOPLP range from 'chip first', with 'face-up' and 'face-down' configurations, to 'RDL first' processes [2]. For RF applications operating above 100GHz, 'chip first, face-down, RDL last' approach is chosen. This provides the shortest interconnects, with only copper plated vias for the chip connection, which is most beneficial to reduce HF signal losses.

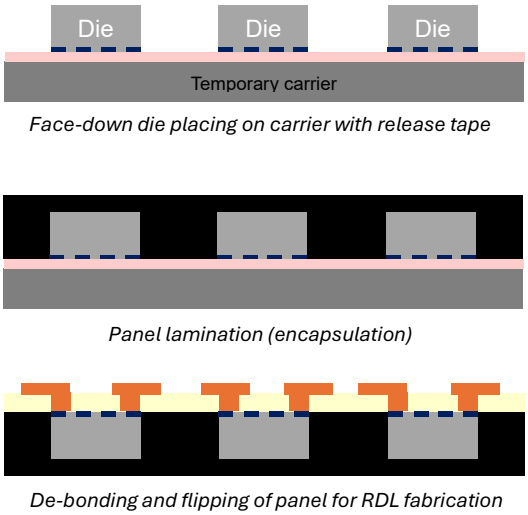


Figure 1: Schematic of the 'chip-first, face down' fan-out process flow including 'RDL last'.

The fan-out packaging process flow, as shown above in Figure 1, starts with face-down die placement on a temporary glass carrier (352x320mm^2) with thermal release tape (Revalpha from Nitto Denko) on both sides. For placement of these 5x5mm^2 dummy dies with 5mm die-to-die spacing, a Datacon 2200 Evo Plus die bonder was used. The result with 675 dies in 25x27 matrix is shown in Figure 2.

The encapsulation of the reconfigured panel is performed by vacuum lamination of epoxy-based dry films (Cellfil from Taiyo) using a 2-step process.

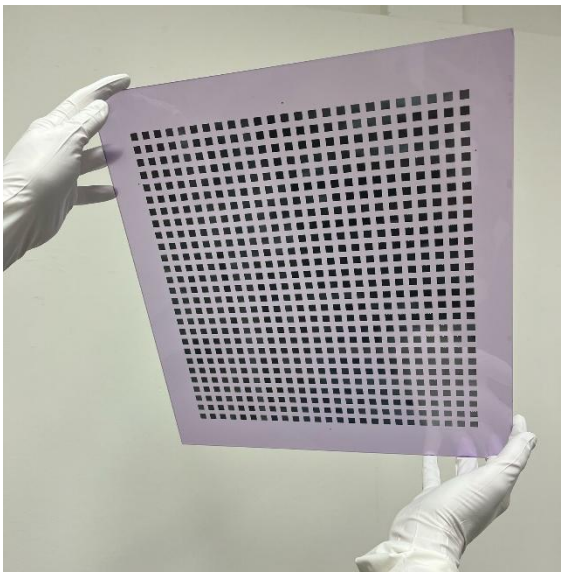


Figure 2: Photo of a Gen1 size glass panel after pick-and-place of 675 dies on thermal release layer.

During the first step (at 100°C, with vacuum for >10 minutes and 0.1MPa pressure for 1 minute), the dry film flows and encapsulates the dies. The second 'flattening step' (same 100°C with higher pressure) allows the surface of the epoxy film to become more even on panel level.

After this lamination process, the encapsulated panel is de-bonded from the temporary carrier, followed by a final 'post mold cure' process at 180°C for 1 hour.

As next step, the top side redistribution layer (RDL) is applied using semi-additive process with a photosensitive dielectric layer of polybenzoxazole (PBO) and plated copper (Cu). Patterning of the PBO-layer and Cu-traces is performed by a maskless aligner (MLA150 from Heidelberg Instruments Mikrotechnik GmbH) after adapting the layout to the real die position measured after lamination and curing. Metallization is applied using a sputtered titanium/copper (~100nm/200nm Ti/Cu) seed layer deposition followed by Cu-electroplating. Final package singulation is done by laser or blade dicing, resulting in 675 single components.

The main process steps to create high-aspect-ratio (HAR) through-package vias (TPVs) are shown in Figure 3 and described on the next page. This TPV process can also be performed after die placement, and prior to encapsulation (by lamination or molding) in a standard FOPLP process.

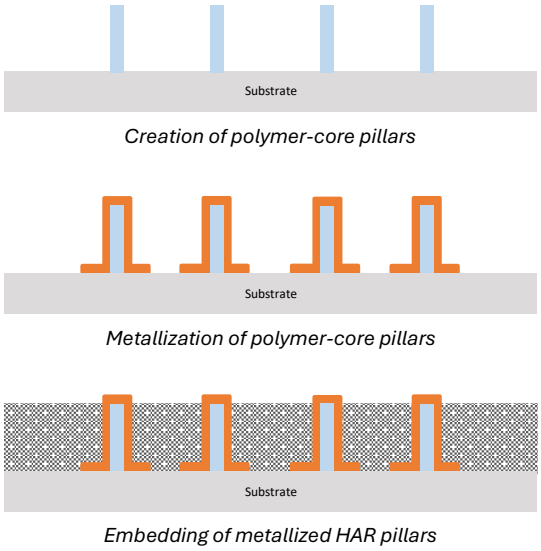


Figure 3: Schematic of HAR TPV fabrication process.

First, a 6" temporary glass carrier is coated with SUEX dry film photoresist. After lamination and soft bake, this photoresist layer is patterned via lithography to form the high-aspect-ratio polymer-core pillars.

After hard baking and an oxygen-plasma step (to improve metal seed layer adhesion to the pillars' surface), a Ti/Cu (~100nm/200nm) seed layer is applied by sputtering process. A second lithography step defining the pillar areas to be metallized, followed by ~5µm Cu plating, finishes this HAR TPV fabrication process.

Figure 4 below shows a FIB-SEM cross-section image of the conductive TPV pillar after Cu plating, in which the polymer core (SUEX) and the Cu-metal shell are clearly visible.

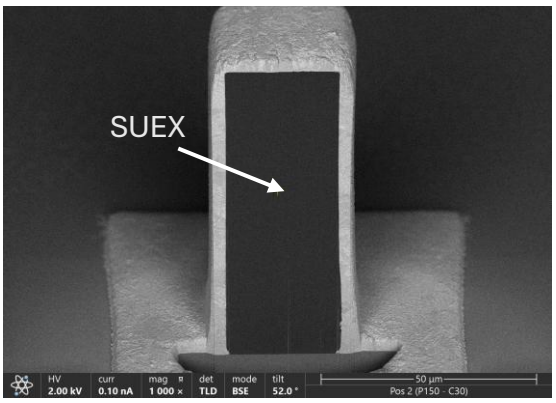


Figure 4: FIB-SEM cross-section image of a HAR TPV showing its polymer-core structure and Cu-metal shell.

Finally, a vacuum lamination step with epoxy-based build-up films is performed to encapsulate (embed) the TPVs. This can also be done by compression molding with EMC in liquid, granular or film form.

3.3 Experimental results

The result of the Gen1-size fan-out panel is shown in Figure 5 together with SEM cross-section images of the total stack. Thickness of the Cu-lines in the RDL is ~5µm with a 40nm average roughness. This is below the 100nm skin depth of Cu at 100GHz. Meeting this requirement is key for best RF performance since the roughness of the Cu-surface influences the loss of signal transmission, especially in high-frequency range >100GHz.

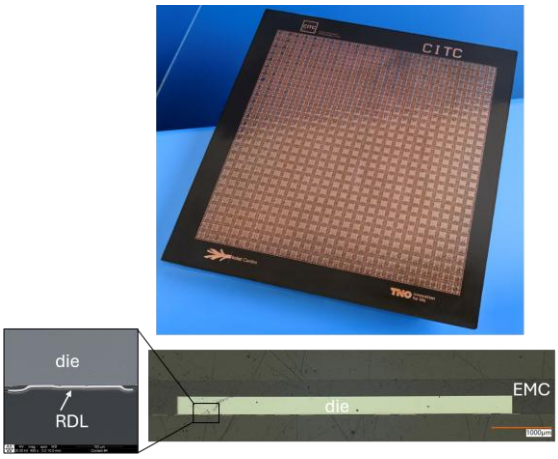


Figure 5: Photo of Gen1-size fan-out panel and cross-section images of the die package with RDL interconnects.

This HAR interconnect technology enables the fabrication of a wide range of different TPV heights, with feasibility of high pillars ranging from ~50µm to ~800µm demonstrated. Figure 6 shows ~800µm high TPVs with a diameter of ~100µm, meaning an aspect ratio (AR) of ~8.

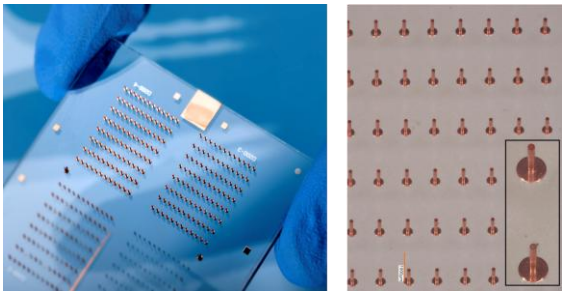


Figure 6: Photo and tilted optical microscope image of ~800µm high TPVs with diameter of ~100µm (AR=8).

To demonstrate the integration of vertical interconnects in panel format, ~50µm high TPVs were made on top of the Cu-tracks in RDL layer as shown in Figure 7(a). Ajinomoto Build-up Film (ABF) was used to encapsulate the pillars. By tuning the lamination parameters as well as the number and thicknesses of the ABF layers, the top side of the metallized pillars remains exposed, ensuring electrical conductivity before next processing steps.

Figure 7(b) shows a top view image of the same sample after embedding these conductive pillars into the ABF build-up layers. This image highlights also the top metallization of the pillars sticking out of the molded surface. A cross-section SEM image of such TPVs is shown in Figure 7(c).

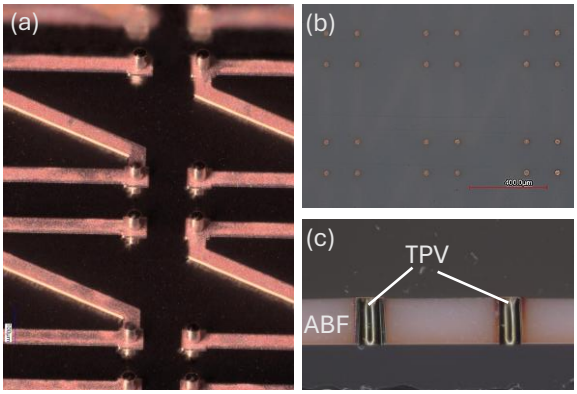


Figure 7: (a) Tilted optical microscope image of TPVs built on top of Cu tracks in RDL, (b) Top view optical microscope image of same sample after ABF lamination with pillar top metallization exposed, (c) Cross-section image of TPVs embedded in ABF build-up layers.

Since these TPV pillars are defined by lithography, this '3D-build-up' technology enables layout variations and freedom in design. For instance, different through-package interconnect functions like 3D coaxial shapes can be made inside the package to significantly improve RF signal isolation (shielding) of the interconnects (see Figure 8 with top side view and optical microscope images). The ring around the TPV is an example of an electromagnetic signal shielding structure.

These 3D design capabilities, with high resolution RDL and high-aspect-ratio TPV, have clear potential to bring significant advantages in terms of achievable compactness, system integration and high-frequency performance compared to standard PCB and FOPLP designs using laser drilling for making vertical interconnects.

As such, this versatile FOPLP innovation with embedded conductive '3D-build-up' structures made through semi-additive lithography batch process has high potential to advance fan-out panel for 6G and millimeter-wave radar devices and reduce production cost.

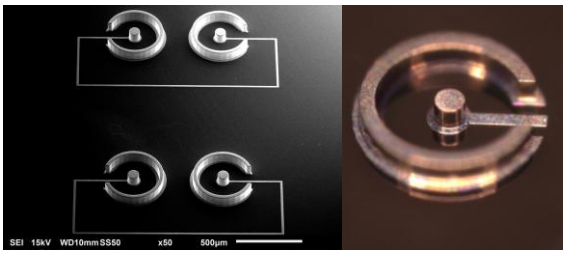


Figure 8: SEM (left) and optical microscope (right) images of TPVs with coax shape for shielding purposes.

4 Fully additive fan-out for discrete power devices

4.1 State-of-the-art (SOTA)

Conventional leadframe-based and wire- or clip-bonded packages are the incumbent, reliable and cost-effective choice for discrete power devices due to its mature manufacturing for decades, low production costs, stable supply chains, broad footprint compatibility, and proven suitability for low pin-count applications [5].

Such power devices use heavy aluminum wires, ribbons, or copper (Cu) clips to reduce resistance and increase current capacity, while soldered or sintered die attach layers typically can provide enough thermal conductivity for heat dissipation. Still lead-containing solder is mostly used and exempted for attaching die and clip for >25 years. Besides its environmental impact, lead-solders have limitations in passing automotive reliability requirements (especially when introducing SiC and GaN) and same for thermal conductivity (<40W/m-K).

Additionally, today's wire- and clip-bonded architectures inherently limit further package miniaturization and high-density integration. As described in previous sections, FOPLP typically enables high-density interconnects, strong electrical and thermal performance, and ultra-thin package profiles [6].

However, laser-drilled and Cu-plated vertical vias, together with multi-step semi-additive plating, make current FOPLP processing capital-intensive, complex, and often more costly, especially for such low-cost and price-sensitive discrete power devices.

For certain discrete packaging applications where feature resolutions are relaxed to several hundreds of microns, fully additive printing technology can be employed to replace cost intensive fan-out panel process steps. The additive fan-out packaging development described in next section retains the principal benefits of FOPLP (e.g. no need for lead frames, ribbons, clips and wire- or clip-bonding), while replacing major cost-driving steps with comparatively simple and proven screen-printing processes. This is resulting in a reduced process step count enabling a significant cost-down potential for these price-sensitive power components.

This fully additive fan-out process is demonstrated on 152x152mm² panels, with the potential to be scaled up to 310x310mm² being compatible with commercially available back-end assembly equipment. A major advantage of using screen printing is the capability of building vias and different cavity shapes in-situ (‘all in one printing stroke’) as described in next sections.

4.2 Fabrication process

The fabrication process begins by applying a semi-transparent temporary bonding layer on a 1.1mm thick glass carrier. This layer is non-sticky at room temperature, enabling fiducials to be printed directly on its surface for accurate die alignment. Silicon dies with a thickness of 90µm are then placed using a Datacon 2200 Evo Plus pick-and-place system, as shown in Figure 9(a).

A first conductive seed layer is screen-printed onto the temporary bonding surface to define the bottom-side metal package outline. Alignment between the printed features and die pads is done by fiducials. A Henkel liquid epoxy molding compound (EMC) is subsequently screen-printed over the panel using a patterned mesh that simultaneously encapsulates the dies and creates openings that serve as vertical interconnect access. This eliminates the need for laser or mechanical drilling, as illustrated in Figure 9(b). Screen mesh selection, achievable feature dimensions, and other critical parameters for printed EMC structures were reported previously [7].

A second seed layer is printed on top of the EMC to form the top side gate and source interconnects to the metal outline on bottom side. Screen-printing allows considerable flexibility in clip geometries and via configurations, as shown in Figure 9(c).

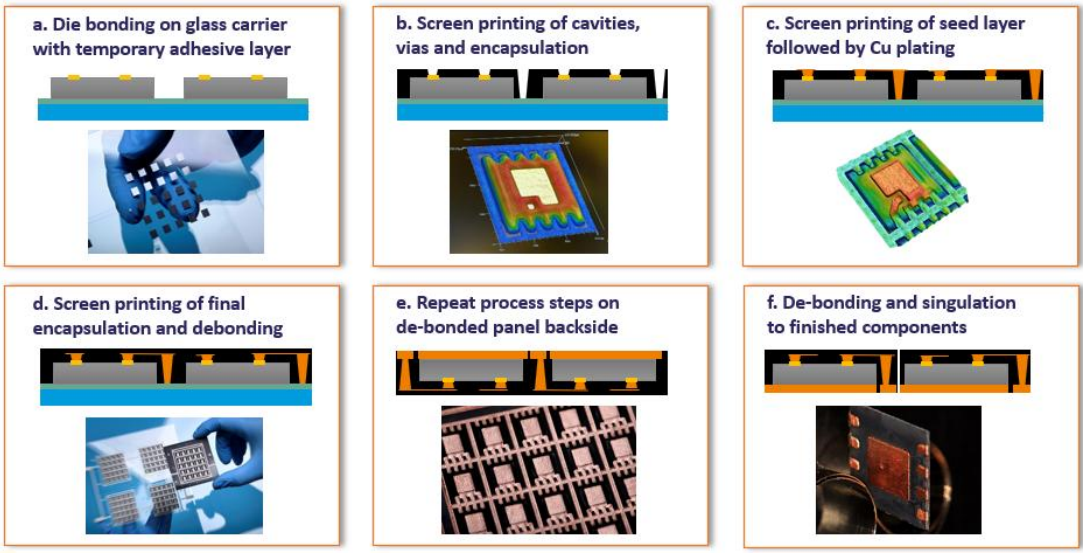


Figure 9: Additive fan-out process flow, a) Dies attached to temporary carrier, b) EMC via formation using screen-printing, c) Screen-printing and Cu-plating of top clip, d) Top encapsulation with printed EMC and panel de-bonding, e) Definition of the backside contacts, (f) Singulation to functional

Copper is then electrolytically plated onto the electrically connected seed layer with a thickness of 50-70µm, providing the required electrical and thermal performance. Because all seed layer segments are connected to the package perimeter – like a lead frame – plating can be performed using a standard and straightforward fully additive process.

An additional EMC layer is stencil-printed to encapsulate the top surface. Stencil-printing allows thicker and more uniform deposition, although transfer or compression molding can also be considered. Where exposed top side terminals are required, screen printing can define openings in the encapsulation layer [7]. This completes the upper half of the panel, which is then de-bonded from the temporary carrier, as shown in Figure 9(d).

The partially completed panel is flipped, re-bonded to another temporary carrier, and processed on the bottom side using same EMC deposition, seed layer printing, and Cu-electroplating process, as shown in Figure 9(e). After both sides are completed, the panel is de-bonded again and singulated by laser dicing into individual functional devices, as shown in Figure 9(f).

The final discrete power component measures 5.0x6.0mm² and includes 0.4mm wide terminals at a pitch of 0.65mm, which matches the industry-standard DFN56 footprint. This lead-free and fully additive fan-out process provides substantial design flexibility in package layouts, 'printed clip' geometries, and interconnect arrangements, which can be modified primarily through changes to the screen (mesh), stencil and printing sequence.

4.3 Experimental results

The fabricated structures were evaluated using optical microscopy, SEM-EDX, confocal height profiling, and cross-sectional imaging. Figure 10(a) shows the first printed epoxy molding compound (EMC) layer extending from the flat glass carrier to the top surface of the 90µm thick MOSFET die. This EMC layer serves two functions. It creates a gradual ramp that enables the seed layer to be printed across the die topography, and it protects the die surface from electrical shorts while leaving the source and gate contacts exposed.

Figure 10(b) shows the silicon MOSFET die fully covered by the printed epoxy mold compound (EMC) and seed layer before Cu-electroplating, including 'copper clip' area and ~500µm wide gate connection. Printing on the die top contacts is challenging, because the process must bridge the die topography while maintaining accurate alignment and feature dimensions. Nevertheless, height variations associated with the 90µm thick die were successfully accommodated. The gate contact and clip structure were printed simultaneously, creating a direct electrical path from the die surface to the package side terminals.

After the panel is de-bonded and flipped, a final seed layer is printed onto the drain pads and Cu-electroplated, as shown in Figure 10(c), to form the final bottom contacts used for solder attachment on test PCBs.

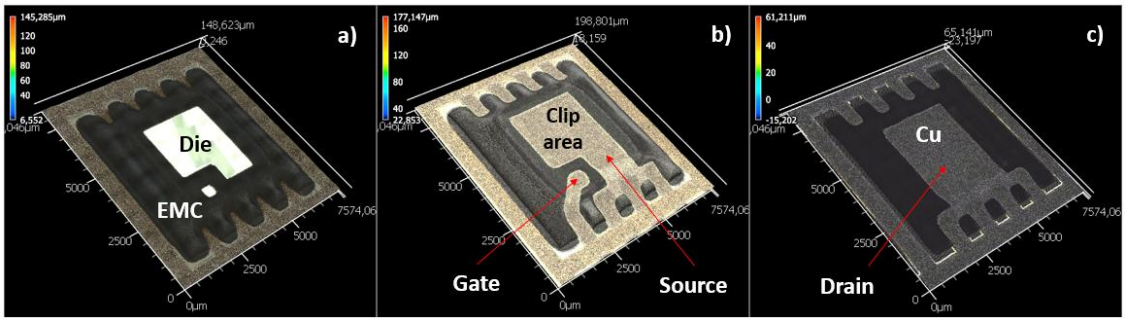


Figure 10: 3D rendering of confocal scans of additive fan-out package, a) Printed epoxy mold compound (EMC) over printed grid on carrier and MOSFET die, b) Seed layer printed gate and source connections to die top, c) Printed and Cu-plated drain connection to die back side after de-bonding and flipping of panel.

A high-resolution cross-section of a singulated final component was made to investigate the complete package geometry as presented in Figure 11.

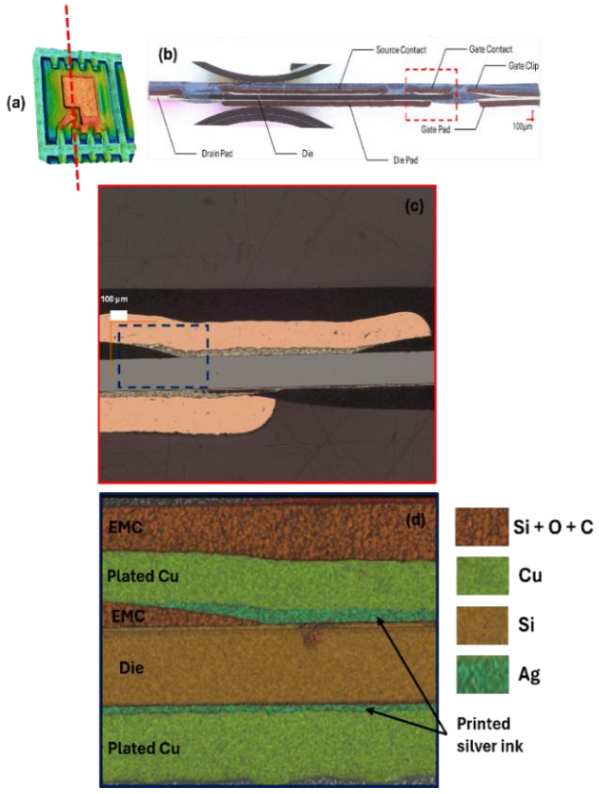


Figure 11: Cross-section view of final additive fan-out package, (a) Location of cross-section (red line), (b) View of gate and drain contacts to die, (c) Overall cross-section view of additive fan-out package, (d) EDX micrograph of cross-sectioned package.

Figure 11(a) identifies the cross-section location, while Figure 11(b) shows the copper drain, source/drain, and gate pads separated by thin layers of molding compound. Thin gray regions beneath the plated copper correspond to the printed seed layer. The 90µm MOSFET die is clearly visible in the upper portion of the package, together with the printed source and gate contacts extending to its surface. These Cu-plated features connect to the external side pads through the printed clip structure.

A magnified image of the gate region in Figure 11(c) shows a Cu-thickness of ~65µm. The flow behavior of the liquid EMC produces gently sloped via sidewalls, which support printing across the package topography.

Finally, a feasibility study published before showcased screen-printed via diameters of ~100µm in epoxy mold compound [7]. This means that there's room toward finer resolutions for this fully additive fan-out technology described in this paper.

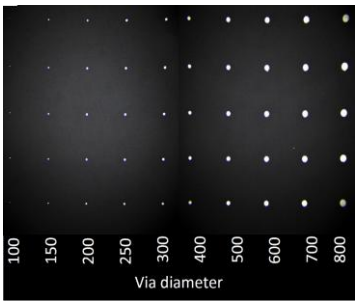


Figure 12: Screen-printed vias in EMC down to 100µm

5 Conclusions

This paper presented two innovative fan-out panel-level packaging (FOPLP) technologies together with their fabrication approaches and experimental validation results:

- A *semi-additive FOPLP platform* based on conductive through-package-via (TPV) pillars and three-dimensional conductive structures fabricated prior to embedding in an epoxy encapsulant.

- A *fully additive FOPLP platform* based on printed cavities and printed seed layers within an epoxy encapsulation process, targeting substantial cost-reduction.

Table 1 provides an indicative comparison between these two emerging FOPLP technologies versus conventional FOPLP manufacturing process currently used in production (see next page).

It should be noted that this comparison reflects the current development status of both platforms. Ongoing development activities at TNO/CITC aim to further expand the capabilities and performance of these technologies, next to reliability assessment.

For the HAR TPV platform, future developments target line/space dimensions of 10/10µm, via diameters of 20µm, and aspect ratios of 10 for vias larger than 50µm. For the fully additive fan-out platform, future developments focus on accommodating thicker dies (>100 µm), reducing via diameters (<200 µm), and achieving higher aspect ratios (>1).

	Typical Fan-Out PLP *)	Fan-Out PLP for HF RF **)	100% Additive Fan-Out **)
Target Application	Miscellaneous	RF System Integration	Power IC/Discrete
FOPLP Process	Chip First, Face Down	Chip First, Face Down	Chip First, Face Up
Panel Size (mm2)	Up to 700 x 700	Up to 350 x 320	Up to 350 x 320
Panel Thickness (mm)	Up to ~1.5	Up to ~1.5	Up to ~1.5
Die Thickness (µm)	Up to 380	Up to 250	Up to 100
Encapsulation Process	Compression Molding	Vacuum Lamination	Screen, Stencil Printing
Through Package Vias (TPV)	Laser Drilling, Cu Plating	Cu Plated Polymer Pillars	Screen Printing, Cu Plating
TPV Processing	Serial (one by one)	Batch (all in one go)	Batch (all in one go)
Minimum Via Diameter (µm)	~10	~50	~200
Blind Via Aspect Ratio (H/D)	~1	~8	~0.5
Minimum Line/Space (µm)	~5/5	~15/15	~100/100
Redistribution Layer (RDL)	Lithography, Semi-Additive		Seed Layer, Cu Plating
Capital Investment	High	Medium	Low
Technology Status	In Production	Under Development	
**) Based on ECTC paper from T. Braun [2] and customer insights*		***) Based on TNO's Gen1 glass panel pilot line*	

Table 1: Comparison of traditional fan out, fan out for HF RF and fully additive fan out.

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