Advanced Embedding Technologies for High Performance SiC Power Modules in Automotive Applications

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Abstract

The ongoing transition towards electrified powertrains places increasing demands on power module performance, reliability, and scalability. Automotive traction inverter applications based on silicon carbide (SiC) MOSFETs require advanced packaging solutions capable of supporting high power density, low parasitic inductance, and efficient thermal management. Conventional module concepts are increasingly challenged by the fast switching behavior of SiC devices and the resulting electrical and electromagnetic constraints.

Embedding technologies provide a promising approach to address these challenges by integrating bare power semiconductor dies directly into multilayer substrate architectures. This work presents an advanced embedding concept for high performance automotive power modules utilizing SiC MOSFETs. Bare dies are attached to thermally conductive substrates by silver sintering, followed by multilayer vacuum lamination using epoxy prepreg materials. Electrical interconnects are realized through laser drilled micro vias and electrolytic copper plating, enabling compact current paths, thick copper routing, and efficient heat spreading.

The presented approach significantly reduces parasitic elements, particularly stray inductance, thereby supporting the exploitation of fast SiC switching characteristics while mitigating voltage overshoot and electromagnetic interference. Key aspects of the technology, including semiconductor requirements, thermal and electrical design considerations, and material selection, are discussed. Practical power module implementations demonstrate the suitability of the embedding concept for scalable, high performance automotive applications.

Key words

Embedding, PCB technology, SiC MOSFET, Power module, low inductance

I. Introduction

The PCB based embedding of power semiconductors like SiC MOSFET or GaN provides several advantages. Beside the potential of miniaturization and the possibility of three dimensional approaches, the improvement of the electrical performance is a mayor benefit. The replacement of bond wires to contact the semiconductor with the use of direct copper connections, result in a very short connection length and with this in a significant reduction of parasitic inductance. As a result, the switching behavior can be improved and switching losses are reduced. The addressed applications can be multifaceted: (1) Single die packages, what we call “Prepackages”, only containing one power semiconductor to form a very robust and improved package solution, that could be handled like an SMD component, (2) power modules, half bridge or complete inverter structures, for electrically improved systems, or (3) 3D modular power electronics, which provides the possibility to combine a power module with needed logic and driver functionality in a compact and robust monolithic block.

Looking on this technology in a European view, several companies are offering embedding approaches for power modules, most of them out of the PCB world. Schweizer Electronic (DE) and AT&S (AT) do have a long experience with their p² Pack [1] or ECP technology [2] respectively. In addition, other PCB manufactures gain more interest in this technology topic, like Würth electronic [3] or Unimicron Germany [4]. The basic principle of all the different approaches to realize embedded component packages or modules is quite similar for all and will be described in the following in detail.

II. Embedding Technology

A. Motivation

The use of wide bandgap (WBG) semiconductors such as SiC or GaN allows a very fast switching of high voltages in the kV range. These semiconductors can switch on from 0 to 1.000 V in a few nano seconds. If a conventional chip packaging is used for these semiconductors, such as wire bonded and over molded packages, the parasitic inductances within these packages significantly degrade the switching performance. For this reason, an adapted and optimized packaging concept is essential, to enable the fast switching performance.

PCB based component embedding is one approach to realize such an optimized packaging concept. In the printed circuit board industry, where this process has been in use for more than a decade, low voltage applications have been the main focus. However, high voltage applications, e.g. for traction inverters in automotive applications, have been gaining in importance in recent years.

By replacing the bond wires that connect the chip by direct copper plated micro via connections, in combination with optimized conductor line length, and the possibility to integrate three dimensional structures, a substantial improvement in the electrical performance of such packages or modules is achieved. The significant reduction in parasitic inductance improves switching behavior and results in lower losses. Embedding technology therefore offers an excellent method for packaging of such semiconductors.

Conventional modules are typically frame based. Here the power components are soldered to a ceramic substrate and the top side connections of the chips are done by aluminum wire bonds. Within the module construction, subsequently the ceramic substrates are then soldered to a base plate and ribbon bonded with the module frame, connecting to the pins for power and control. Apart from the fact that only two wiring levels are available, which do not allow component mounting on the top side, this design results in high parasitic inductances (30 to 100 nH), which is limiting the switching speed.

A step forward to reduce parasitic inductance, and with that allowing faster switching, is e.g. the Semikron-Danfoss eMPack® module [5]. It is based on their SKiM® technology and provides direct chip connection by double sided sintering. Although this approach also only provides two wiring layers, the parasitic inductance can be significantly reduced to around 2,5 nH.

The embedding technology overcomes most of these limitations. It is based on direct Cu connections to the embedded chip and flat Cu wiring on top. With that, lowest parasitic inductances could be achieved. In addition, it provides a flat surface on which additional further components could be placed in closest vicinity of the switching cell, improving the electrical characteristics even further. Proper electrical design can yield in ultra low parasitic inductances down to 0,5 nH.

B. Methods of Power Embedding

To address high voltage applications, a suitable electric insulation needs to be added to the embedded structure. On the other hand, this insulation layer also needs to ensure a sufficient thermal management, since e.g. a single SiC can generate more than 100 W losses.

The method that will fit best into a PCB production environment would be an organic insulation layer (Figure 1). Such a film could be easily implemented into the PCB process flow. The organic material needs to provide sufficient breakdown voltage for e.g. 1.200 V applications and a good thermal conductivity. However, these organic layers are limited in their thermal conductivity. Best in class provide 8 to 10 W/mK according to the datasheets. With this limitation, maximum losses and power density of modules are limited.



Figure 1: Schematic of embedded structure with organic isolation layer

To address higher power densities the integration of ceramic substrates needs to be considered. These are preferably silicon nitride (Si_3N_4) AMB (active metal brazing) substrates. These substrates are providing superior electrical insulation and thermal conductivity up to 90W/mK. Here, the challenge is to combine the ceramic material with the PCB process sequence. To overcome this challenge, the ceramic substrate should be kept as small as possible and will be embedded into the PCB structure similar like the power component itself.



Figure 2: Schematic of embedded structure with ceramic isolation layer

In Figure 2 a schematic example for the use of an embedded ceramic is shown. Here, the ceramic substrate is embedded into a base PCB substrate and the SiC die is assembled to this substrate and is embedded using several layers of epoxy prepreg material. Warpage control of the resulting substrate after embedding is a critical point and needs to be balanced and is mainly determined by the size and density of the ceramic in the substrate.

For both variations, the heat generated by the power component, must be removed effectively from the bottom side of the chip. That is why a sufficient heat spreading, e.g. by thick copper layer, is important to realize an effective transfer at the heat sink or cooler.
The impact of an organic vs. a ceramic insulation, can be demonstrated by a simple thermal estimation. Taking the following boundary conditions into account:
Organic insulation:

- Chip 5x5 mm², 100 µm thickness
- Cu heat spreader 14x14 mm², 2 mm thickness
- Organic insulator 150 µm thickness, 2,8 W/m*K
- T cooling water 65°C, T junction 175°C

Ceramic insulation:

- Chip 5x5 mm², 100 µm thickness
- Cu/Si_3N_4/Cu AMB ceramic 14x14 mm²,
- 0,5 mm Cu layers, 250 µm Si_3N_4 90 W/m*K
- T cooling water 65°C, T junction 175°C

In this case, one MOSFET with an organic insulated structure can conduct 85 A, compared to 114 A for the ceramic version. Based on this estimate, the ceramic insulator allows for approximately 34% higher current per transistor, which offers the possibility of increasing power density or reducing the number of chips within a module configuration.

C. Materials

1) Semiconductor

To be compatible with the embedding process, the components need to have a specified contact metallization. SiC power semiconductors have back and front contacts, typically the drain contact is the backside, whereas gate and source are on the top side of the chip. The back contacts of most power semiconductors have by default a silver or Ni/Au finish, which provides an optimal match with the Ag sintering process, used for die attach. The top contacts (gate, source) of power semiconductors are typically delivered with a 1 to 3 µm thick aluminum metallization. This metallization is not compatible with the micro via drilling process using UV or IR laser and the subsequent metallization process. The micro vias are cut through 5 µm copper (on top) and the 50 to 80 µm thick cured prepreg (glass fiber epoxy compound). During the laser drilling around 1 to 2 µm of the contact metallization can be removed by the laser ablation process. Additionally, cleaning processes, required for the copper metallization, can remove up to 1 µm of copper. Therefore, the contact pad of the embedded component needs to provide a compatible metallization. Hence, a 10 to 12 µm thick electroplated copper metallization is applied, ideally in a wafer level process. This 10 to 12 µm copper pad metallization provides a sufficiently thick pad for a reliable micro via drilling and metallization process.

2) Embedding materials

For the embedding process for high voltage applications, two classes of materials need to be considered: (1) The embedding material itself and (2) thermally higher conductive isolators enabling the thermal management.

As the embedding material, epoxy prepreg or copper clad (CCL) materials are used. Prepreg is the PCB initial material. Certain properties are mandatory, which are the following:

- **High thermal stability:** Since SiC MOSFETs will be operated at high junction temperatures up to 175°C and above, the embedding material needs to be capable of operating at these temperatures. Standard FR4 materials do not provide these capabilities. Therefore, materials with a T_g well above are required. Typical high temperature laminates provide T_g of 250°C and higher.
- **Coefficient of thermal expansion (CTE):** The CTE should be well balanced to the different materials, which will be present in the embedded structure. On the other hand, also elasticity of the material has significant impact on the stresses that will be introduced to the structure. Thermo mechanical modelling will help to determine a well fitting material selection.
- **Breakdown voltage:** Currently 850 V inverter modules are of high attention, typically 1.200 V SiC MOSFET are of interest. With these given numbers, the used embedding material should provide a sufficient breakdown voltage of at least 2 to 3 times of these values.

A careful testing of breakdown voltages is of high importance, as the values listed in data sheets may provide only limited information that does not adequately describe the material's behavior under operating conditions. Depending on their thickness (60 µm to 100 µm), the most commonly used types of material show excellent high voltage performance between 5 kV and 7 kV. Thermal aging and the possible degradation in high electric fields and the impact on the material properties is a topic which is still under investigation.

In addition to the breakdown voltage, for organically insulated modules, the actual thermal conductivity of organic thermally conductive materials is also important for selecting a suitable module design. The values in the data sheets often do not reflect the actual properties. Therefore, testing the thermal conductivity of the bulk material is of great value. In many cases the measured values are up to 30% lower than the values in the data sheet.

Commercially available AMB ceramic substrates are used for the ceramic insulated approach. These offer precisely defined electrical and thermal properties.

D. Electrical design and advantages

Looking on the electrical design, the embedding of power semiconductors, which is realizing a planar structure, provides a lot of benefits. In Figure 3 the typical B6

configuration for a 3-phase inverter structure is illustrated. Realizing an embedded module out of this, a planar module, which realizes direct copper connections to the power semiconductor and short and planar electrical paths, can be realized.

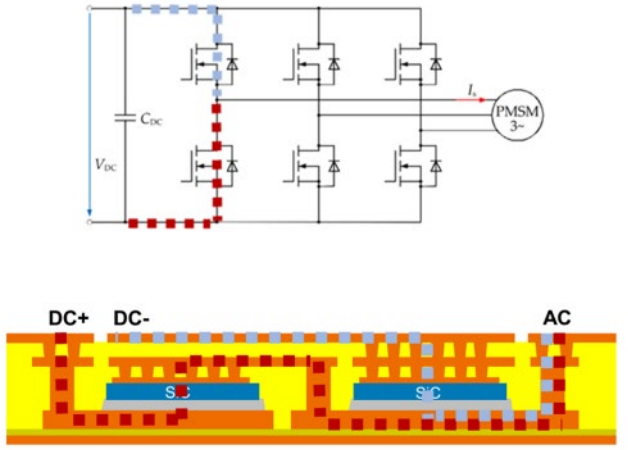


Figure 3. Typical half bridge configuration and schematic of embedded structure

As a result, very short DC link loops are possible to achieve, and the DC link inductance can be reduced to below 1 nH. In addition, DC link snubber can be placed on top of the planar embedded module, very close to the switching cell (**Figure 4**). With this possibility, zero ohm gate resistance is possible, allowing fastest switching without significant ringing, reducing the switching losses by 70% and more.

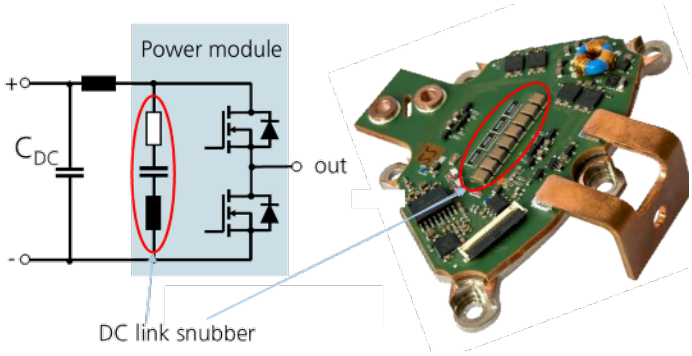


Figure 4. Integration of DC snubber on embedded module

E. Embedding Technology

The complete process flow for the embedding of power electronic devices like IGBT, MOSFET, SiC transistors or others is based on printed circuit board technology in combination with a suitable die attach method. Also, the material properties of the used FR4 materials are of paramount importance. Like already described, beside suitable thermo mechanical characteristics, they need to provide the ability to withstand higher operational temperatures, because of the losses and resulting temperatures of the embedded power semiconductors.

The general process flow is shown in Figure 5. In the first step, the base substrate with embedded ceramic substrates is produced. Therefore, core and prepreg material with opening at the positions of the ceramics are prepared. The core layers are helping to fix the ceramics during the subsequent lamination for embedding these on one side and will provide registration infrastructure for the die attach of the power semiconductors. The prepreg layer provides the needed free resin, which will flow and fill all gaps during lamination and "glues" the core material together. Out of this step, a large substrate with embedded ceramic substrates is ready for the following embedding process. For mounting the semiconductors on the embedded ceramic substrates, a low pressure, low temperature Ag sintering process is used. This method offers several advantages: First, it is possible to mount the dies on a large panel format, which enables highly parallel processing. Furthermore, the accuracy of chip attachment, which is important for the following process steps, depends mainly on the accuracy of the chip attachment process, as the chips remain most accurately in position during the sintering process, unlike in a soldering process. In addition, the Ag sintering layer provides excellent thermal (≥100 W/mK) and electrical contact (≤0,008 mΩcm) to the substrate.

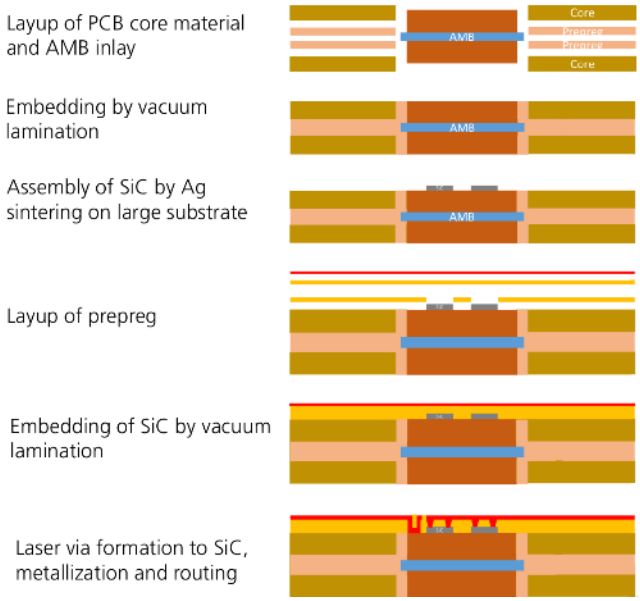


Figure 5. Schematic process flow

The embedding itself is done by vacuum laminating FR4 prepreg layers (glass fiber with epoxy resin in the B-stage). Structured prepreg layers are used to compensate for the height of the chip mount and the chip, and full layers provide the necessary insulation to the electrical layer above the chip. In addition, a copper foil is applied, which is required for the metallization process. The embedding itself is done by

laminating the stack in a standard multilayer laminating press.
Laser via holes are used to establish contacts to the embedded chip, which must be carefully controlled and parameterized so as not to damage the chip. Blind vias to the thick copper substrate or thicker copper layer are usually produced by mechanical drilling. The micro vias are then filled in a copper plating process, followed by structuring of the electrical layer by lithography and etching of the copper. The appearance of the printed circuit board with embedded components is the same as that of a conventional printed circuit board. Therefore, in subsequent processes, either additional signal layers can be processed, solder masks and surface finishes can be applied to mount additional components on the embedded module or additional heat sinks or embedded modules of various types can be applied to the module [6], [7].

The following illustration shows the technological process flow for an embedded power module with integrated ceramic insulation.

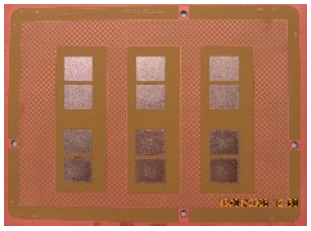


Figure 6: Base substrate with embedded AMB ceramic substrates

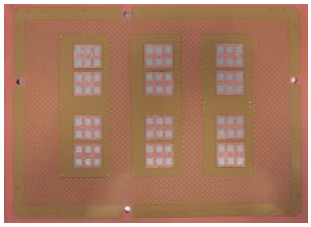


Figure 7: Partial Ag deposition on AMB

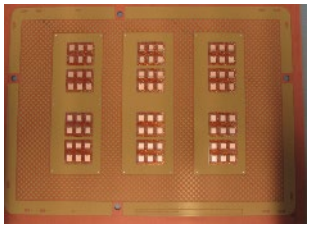


Figure 8: Ag Sinter Die attach

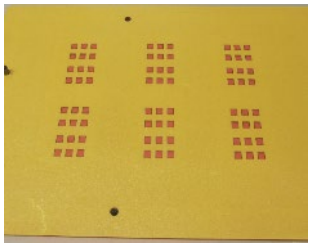


Figure 9: Layup for embedding



Figure 10: Structuring of electrical routing layer

In the first step, the base substrate with embedded ceramic substrates (AMB) is produced, **Figure 6**. This is realized by laying up structured prepreg and core layer and inserting of AMB substrates into the openings. Subsequently, lamination and embedding of the AMB is done. To prepare the copper surface of the AMB for the Ag sinter die attach, immersion silver is deposited at the positions of the dies (**Figure 7**). In the next step, the SiC chips are assembled onto the base substrates. First, Ag sintering paste is applied using stencil printing. The chips are then precisely positioned using a suitable chip bonding machine. During this process, the substrate and the bonding tool are heated to fix the chip onto the Ag sintering paste. A low temperature, low pressure sintering process is then carried out on the large panel format (**Figure 8**). In preparation for the embedding process, structured layers of prepreg, which provide the thickness required to compensate for the chip and chip attachment height, as well as prepreg as an insulation layer and copper foil are applied over the entire surface (**Figure 9**). This stack is transferred to a multi layer laminating press, where the lamination process for embedding is carried out. During this process, pressure and temperature ramps are applied in a vacuum atmosphere. The B-stage resin becomes liquid and fills all gaps as it flows, completely embedding the components. During the curing phase at curing temperature, the B-stage resin cross links completely, ensuring the laminate's excellent thermo mechanical and electrical properties.
Following this process step, a typical process sequence is carried out, that is comparable to PCB manufacturing. The micro via connections to the embedded SiC chips are created using laser drilling and the micro via connections to the copper surface of the AMB copper are created using either laser drilling or mechanical drilling. Cu metallization is performed to fill the vias with copper and build up the required copper thickness. Finally, the conductor lines are structured in a typical subtractive process: application of photoresist, lithographic exposure and etching of the copper (**Figure 10**).
In **Figure 11** and **Figure 12** a cross section of a half bridge module manufactured in this way is shown. Here, an AMB consisting of a 300 µm thick copper layer and a 320 µm thick Si_3N_4 ceramic is used and embedded as described. The SiC MOSFETs are sintered onto the upper copper of the AMB substrate, embedded and connected. A two layer wiring configuration is produced.

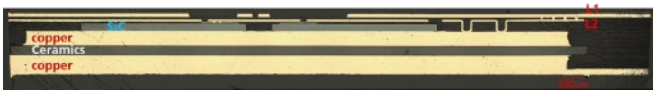


Figure 11: Cross section of a embedded half bridge module with embedded AMB and SiC MOSFETs



Figure 12: Detail of embedded module

Figure 13 shows an example for a half bridge module with ceramic safety insulation. On two embedded AMB

substrates, six SiC MOSFETS are assembled and embedded for high and low side switch each. The embedding is done in the way described and the high current connections are later realized by laser welded bus bars.



Figure 13: Ceramic based half bridge module

III. Applications

A. Single Die Packages

The most basic form of an embedded power semiconductor package consists of a single die integrated into a robust housing. This structure serves as an initial building block for more complex configurations, such as half bridge modules, while leveraging the benefits of embedding technology, namely minimal thermal impedance and negligible parasitic inductance. These characteristics are critical for high performance power conversion applications.

At Fraunhofer IZM different types of prepackages were developed over the last couple of years. These focused on simple, non insulated prepackages, with SiC dies packaged in a robust and electrical improved housing, as well as on prepackages already containing safety insulation. In both cases the prepackages provide superior thermal and electrical properties and can be handled like a standard SMD component for further modularization.

In **Figure 14** the principle of an insulted prepackage is shown.

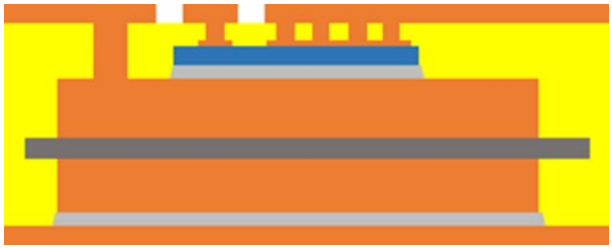


Figure 14: Schematic of embedded (SiC) prepackage with integrated safety insulation

To produce such prepackages, the process sequence will remain the same, with the difference, that in addition to the semiconductor, the ceramic substrate will be assembled to the base copper.

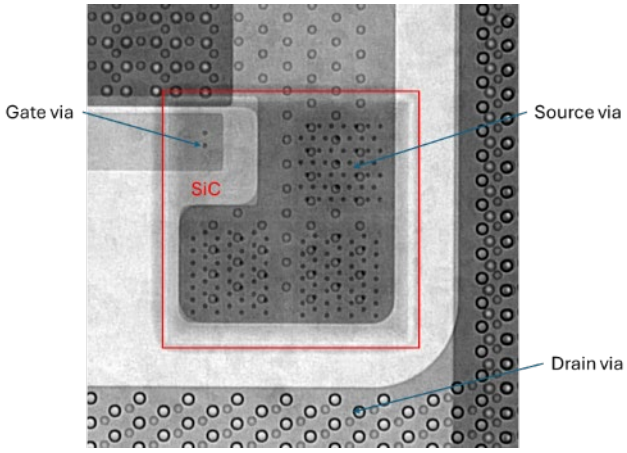


Figure 15: X-ray of SiC prepackage structure

Figure 15 shows an x-ray image of such a prepackage structure with integrated ceramic substrate. The gate and source via connections are applied directly to the corresponding pads on the chip. The drain connection is realized by micro via down to the top copper of the ceramic substrate, on which the backside of the die is electrically and thermally conductive assembled. The entire structure offers short connection lengths with low inductive coupling, which is achieved by the direct copper connection using copper filled micro vias. If necessary, an additional copper layer can also be produced for routing.

In addition, **Figure 16** shows a cross section of the resulting package is shown. These prepackages are designed for 850 V applications, using 1.200 V SiC MOSFET.

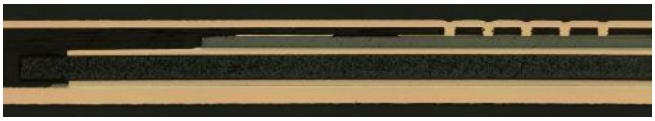


Figure 16: Prepackage with embedded SiC MOSFET and Ceramic insulation

B. Multi die prepackages for high performance traction inverter

As part of the “Dauerpower” project [8] (FKZ 19I21023C), an innovative inverter for electric vehicles was developed, that increases efficiency and performance through improved cooling management and the use of silicon carbide (SiC) semiconductors. The aim was to increase the performance of the drive trains, extend the service life of the components and reduce production costs. The entire system, including hardware and software, was developed as part of this project. An integral part of the converter concept is the embedding of

power semiconductors based on printed circuit board technologies.
The embedding of the components makes it possible to keep the distance between the forward and reverse conductors short, thereby reducing the stray inductance of the commutation circuit. This in turn allows full utilization of the semiconductor performance through faster switching operations and further reduces losses.
The basis for this success are 48 1200 V SiC transistors, grouped into three modules. These are embedded directly with ceramic insulation using the process described above, allowing for optimal thermal management and, thanks to the implementation of prepackages with two MOSFETs each, also offering great potential for scalability.

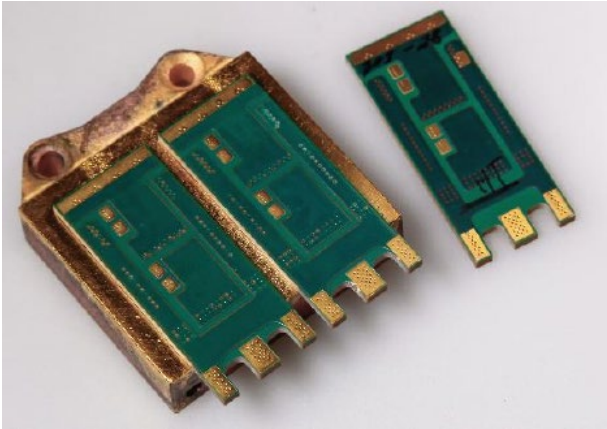


Figure 17. Prepackages Ag sintered on Cu heat sink

Figure 17 shows the individual prepackages and their attachment to the copper heat sink. Each of these prepackages uses two separate silicon nitride (Si_3N_4) ceramic substrates, each of which has a SiC MOSFET mounted and embedded on it. In addition, a separately manufactured high current printed circuit board is embedded in the package design. This provides the high current connections on the base of the prepackage. The gate contacts are located on the top of the prepackage. **Figure 18** shows a cross section of a prepackage mounted on the heat sink and illustrates its structure.

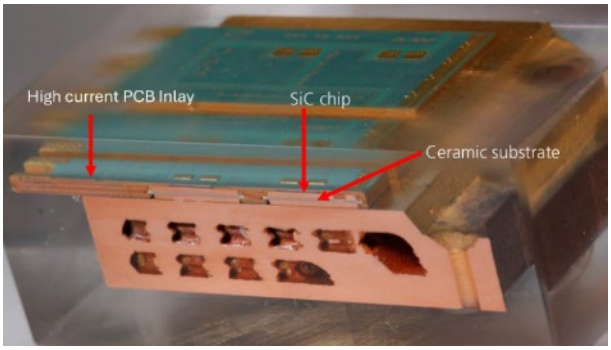


Figure 18. Cross section of prepackages and heat sink

The Cu heat sink is then mounted on the aluminum water cooler (**Figure 19**) and the complete system is built from it (**Figure 20**). The advanced cooling system uses 3D printed cooling elements that are optimally matched to the thermal requirements and ensure uniform heat dissipation.



Figure 19. Prepackage with Cu heat sink mounted to Al water cooler

The 3-phase drive converter (Figure 20), constructed in this way, achieves a peak efficiency of 98.7%. The continuous power output is 600 kW and a peak power of 720 kW can be provided. The power density is 200 kVA per liter, which is significantly higher than that of conventional converters used in electric vehicles. Thanks to the electronics packaging technology used for the SiC MOSFET and the entire module, the commutation inductance is only 1,1nH.

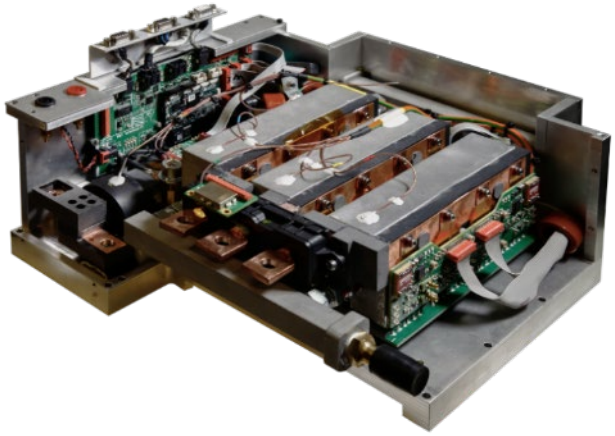


Figure 20. Complete inverter with embedded SiC dies and optimized cooling

III. Conclusion

The embedding of power electronic components into advanced packaging structures presents a significant advancement in enhancing system reliability and electrical performance. Recent developments in automotive powertrain systems have focused on the mass production of

high voltage inverters utilizing silicon carbide (SiC) MOSFETs. Embedding technologies enable superior thermal management, reduced parasitic inductance and improved electrical interconnects, which are critical for exploiting the full potential of SiC devices.
SiC MOSFETs offer markedly lower conduction and switching losses compared to conventional silicon based transistors, making them highly advantageous for high efficiency and high power density applications in electric vehicles. To support the fast switching characteristics of SiC semiconductors, packaging solutions must minimize parasitic effects, particularly stray inductance. These requirements underscore the importance of embedding technologies in achieving robust, scalable and high performance power module designs for next generation automotive systems.

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