

SHIELDUSA: *Leap-ahead organic substrate enabled by fan-out technology, domestic materials, process innovations, and novel EDA workflows*

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Mike Naujokaitis, Tim Takeuchi, Leslie Hwang, Chris Bailey,
Craig Bishop and Jason Conrad

IMAPS DPC 2026
March 4th, 2026

DECA

ASU

Outline

- Introduction
- **SHIELD** USA
- Electronic Design Automation
- Process Flow
- Key Technologies
- Conclusion

Outline

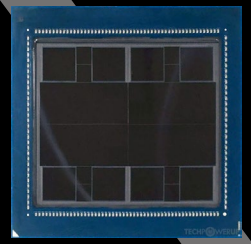
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Three Technology Imperatives for Scaling AI Hardware

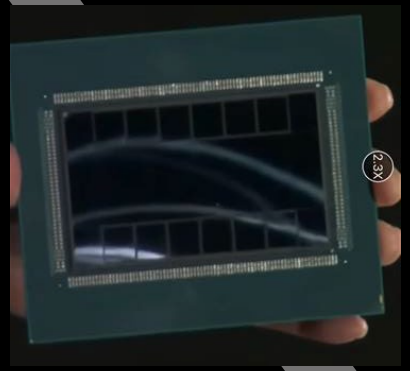
Large form factor



nVIDIA H100
- 6 HBM3 stacks
- 1 GPU die
- ~54x33 mm²



AMD MI300
- 8 HBM3 stacks
- 4 GPU dies w. HBI
- ~ 49x43 mm²



AMD CES 2026
- 12 HBM3 stacks
- X? GPU dies
- ~ 110x80 mm²

Large form factors to >120x120mm²

Source: nVIDIA, AMD, CES2026

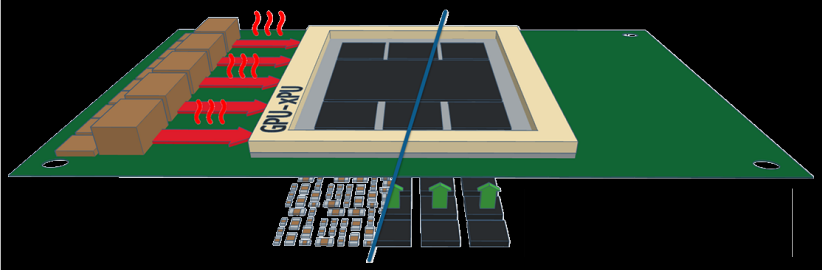
Increased IO density

HBM generation	HBM3 (2025)	HBM4 (2026)	HBM5 (2029)	HBM6 (2032)	HBM7 (2035)	HBM8
Datarate (Gbps)	6.4-8	8	8	16	24	32
Signal IO count	1024	2048	4096	4096	8192	16384
Bandwidth (TB/s)	1	2	4	8	24	64
Capacity (GB)	24	48	80	120	192	240

Source: KAIST Standard HBM research roadmap

Dense interconnect of ICs and 3DICs for the increased compute & memory demand

Embedded functionality



Lateral PD

Vertical PD

Source: Power Electronics Magazine, 2025

Embedded functionality in substrate core to minimize power path length and RDL losses

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SHIELDUSA

SHIELDUSA *Delivering the Technology for Scalable AI Hardware*

Leadership

ASU

DECA

Core Partners

AMD

ANALOG DEVICES

IBM

HEIDELBERG INSTRUMENTS

NXP

saras MICRO DEVICES

ROGERS CORPORATION

skywater

SYNOPSYS®

UNIVERSITY OF MARYLAND

$100M Chips Act funded program

Extending Fan-out Technology to Advanced Substrates

Large FF

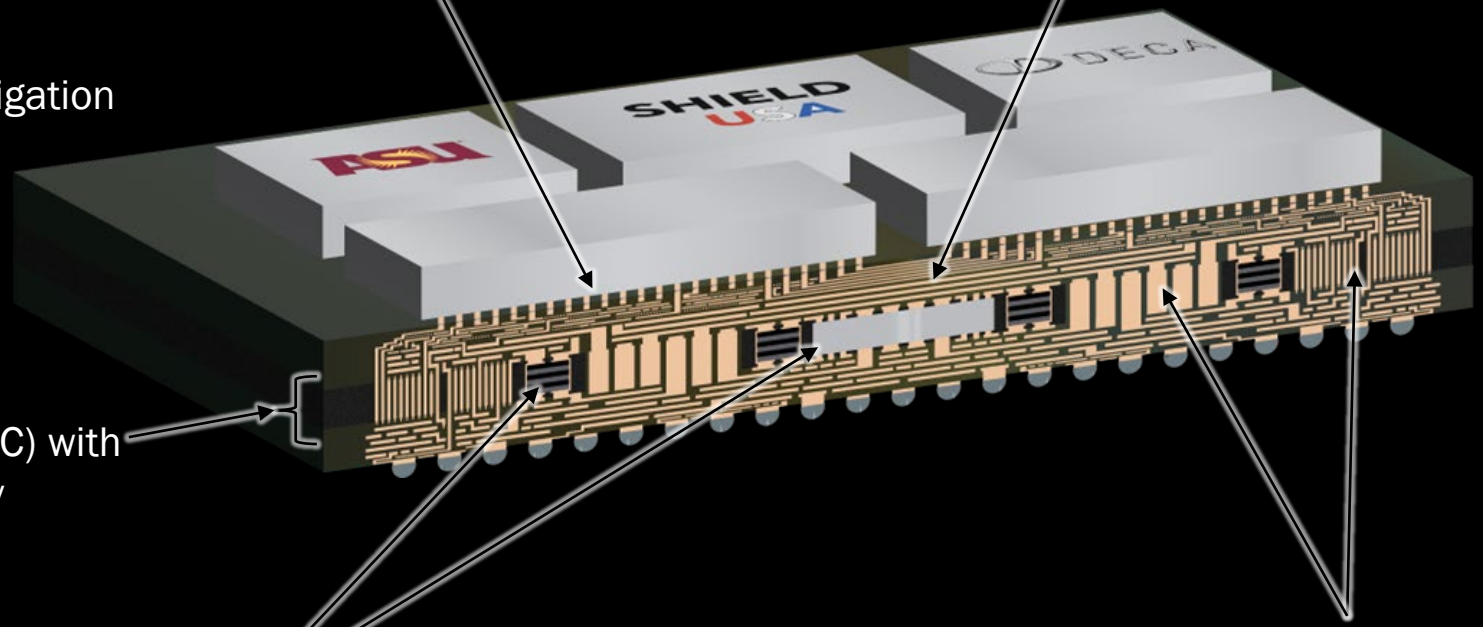
Functionality

IO density

No interposer layer
→ µbump pitch 25µm to sub-10µm roadmap

Robust manufacturing
→ Adaptive Defect Mitigation

Ultra-high density RDL on build-up film (MDx)
→ L&S 2&2µm to 0.5µm&0.5µm roadmap
→ No capture pad vias (5µm to 2µm roadmap)



Molded fan-out core (MC) with embedded functionality

Embedded passives & actives
→ High density caps and inductors
→ Power management, RF, control

High aspect ratio embedded vertical interconnect blocks (VIBs)
→ 35µm to 20 µm pitch through-core

Delivering across the three key AI technology imperatives

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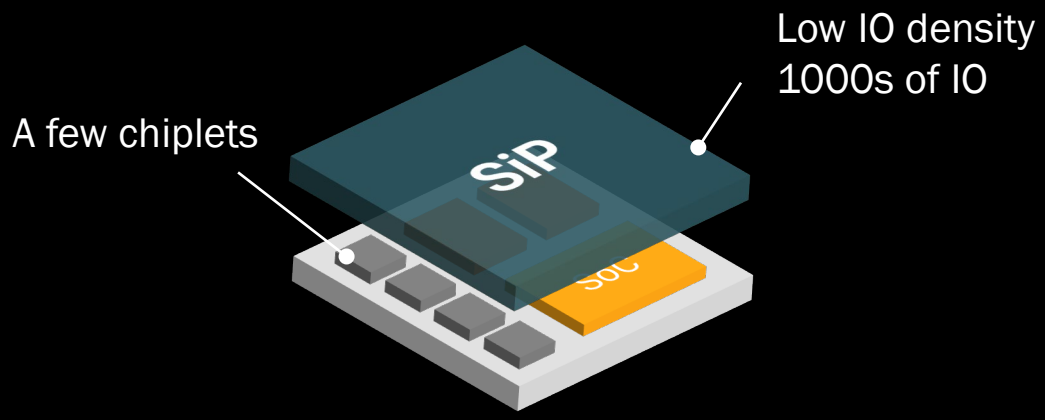
SHIELDUSA

Outline

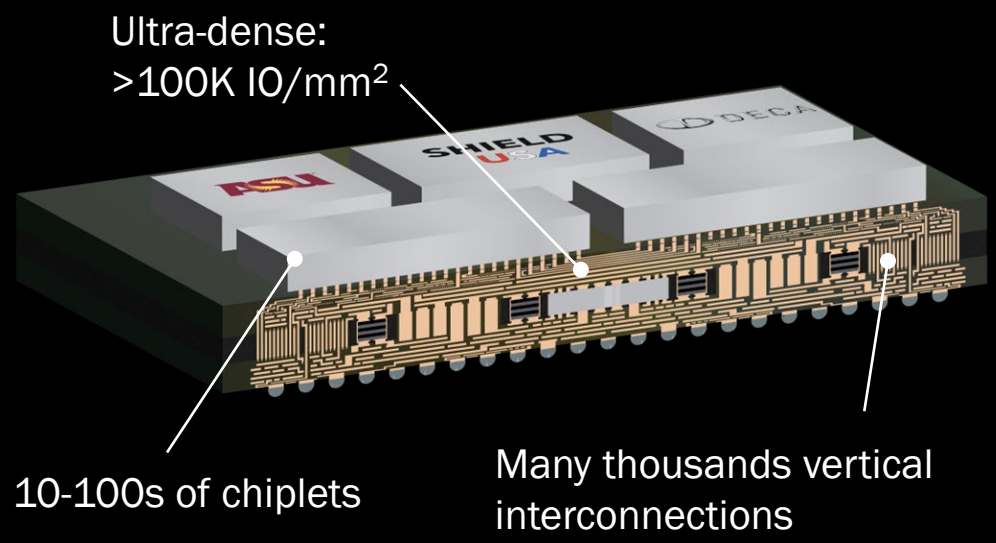
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Increased IO Density Drives New EDA Flows

PACKAGE-LEVEL ASSEMBLY
(mm-to-µm scale)



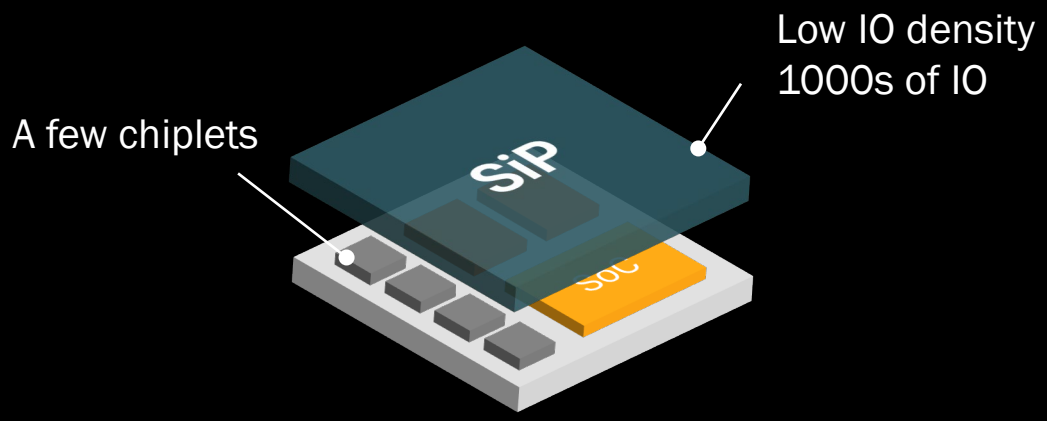
CHIPLET-INTEGRATION
(µm-to-nm scale)



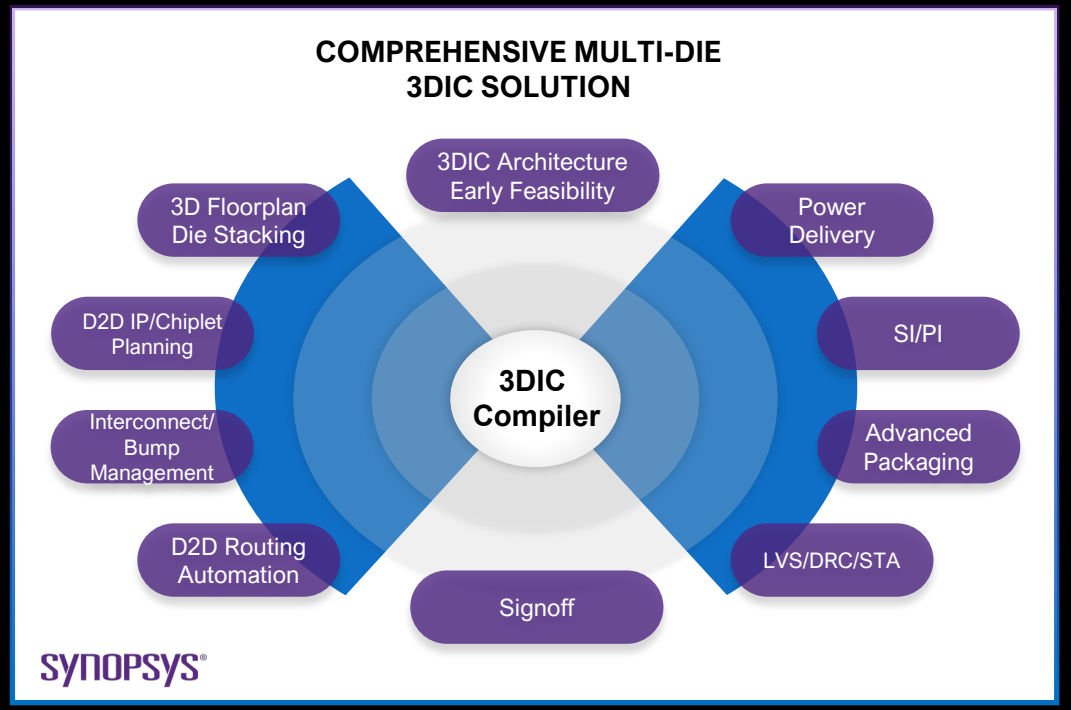
Design and optimization of stacks, chiplets and substrate must be performed together

Increased IO Density Drives New EDA Flows

PACKAGE-LEVEL ASSEMBLY
(mm-to-µm scale)



CHIPLET-INTEGRATION
(µm-to-nm scale)



Simultaneous floor-planning of chips and embedded components,
combined with IC-style design-rule-aware auto-routing

First Synopsys Engineering PDK Released

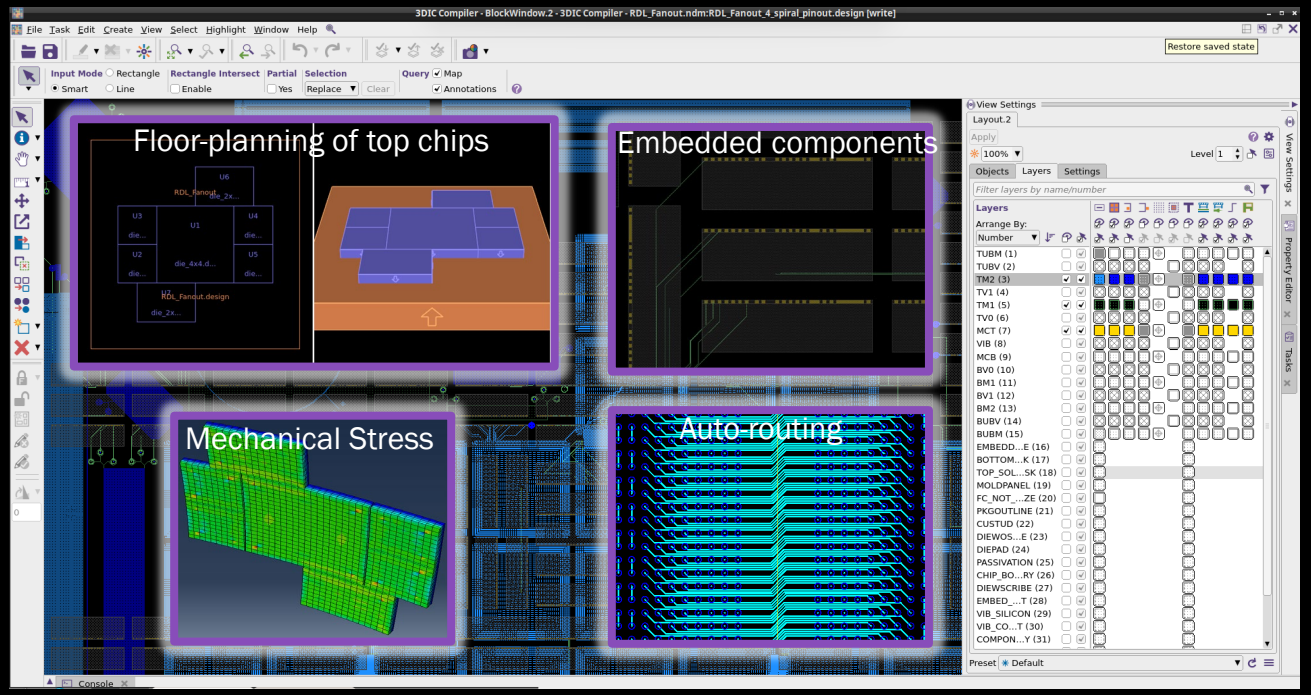
SHIELDUSA Design Kit

Documentation:
Design rule manuals, methodology guides and specs

EDA Collateral:
Tech files, DRC decks, libraries and automation

Electrical Modeling:
Tech files, material properties, libraries and specs

Thermomechanical & Reliability Modeling:
Tech files, material properties, models and specs

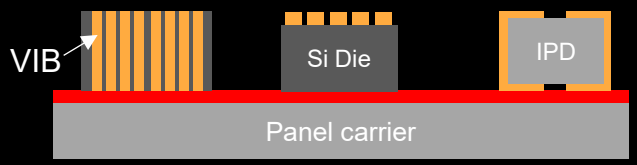


SHIELD USA multi-layer substrates with embedded components fully designed in Synopsys 3DIC Compiler

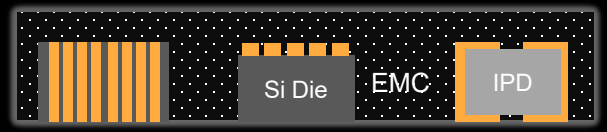
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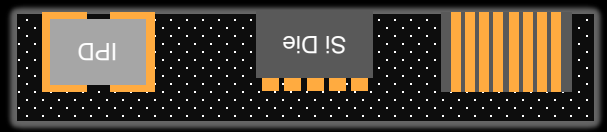
High Level Process Flow



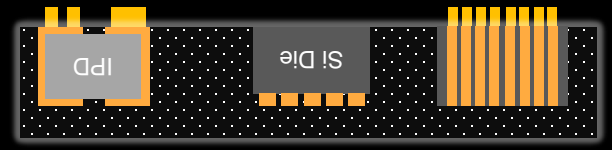
1. Die and component attach



2. Mold, debond and cure



3. Backgrind

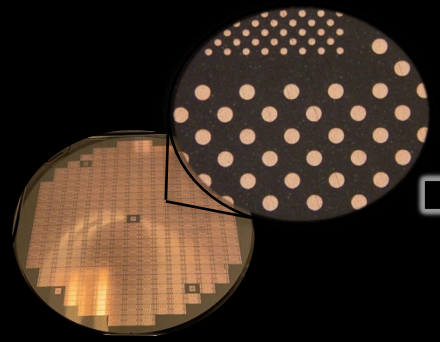


4. Adaptive Patterning and Via electroplating

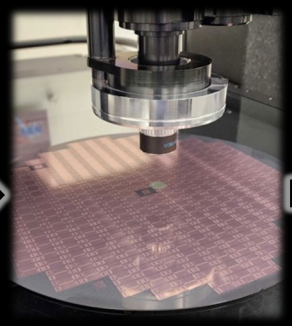
Solving die shift with Adaptive Patterning™ (AP)

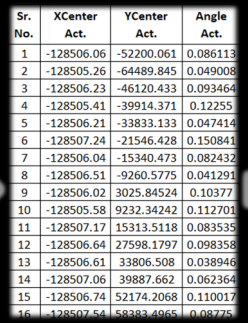
→ Unique lithography pattern optimized to ensure ideal contact and high-resolution interconnect precisely aligned to each embedded device

Adaptive Patterning Process Flow



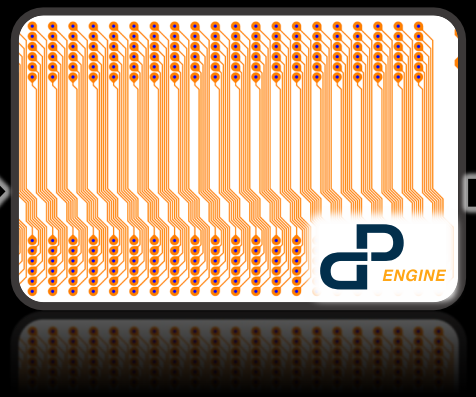
Measure actual die position using high-speed optical scanner





Sr. No.	XCenter Act.	YCenter Act.	Angle Act.
1	-128506.06	-52200.061	0.086113
2	-128505.26	-64489.845	0.049008
3	-128506.23	-46120.433	0.093464
4	-128505.41	-39914.371	0.12255
5	-128506.21	-33833.133	0.047414
6	-128507.24	-21546.428	0.150841
7	-128506.04	-15340.473	0.082432
8	-128506.51	-9260.5775	0.041291
9	-128506.02	3025.84524	0.10377
10	-128505.58	9232.34242	0.112701
11	-128507.17	15313.5118	0.083535
12	-128506.64	27598.1797	0.098358
13	-128506.61	33806.508	0.038946
14	-128507.06	39887.662	0.062364
15	-128506.74	52174.2068	0.110017
16	-128507.54	58383.4965	0.08775

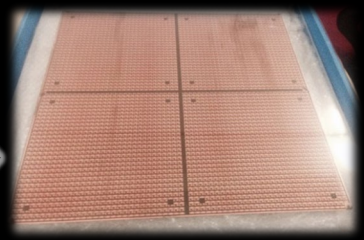
Die measurement data



Dynamically generate lithography pattern



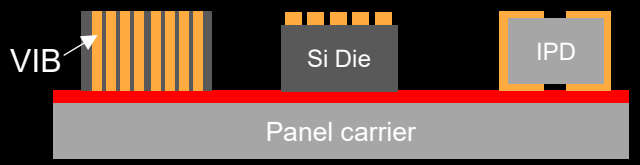
LDI Expose tool



Unique lithography pattern per panel
(no reticle size limitations)

1. Measure **2. Optimize** **3. Expose**

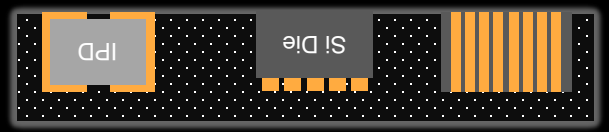
High Level Process Flow



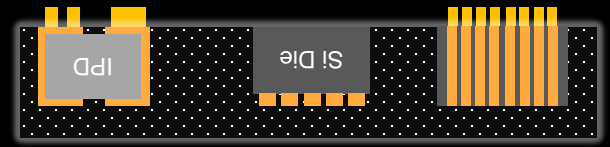
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2. Mold, debond and cure



3. Backgrind



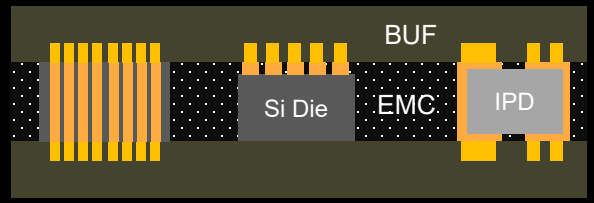
4. Adaptive Patterning and Via electroplating



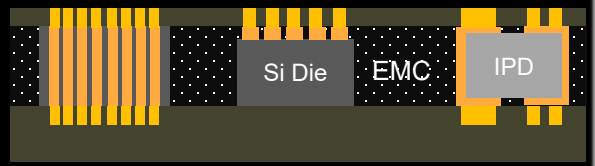
5. BUF application, flip & frontgrind



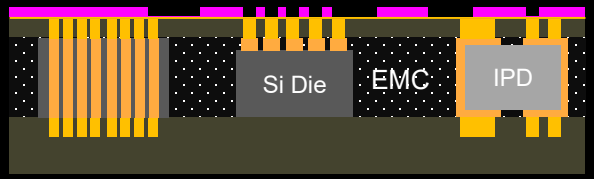
6. Adaptive Patterning and Via electroplating



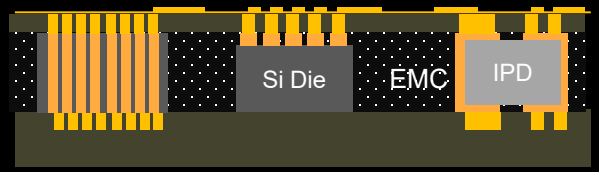
7. BUF application & cure



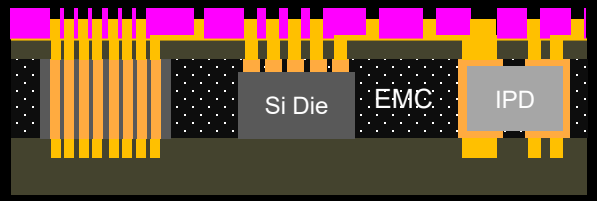
8. Grind & reveal front via



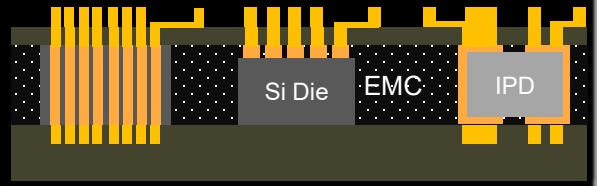
9. Seed deposition, PR application, expose & develop



10. Wiring (Cu) electroplating and resist strip



11. PR application, expose & develop Via (Cu) electroplating

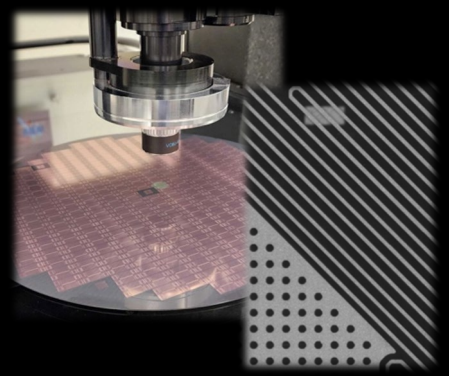


12. PR strip & seed etch

Repeat M-Series™ Direct (MDx) process for multi-layer dual-sided build-up

Robust Manufacturing – Even for Sub-micron Wires

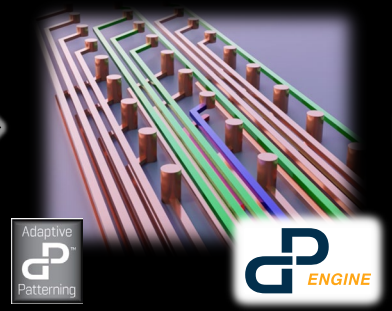
Extend Adaptive Patterning® Technology to Adaptive Defect Mitigation (ADM)



Optical inspection of fabricated layer



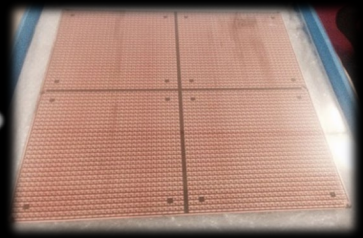
Defect map



Dynamically generate lithography pattern of subsequent layer



LDI Expose tool



Unique lithography pattern per panel
(no reticle size limitations)

1. Inspect

2. Re-route

3. Expose

Unique lithography pattern to ensure defect mitigation by dynamically re-routing around defects on subsequent layers

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Extending Fan-out Technology to Advanced Substrates

Large FF

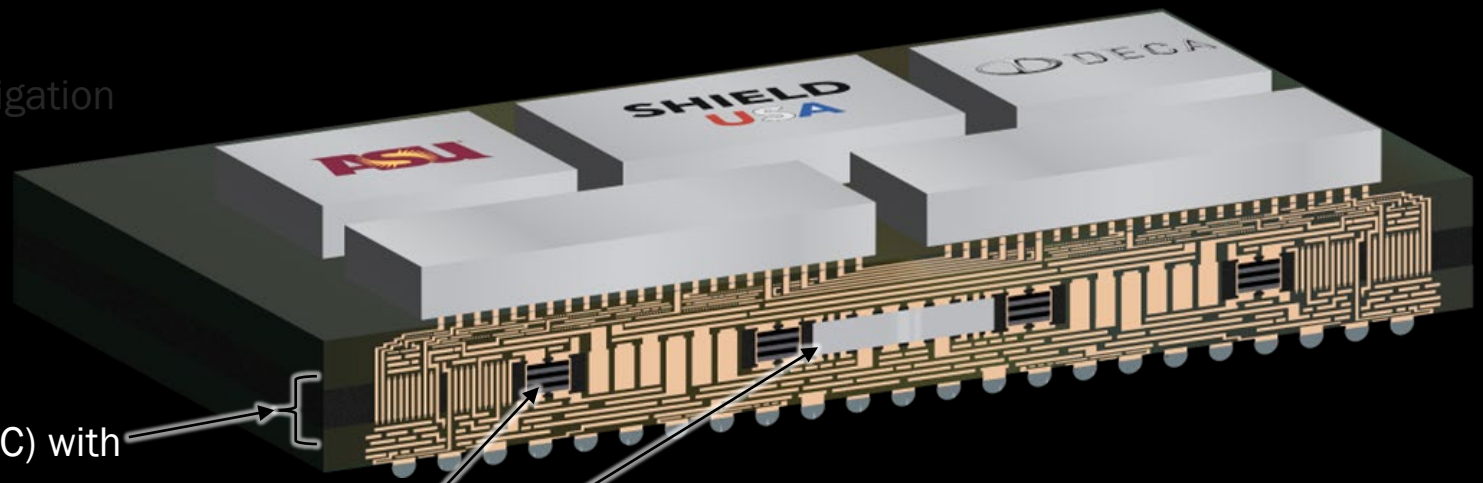
Functionality

IO density

No interposer layer
→ µbump pitch 25µm to sub-10µm roadmap

Robust manufacturing
→ Adaptive Defect Mitigation

Ultra-high density RDL on build-up film
→ L&S 2&2µm to 0.5µm&0.5µm roadmap
→ No capture pad vias (5µm to 2µm roadmap)

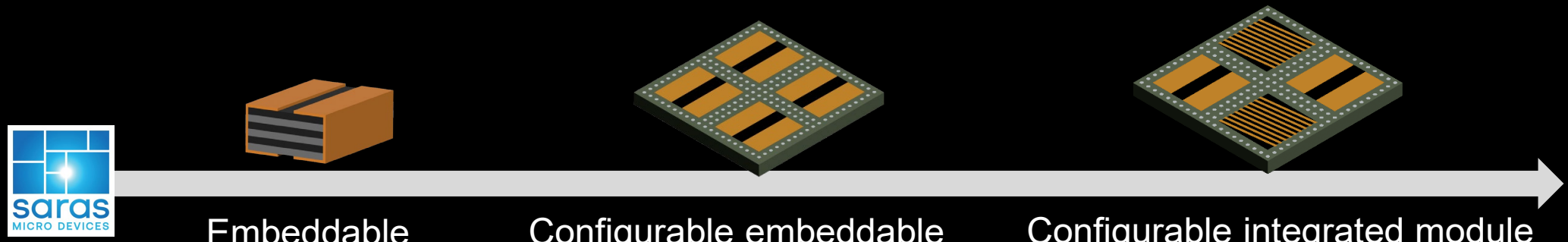


Molded fan-out core (MC) with embedded functionality

Embedded passives & actives
→ High density caps and inductors
→ Power management, RF, control

High aspect ratio embedded vertical interconnect blocks (VIBs)
→ 35µm to 20 µm pitch through-core

Key technologies – Embedded Functionality

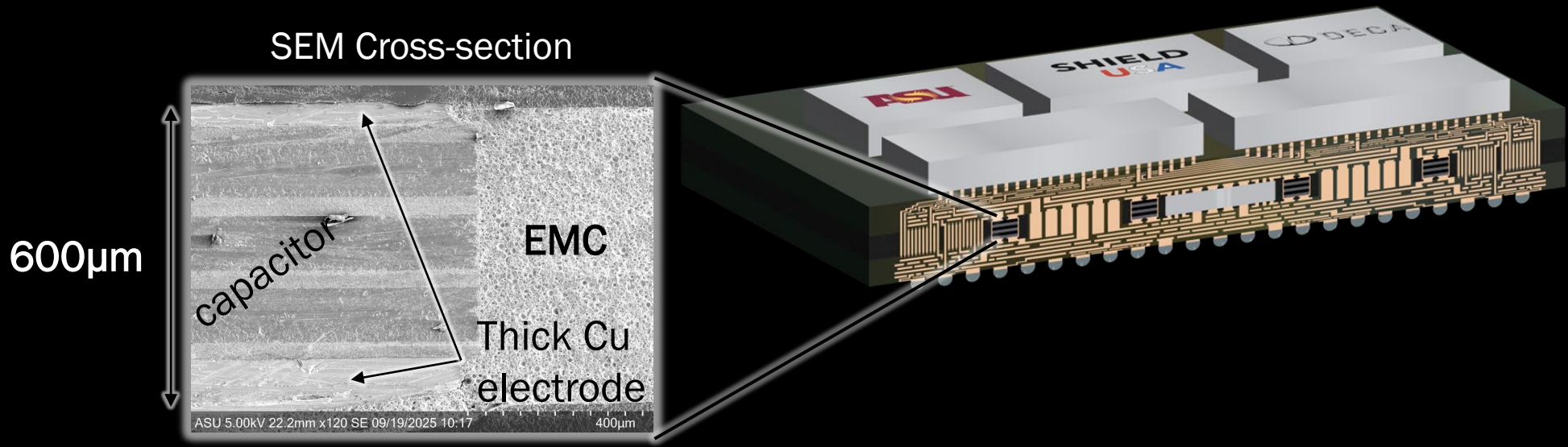


Embeddable capacitor

Configurable embeddable multi-domain module

Configurable integrated module with multiple capacitive and inductive domains

SEM Cross-section



Embedded passives and configurable modules enable improved PD architectures (e.g. vertical PD)

Extending Fan-out Technology to Advanced Substrates

Large FF

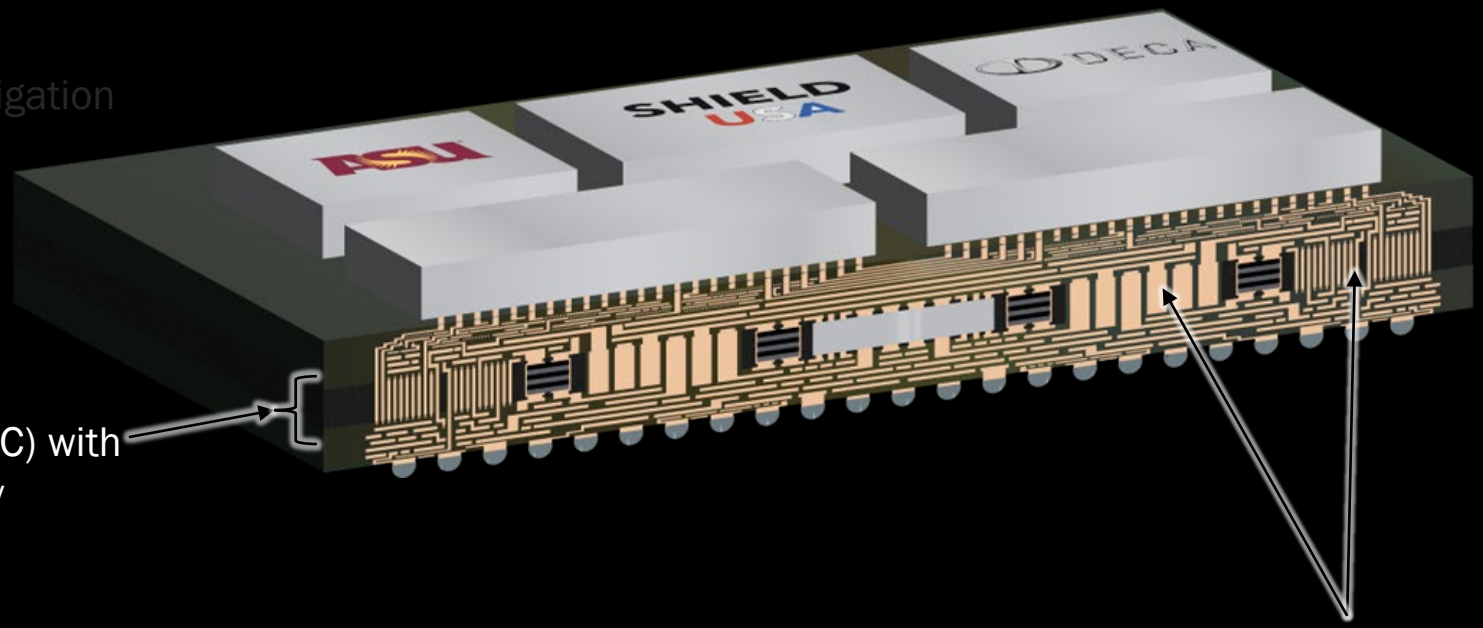
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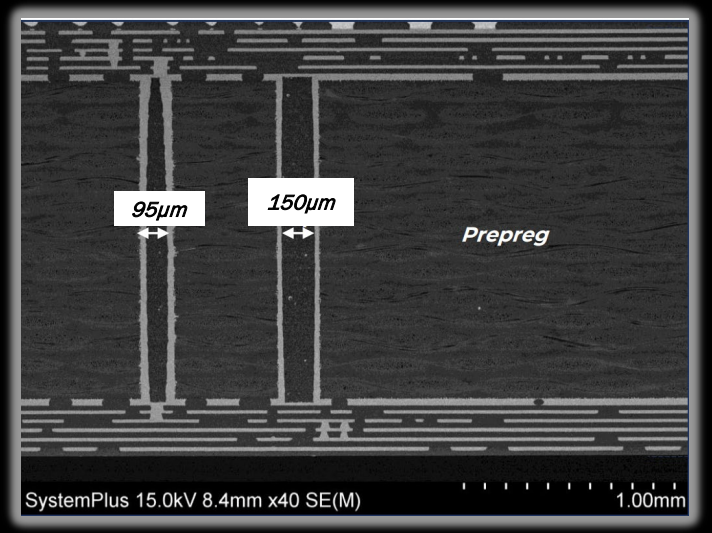
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SHIELDUSA

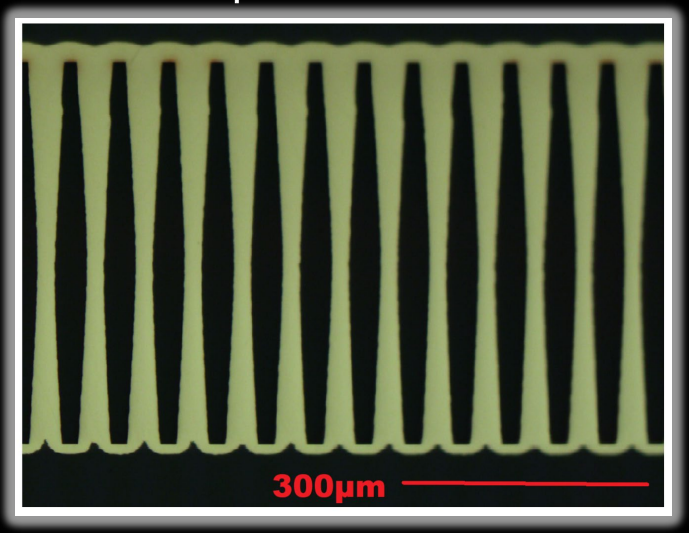
Breaking the Aspect Ratio Limitation of Through Core Vias

1.5mm Organic Core
100-150µm vias AR~10:1



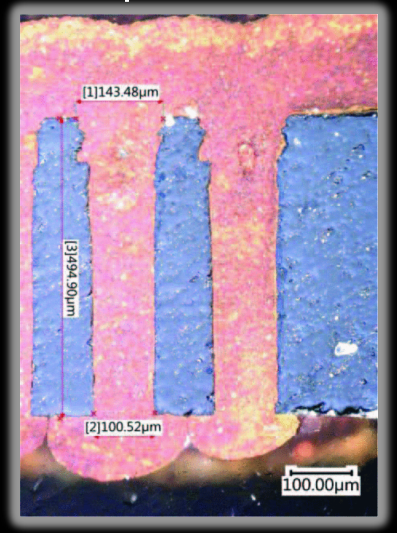
Source: nVIDIA H100 Teardown

450µm Glass Core
50µm vias AR~9:1



Source: Fraunhofer IZM, 2022

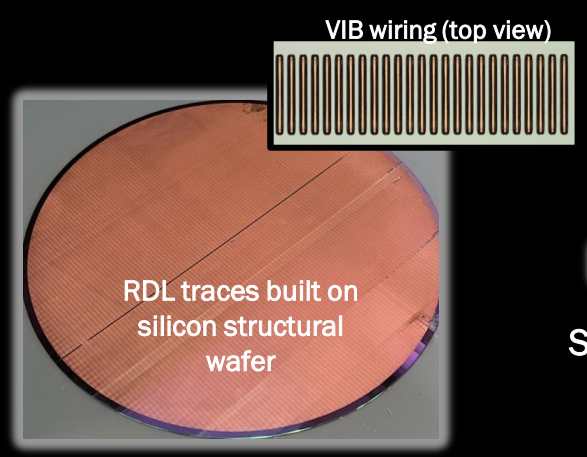
500µm Silicon Core
100µm vias AR~5:1



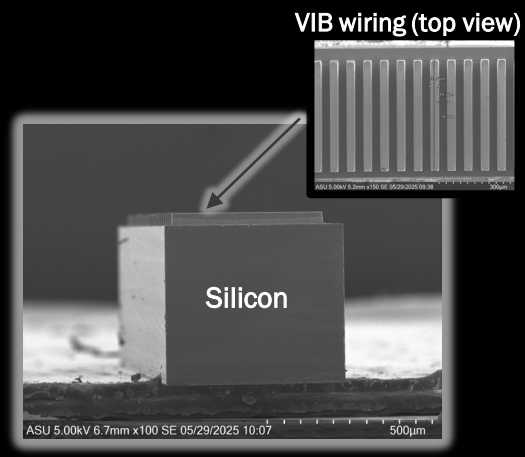
Source: UCLA Si IF, ECTC 2019

Today's substrates feature aspect-ratio limited through core vias limiting the embedding capability of thick components

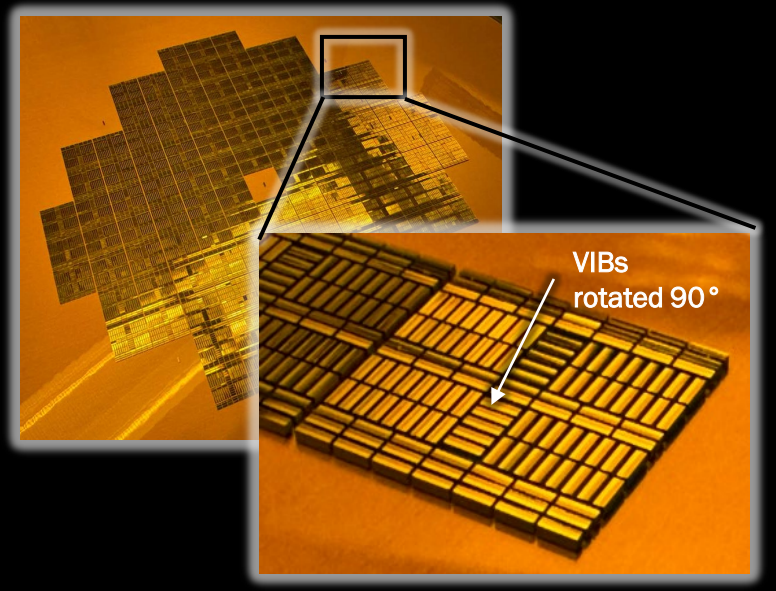
Key Technologies – Vertical Interconnect Blocks (VIB)



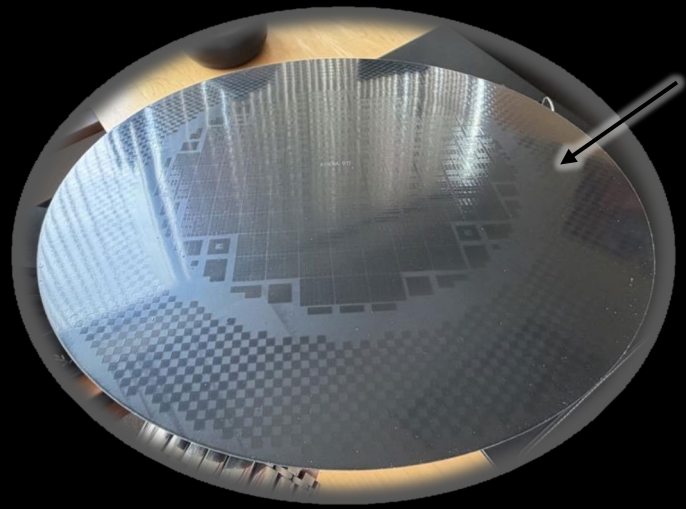
Singulation



90° flip during placement

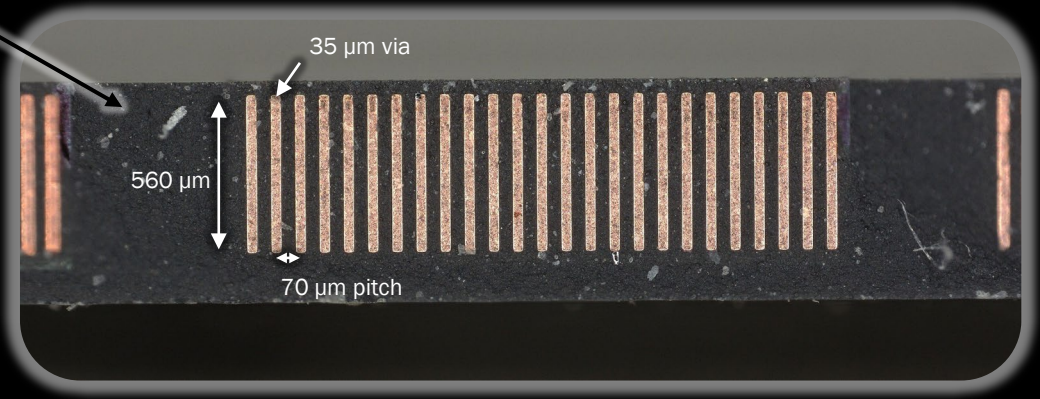


EMC encapsulation



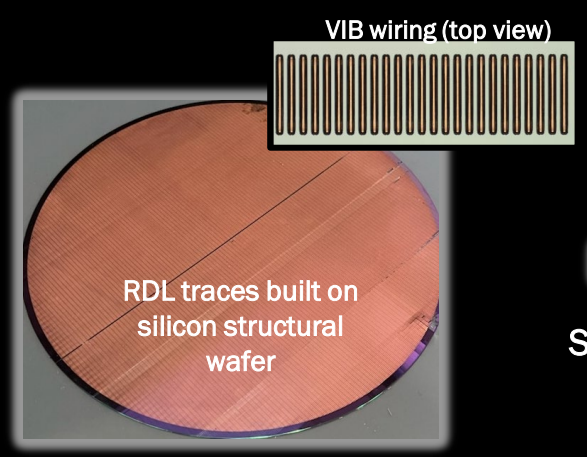
Epoxy Mold Compound (EMC)

X-section view: 16:1 through core transition

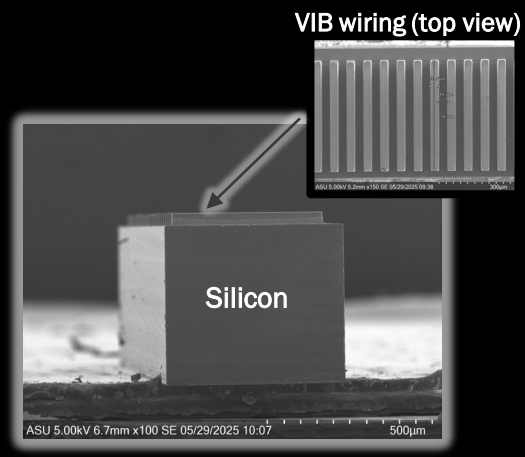


No aspect ratio limitation, VIBs allow thick component embedding (e.g. 1.5mm, AR 56:1)

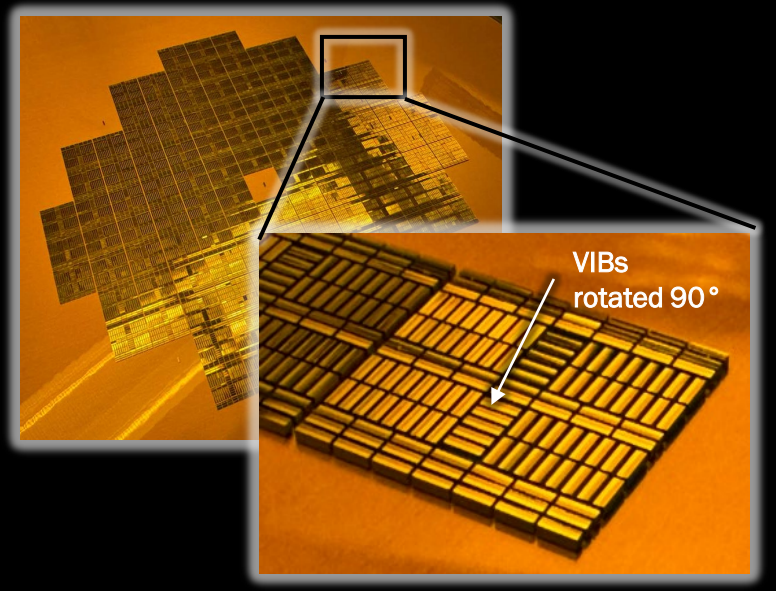
Key Technologies – Vertical Interconnect Blocks (VIB)



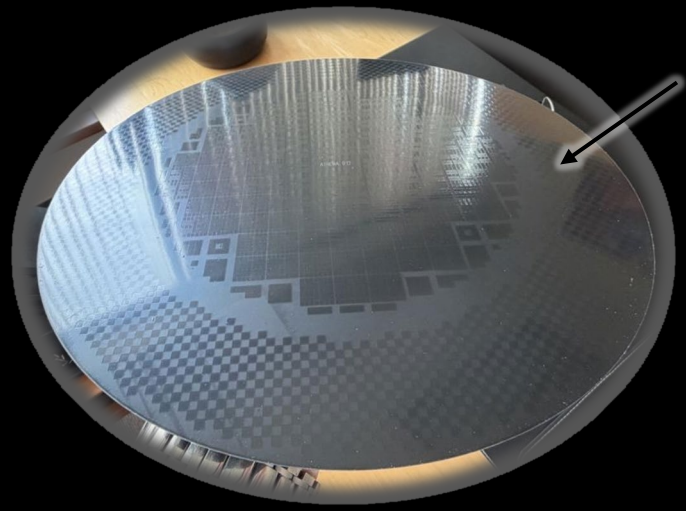
Singulation



90° flip during placement

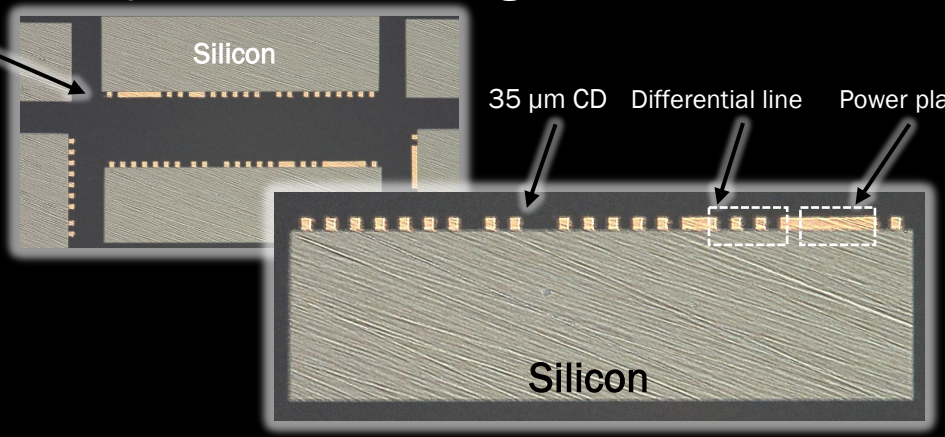


EMC encapsulation



Epoxy Mold Compound (EMC)

Top-down view: VIBs ground and revealed



VIBs allow wide power planes and differential transitions through the core

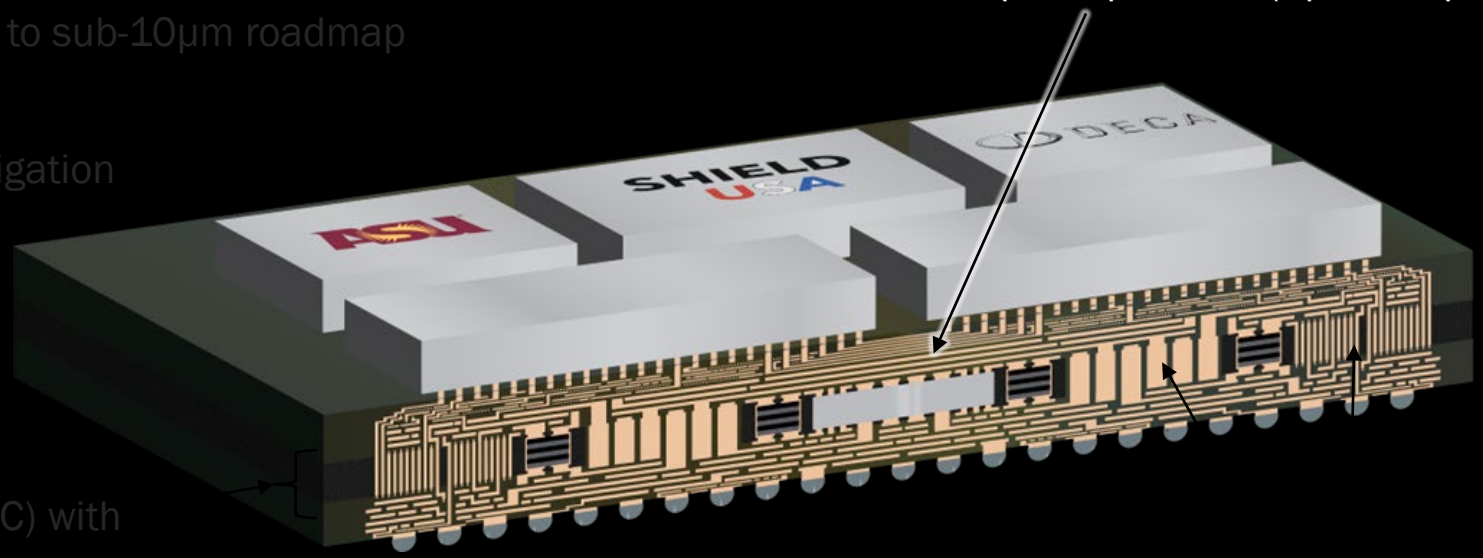
Extending Fan-out Technology to Advanced Substrates

Large FF

No interposer layer
→ µbump pitch 25µm to sub-10µm roadmap

Robust manufacturing
→ Adaptive Defect Mitigation

Ultra-high density RDL on build-up film
→ L&S 2&2µm to 0.5µm&0.5µm roadmap
→ No capture pad vias (5µm to 2µm roadmap)



IO density

Functionality

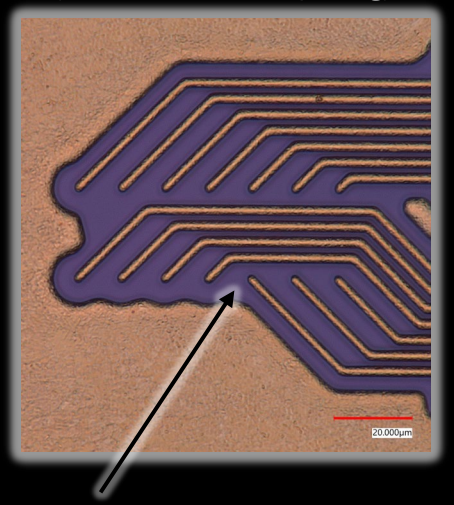
Molded fan-out core (MC) with
embedded functionality

Embedded passives & actives
→ High density caps and inductors
→ Power management, RF, control

High aspect ratio embedded
vertical interconnect blocks (VIBs)
→ 35µm to 20 µm pitch through-core

Key Technologies – Ultra High Density Planarized Wiring

Top View
(1st RDL, before via plating)



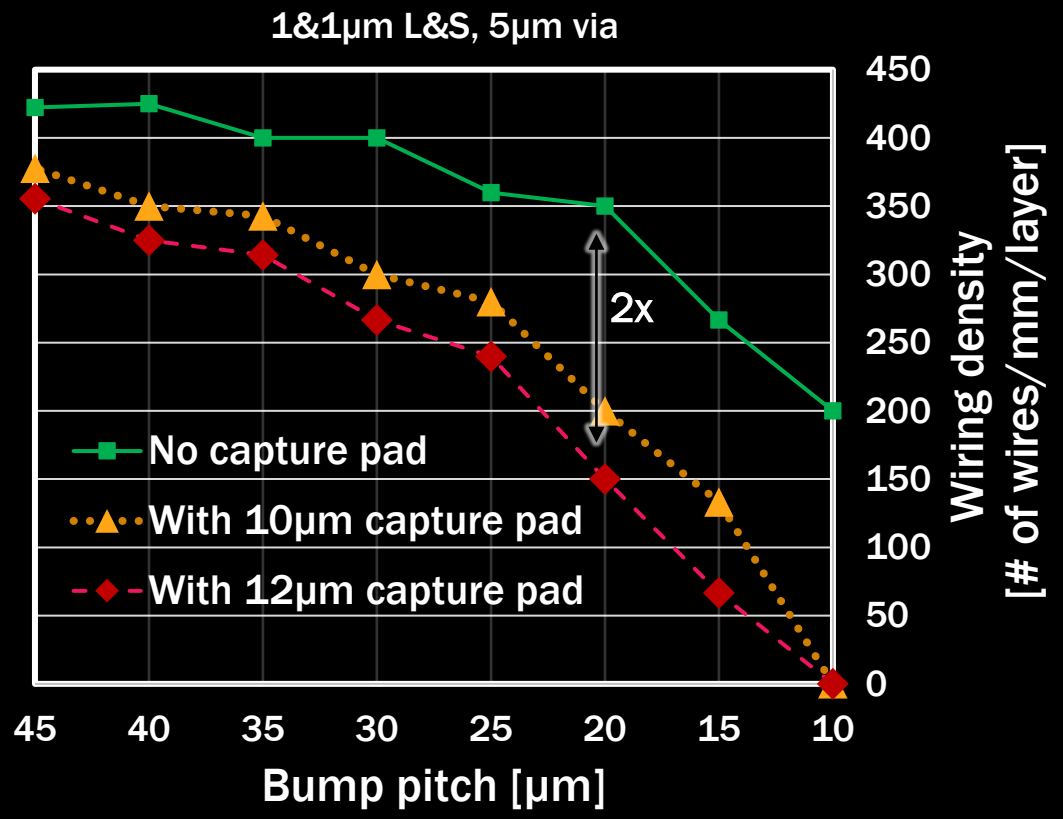
2μm L&S
NO capture pads!



With
capture pad



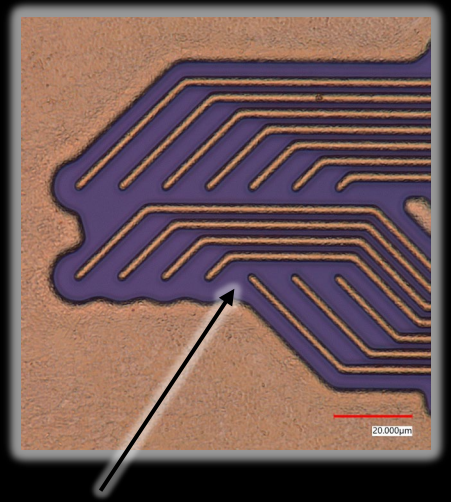
No
capture pad



No capture-pad vias enable >2x wiring density improvement

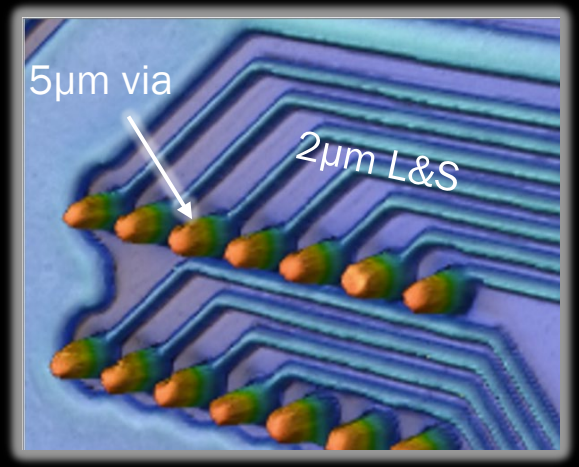
Key Technologies – Ultra High Density Planarized Wiring

Top View
(1st RDL, before via plating)

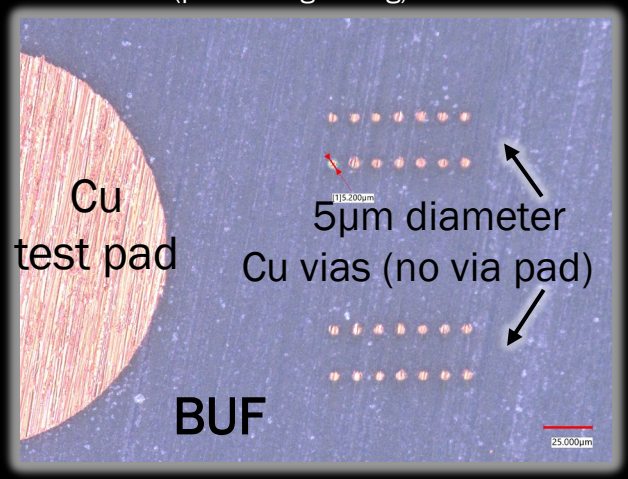


2µm L&S
NO capture pads!

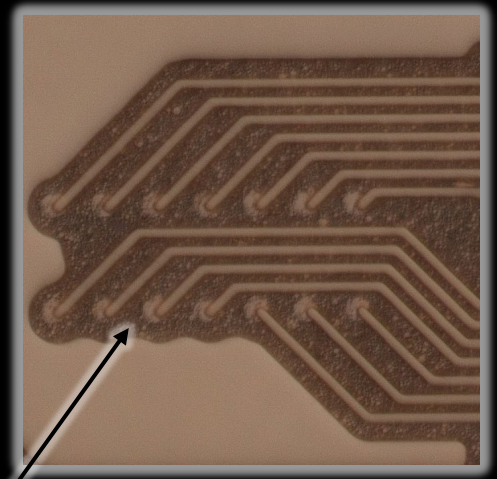
Isometric View
(post via plating)



Top View
(post BUF grinding)



Top View
(post RDL plating)

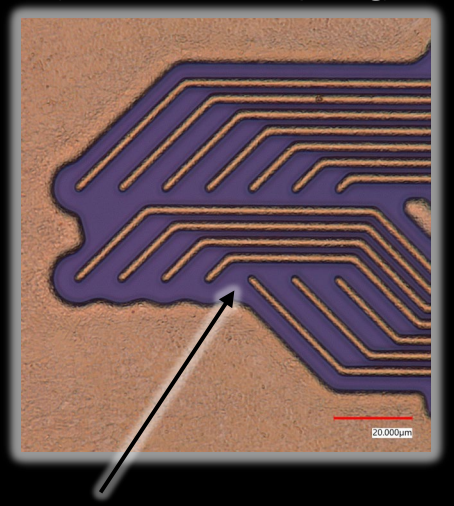


2µm L&S
NO capture pads
Direct trace to via contact

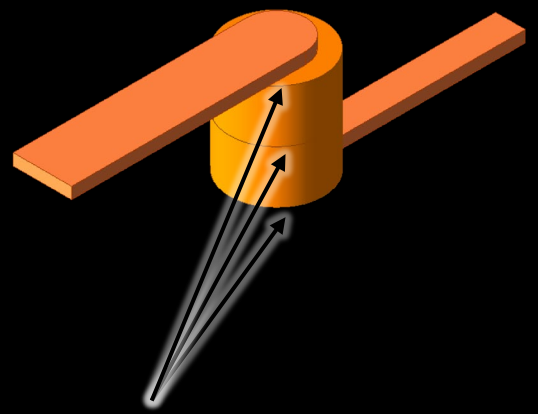
No capture-pad vias (5µm) and 2µm L&S traces enable high density routing

Key Technologies – Ultra High Density Planarized Wiring

Top View
(1st RDL, before via plating)

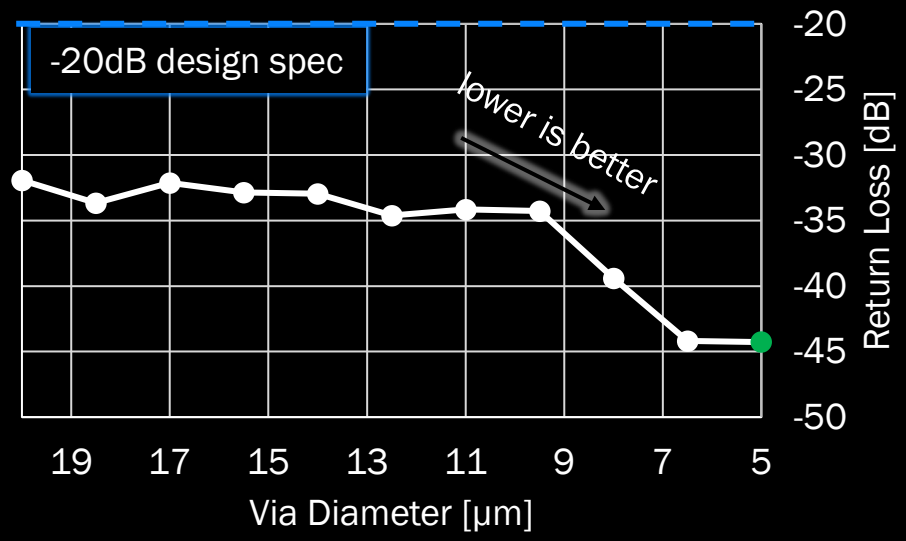


2µm L&S



2x stack via
NO capture pads
at any interface

Stacked via simulated @**140GHz**



No capture-pad stacked vias enable almost reflection-less transitions through the substrate layers

Outline

- Introduction
- SHIELD USA
- Electronic Design Automation
- Process Flow
- Key Technologies
- Conclusion

Come and visit us in Booth 204 !

Large FF

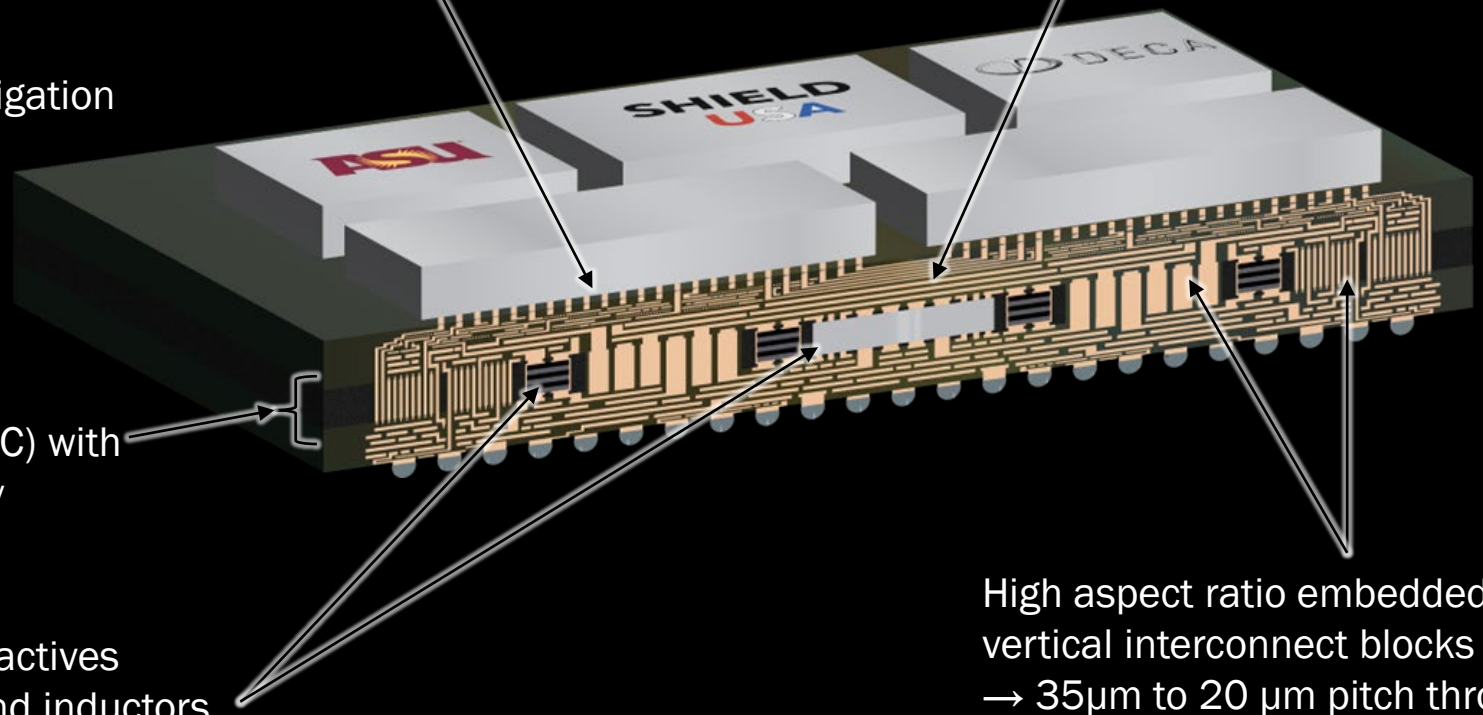
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Molded fan-out core (MC) with embedded functionality

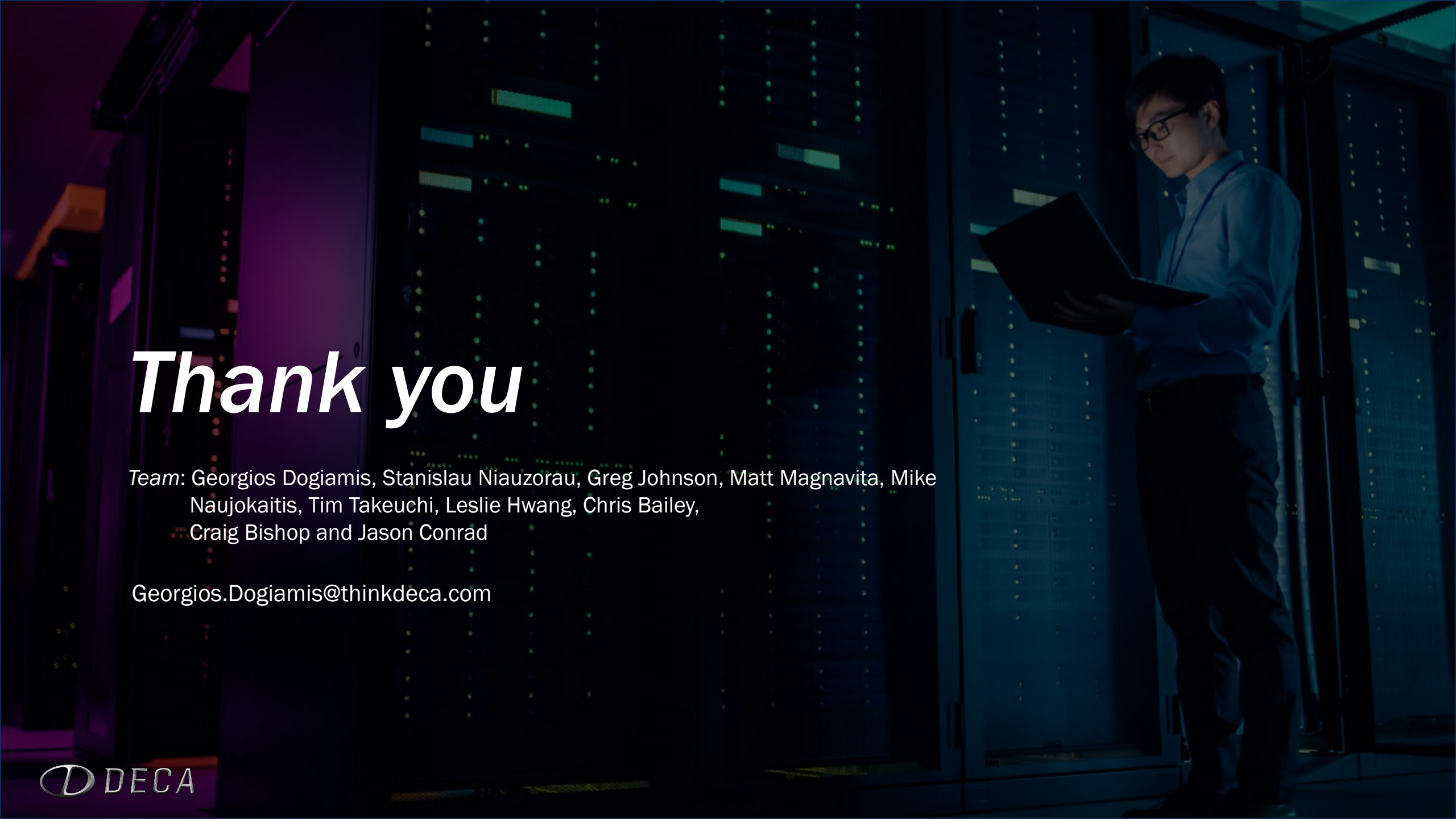
Embedded passives & actives
→ High density caps and inductors
→ Power management, RF, control

High aspect ratio embedded vertical interconnect blocks (VIBs)
→ 35µm to 20 µm pitch through-core
→ Thick power plane through core
→ Truly coaxial transitions through core

Delivering across the three key AI technology imperatives

DECA

SHIELDUSA



Thank you

Team: Georgios Dogiamis, Stanislau Niauzorau, Greg Johnson, Matt Magnavita, Mike Naujokaitis, Tim Takeuchi, Leslie Hwang, Chris Bailey, Craig Bishop and Jason Conrad

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DECA