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Reducing Wafer-to-Wafer Bonding Misalignment to Enable 140nm Pitch Hybrid Bonding

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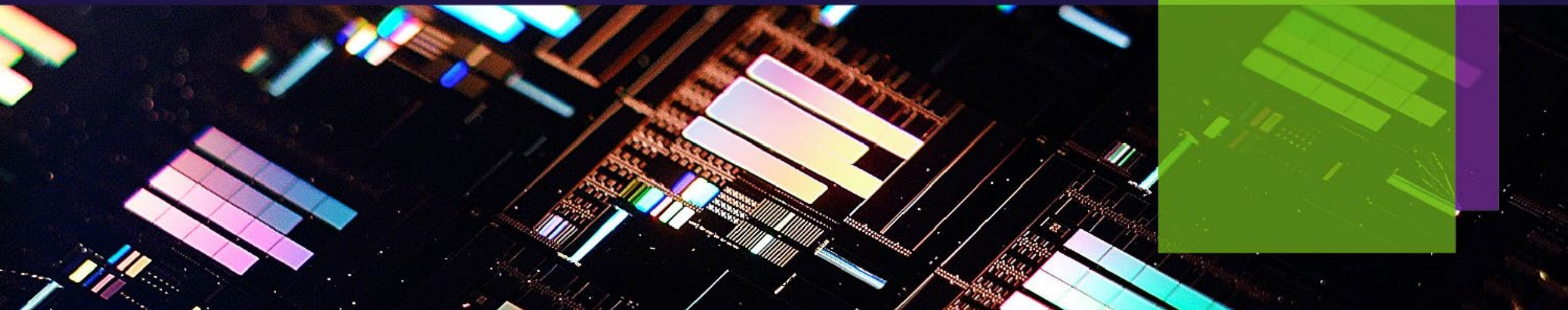
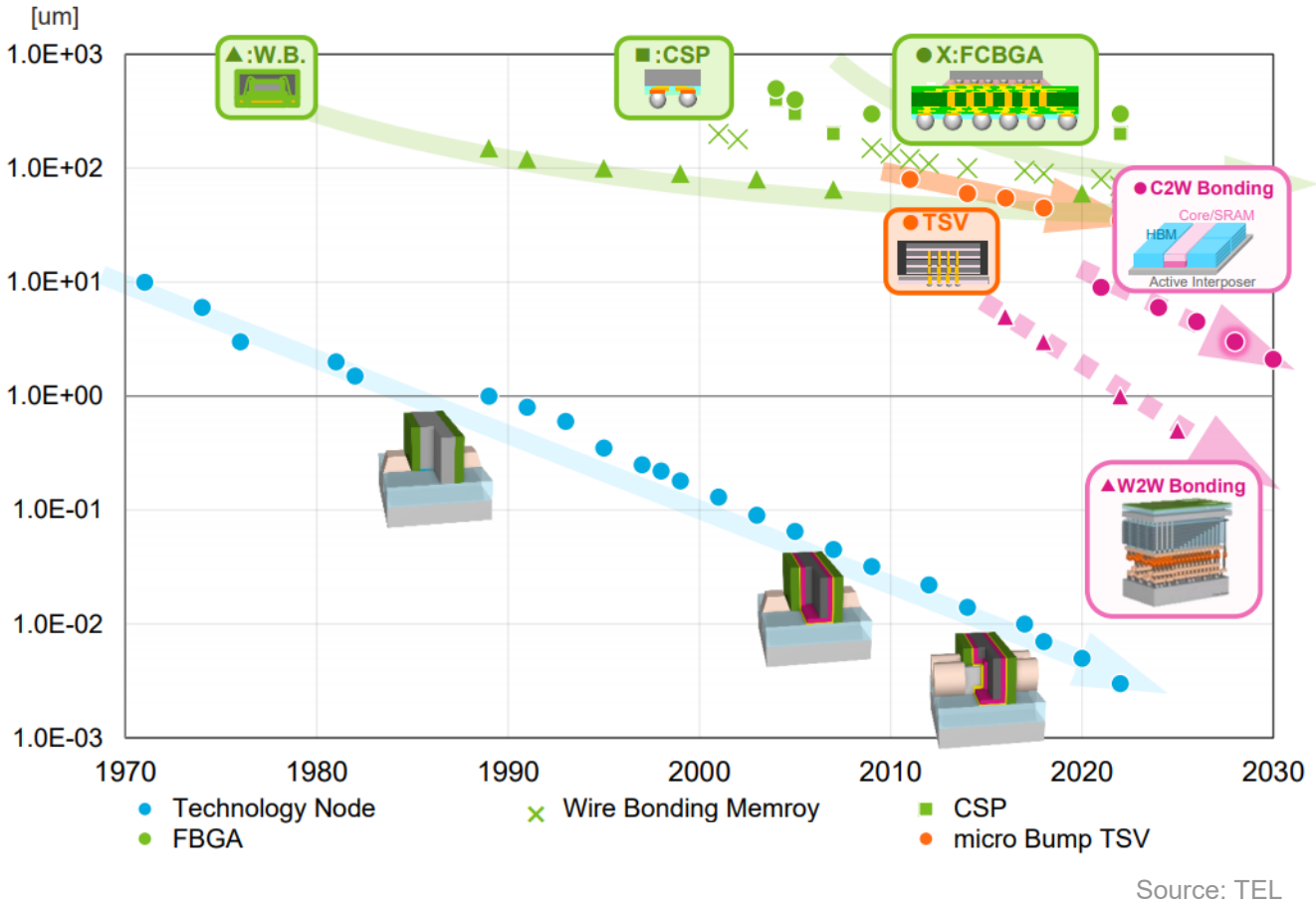


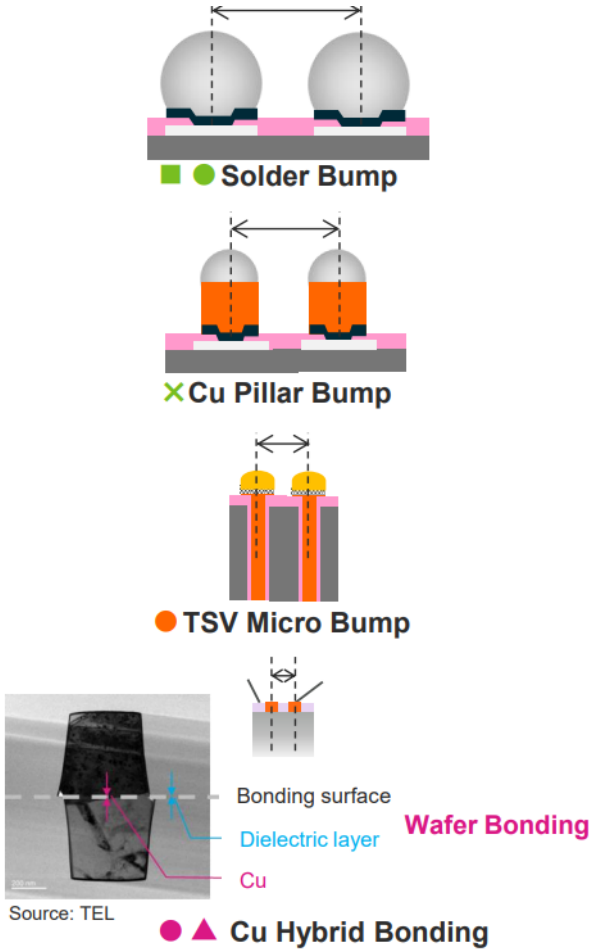
Outline

- Hybrid Bonding Background
- 140nm Pitch Hybrid Bonding Results
- Further Reducing Bonding Misalignment Residuals
- Conclusions and Next Steps

Semiconductor Technology Node and Bump Pitch

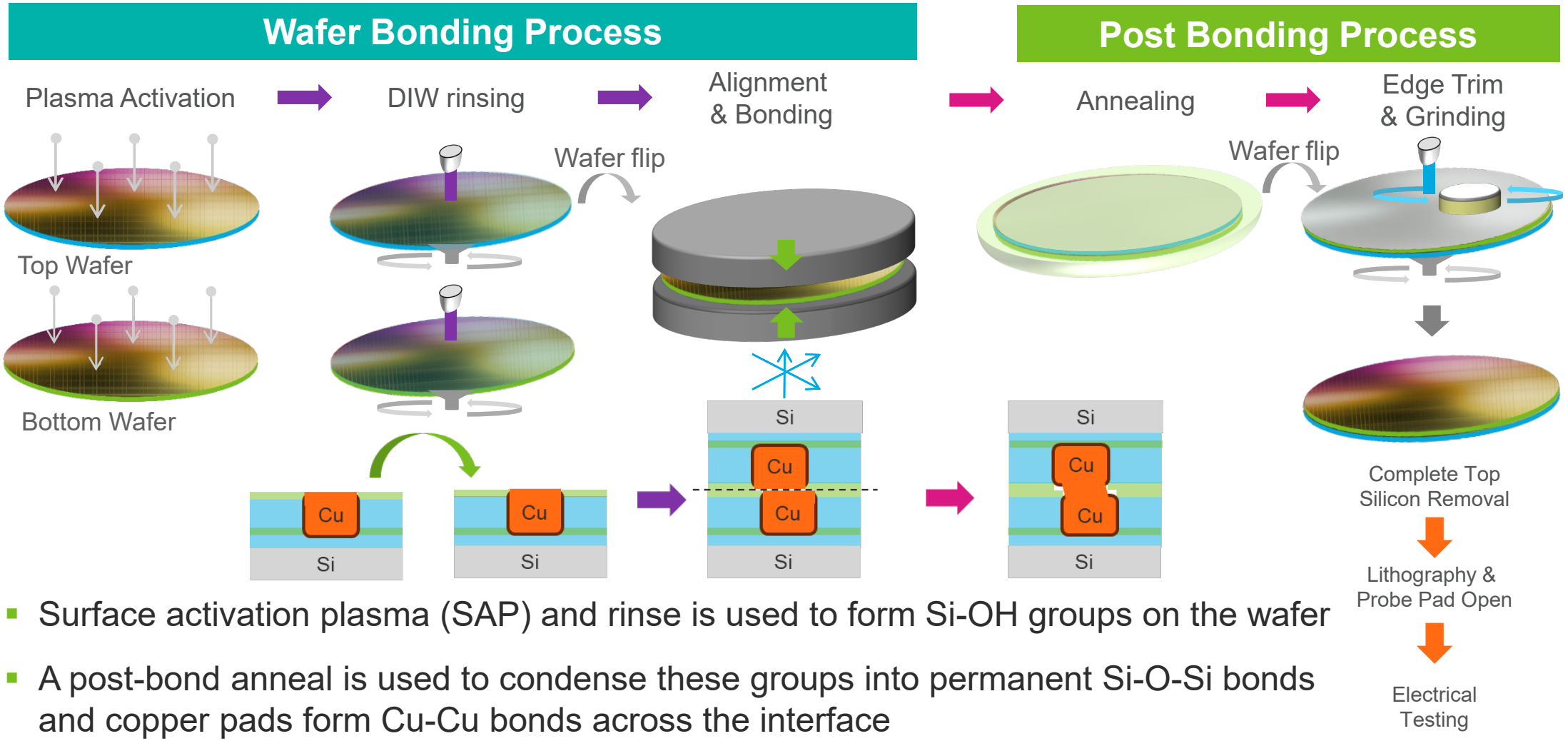


Source: TEL



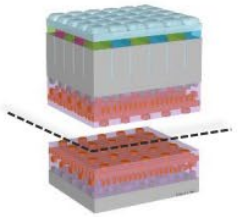
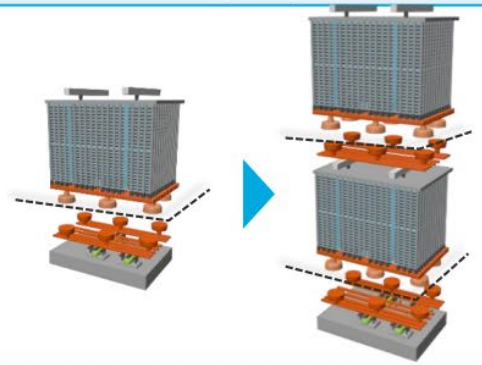
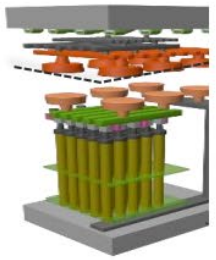
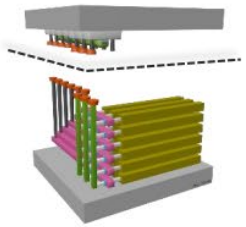
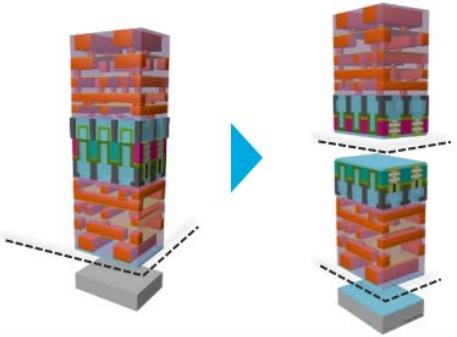
Chip-to-Wafer and Wafer-to-Wafer hybrid bonding enables <10um pad pitch for advanced nodes

Wafer-to-Wafer Hybrid Bonding Process Flow



- Surface activation plasma (SAP) and rinse is used to form Si-OH groups on the wafer
- A post-bond anneal is used to condense these groups into permanent Si-O-Si bonds and copper pads form Cu-Cu bonds across the interface

Wafer Bonding Applications (Frontend)

Application	Frontend Process				
	CIS*1	NAND	DRAM		Logic
Stacking Device	BSI*2 Pixel + (Peripheral) + Logic	3D NAND Cell + Peripheral ⋮ + Cell + Cell + Peripheral	VCT*5 DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	3D DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	BSPDN Logic + Si Substrate BSPDN & CFET Logic + Logic + Si Substrate
Bonding	Wafer to Wafer (CHB*3/Fusion)	Wafer to Wafer (CHB)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (HB*6/Fusion)
Structure					
Status	HVM*4	R&D~HVM R&D	R&D	R&D	R&D~HVM R&D

*1 CIS: CMOS Image Sensor
*2 BSI: Backside Illumination
*3 CHB: Cu Hybrid Bonding
*4 HVM: High Volume Manufacturing
*5 VCT: Vertical Channel Transistor
*6 HB: Hybrid Bonding

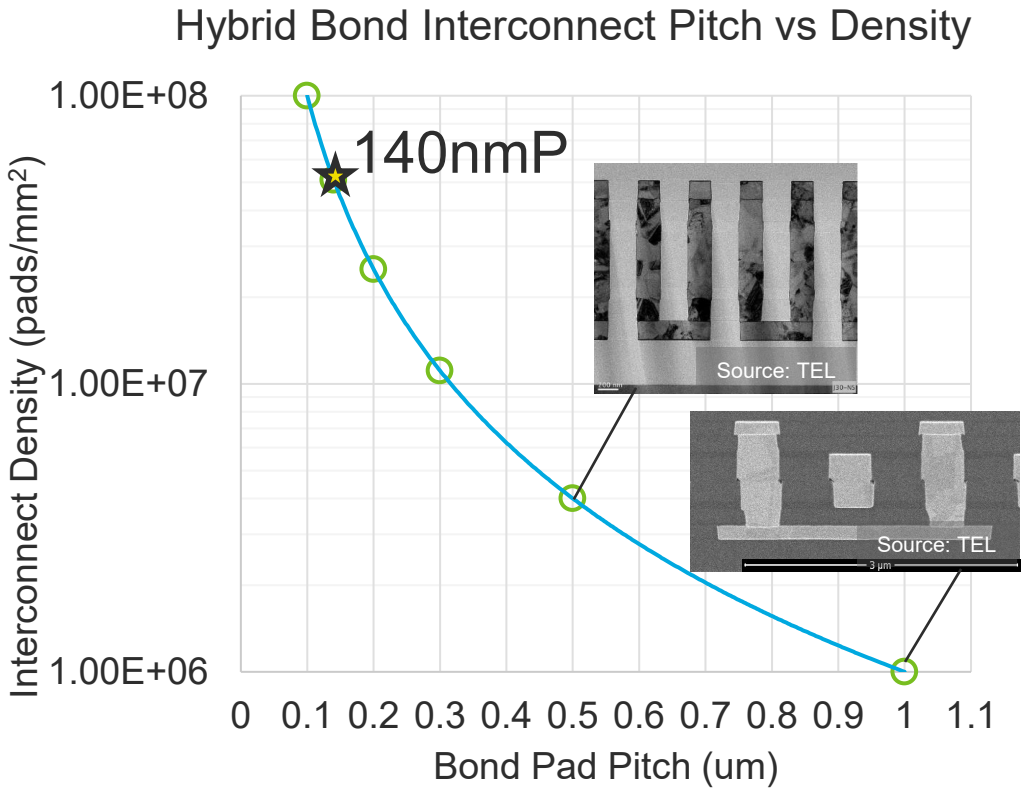
Source: TEL

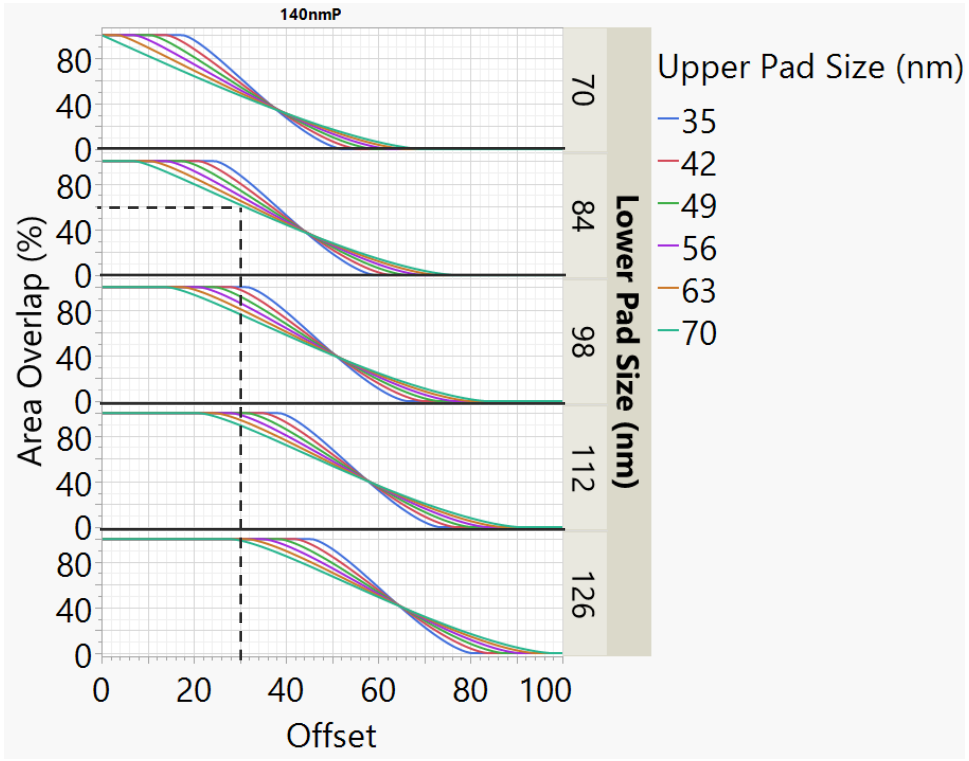
Wafer Bonding Applications (Advanced Packaging)

Application	Advanced Package		
	Stack Memory / HBM	3DIC	
Stacking Device	DRAM Wafer DRAM Wafer + DRAM Wafer + Logic Wafer OR DRAM ( ) Die DRAM ( ) Die + DRAM ( ) Die + Logic Wafer	SoC Disaggregation Device A Wafer + Device AorB Wafer OR A, B, C Die, Wafer	Heat Spreader Heat Spreader + Device
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)	Wafer to Wafer (Fusion)
Structure	**Micro Bump** → ***Cu hybrid*** (More stacks) Change • Thinner die / more stacks • High density connection • Better thermal conductance Cu	**Monolithic SoC** → ***3D Stack IC*** SRAM, CPU/GPU, I/O& Peripheral Change • Small formfactor (3D stack vs. 2D) • Higher speed (shorter wiring, no bump) • Lower power (shorter wiring, no bump) • Lower cost (higher yields, easy to mix processes) • Shorter time to market (matured IP block reuse)	Heat Spreader • Better thermal conductance
Status	R&D	R&D ~ HVM	HVM

Source: TEL

TEL Hybrid Bonding Test Vehicle Background



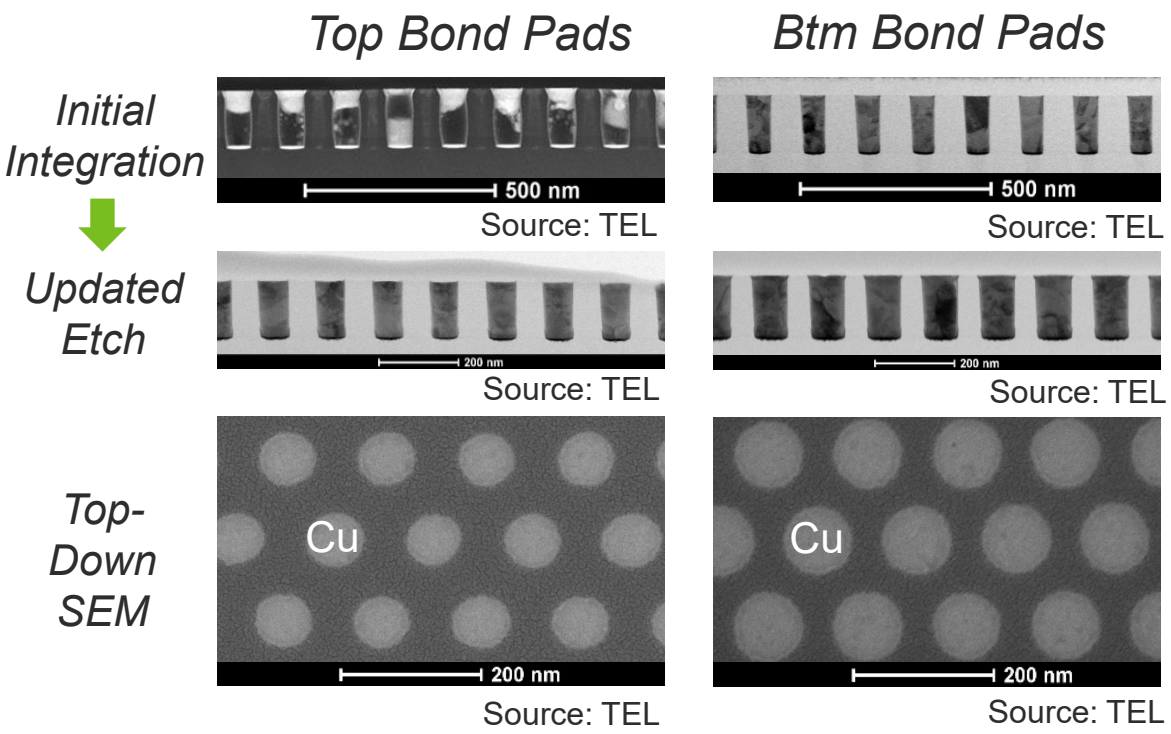


Source: TEL

- TEL previously demonstrated 0.5um and 1um pitch hybrid bonding with E-test yield >98%
- To meet growing demand for increased I/O, 140nm pitch bonding test vehicle is proposed
- Previous study showed bonding via resistance is stable if bond misalignment is < 50% of pad diameter
- For this test vehicle, slightly larger bottom bond pad is chosen to increase misalignment tolerance

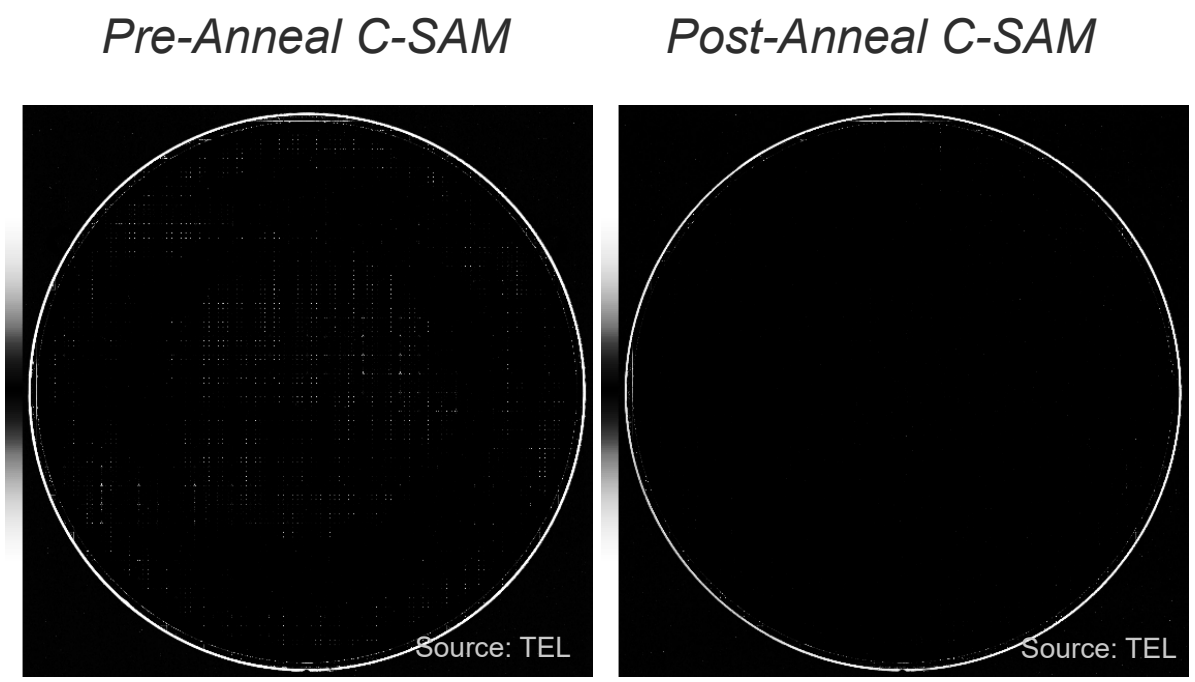
140nm Pitch Hybrid Bonding Test Vehicle (Bond Pad Only)

Incoming Wafer Optimization



- Integration optimized to reach target bond pad diameter (72nm Top and 84nm Btm)

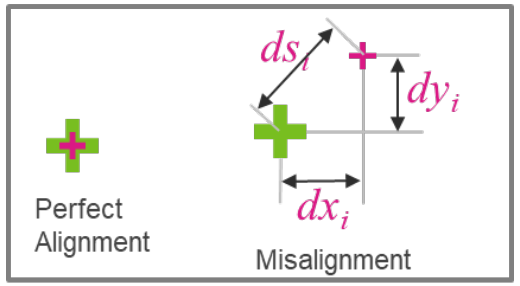
Bonding Demonstration

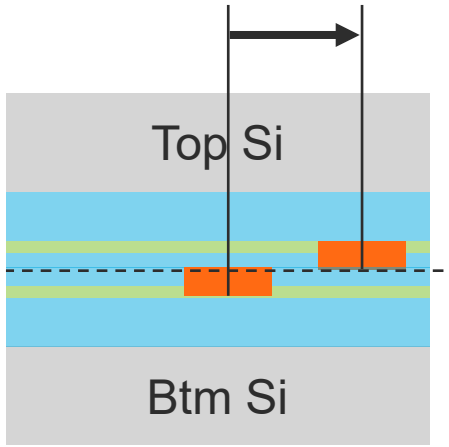


- Void-free 140nm pitch hybrid bonding after 350°C 1hr post-bond annealing

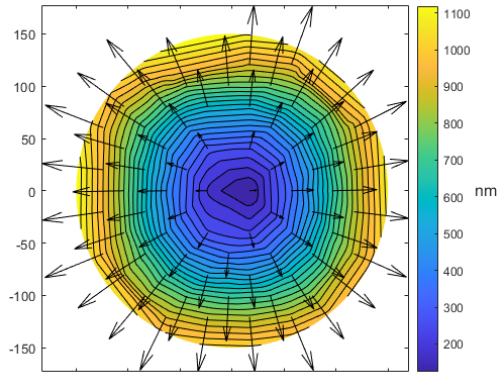
Measuring Bonding Overlay (4-Term Linear Alignment Model)





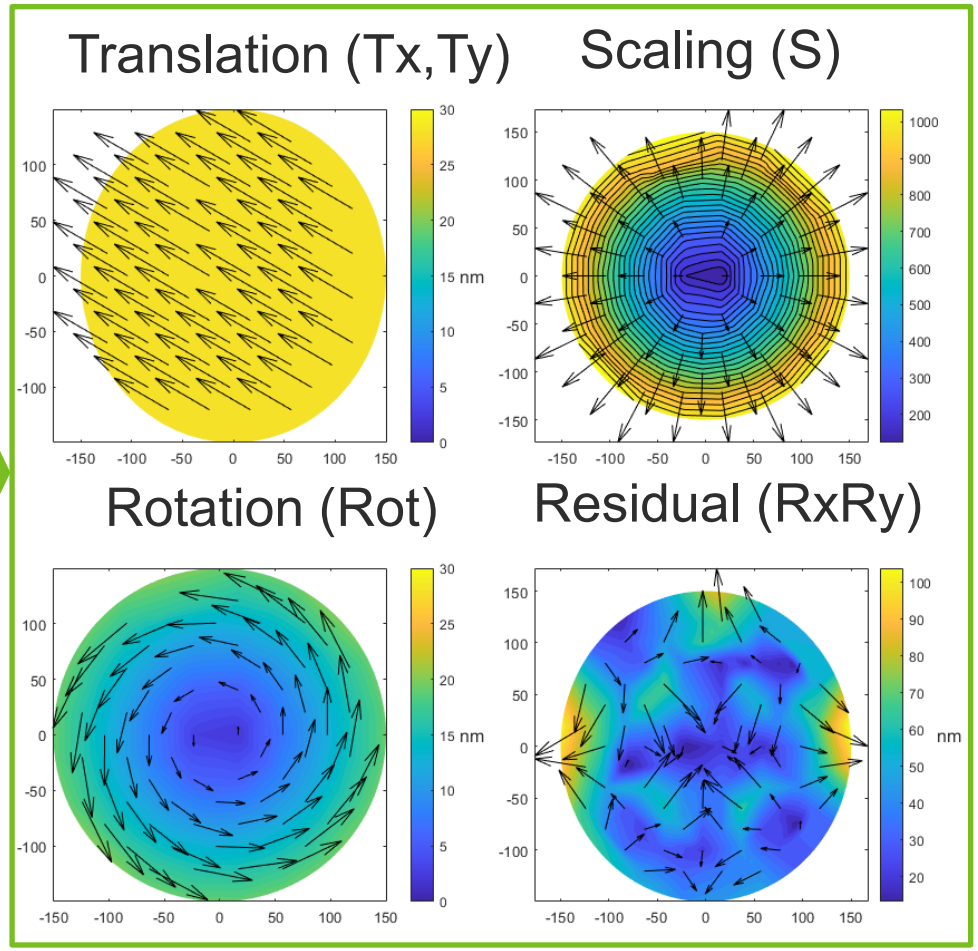


Misalignment (DxDy)

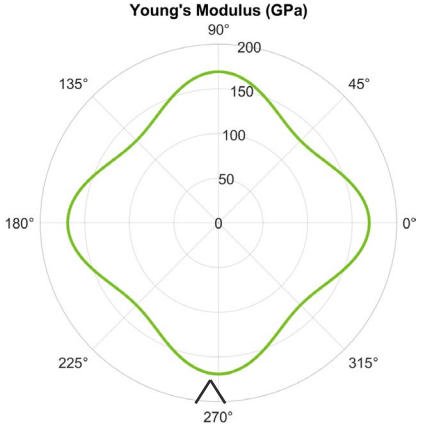


Source: TEL

*DxDy = Tx + Ty + S + Rot + **RxRy***

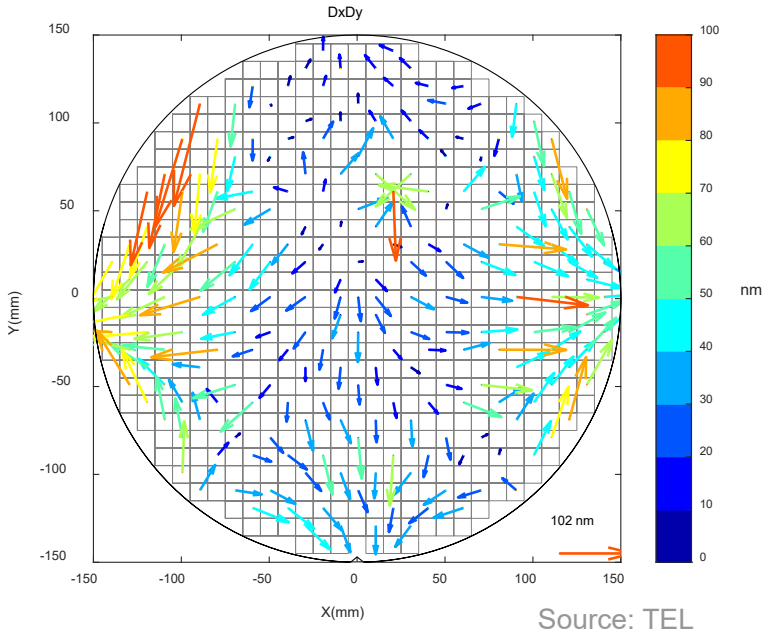


Si (100)
4-fold Properties



Source: TEL

140nm Pitch Measured Bonding Misalignment



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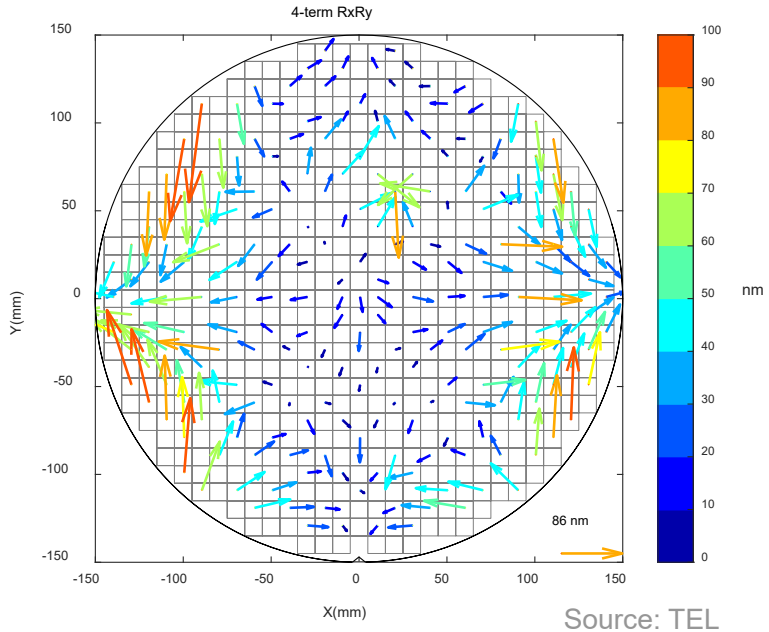
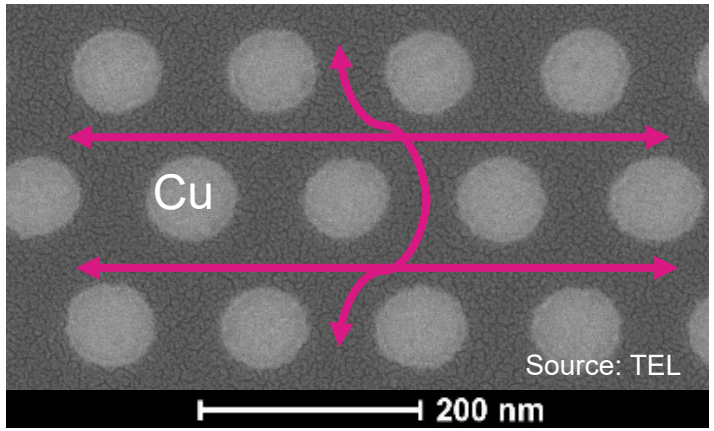


Source: TEL

Top-Down SEM Bond Pads



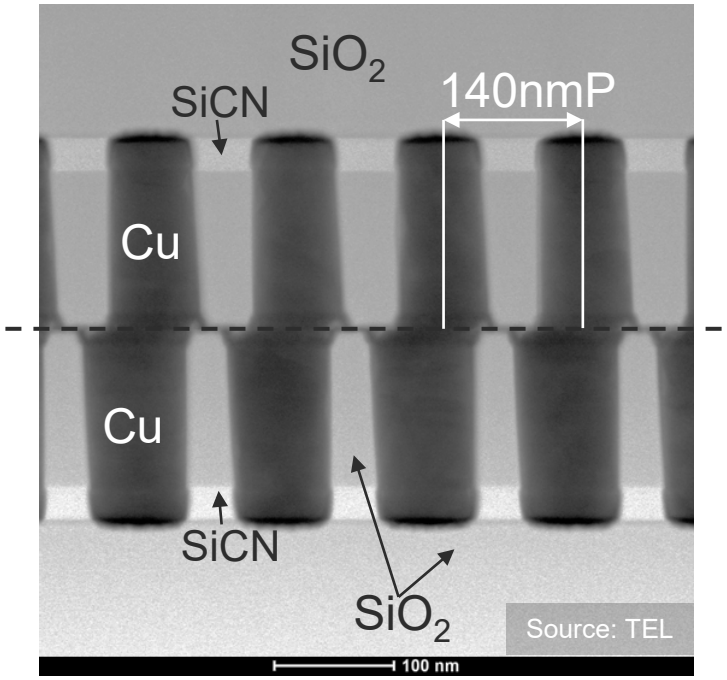
Bond propagation

Tx (nm)	Ty (nm)	Rotation (urad)	Scaling (ppm)	Res X M+3σ(nm)	Res Y M+3σ(nm)
0.1	-13.1	0.07	0.13	85.6	111.4

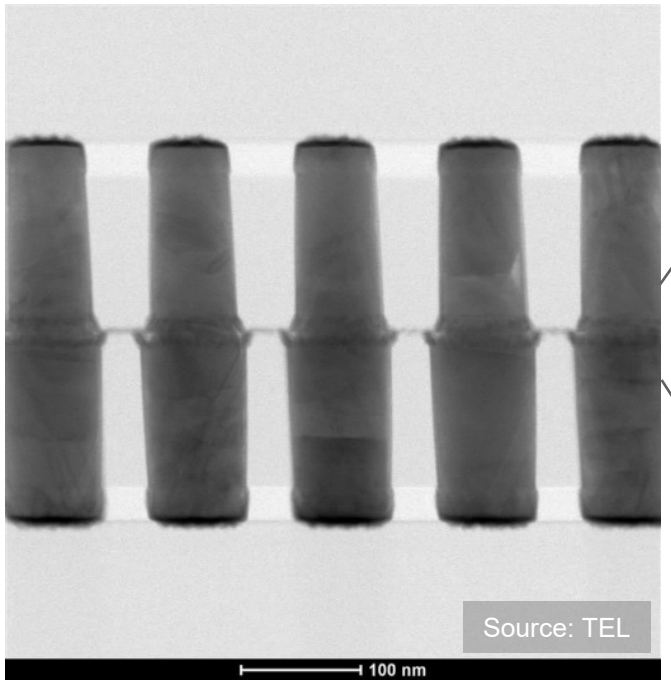
- Residuals are higher than previously reported 500nm pitch hybrid bonding
- Higher misalignment in Y direction attributed to hexagonal bond pad layout

Cross-Sectional TEM of 140nm Pitch Hybrid Bond Interface

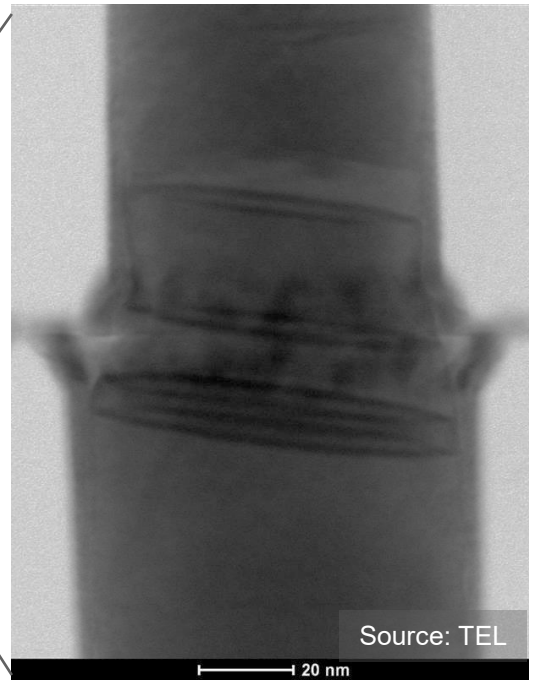
Slightly Misaligned Hybrid Bonding



Well Aligned 140nmP Hybrid Bonding



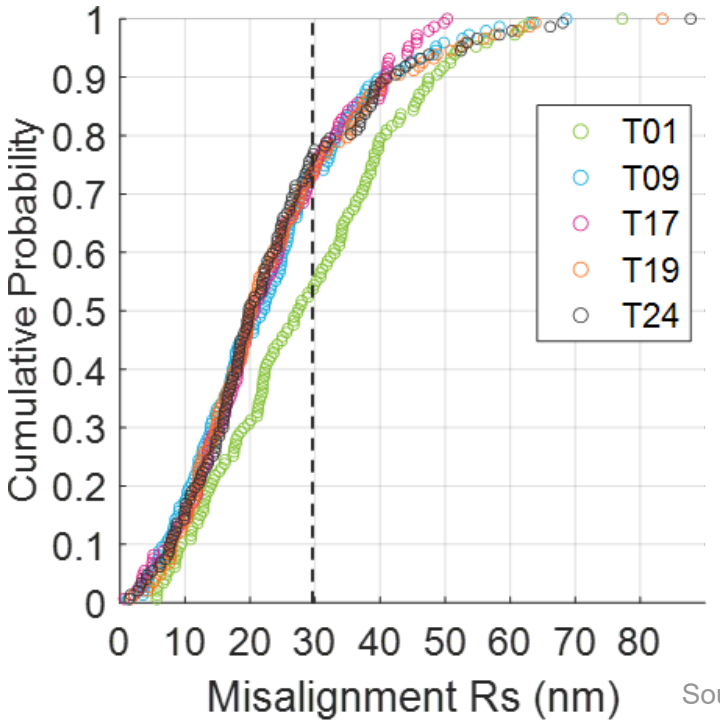
Cu grain growth across interface



Post-anneal TEM shows successful hybrid bonding with Cu grain growth across the bond interface

Optimizing Bond Recipe to Reduce Bonding Residuals

- Bonding residuals for 140nm pitch test vehicle was 80-110nm without optimization
- Bonding recipe recipe from the 500nm bond pitch test vehicle was used as a baseline (T01)
- Optimized bonding recipe had residuals <50nm for champion wafer (T17) with 75% of residuals below 30nm for 4 wafers



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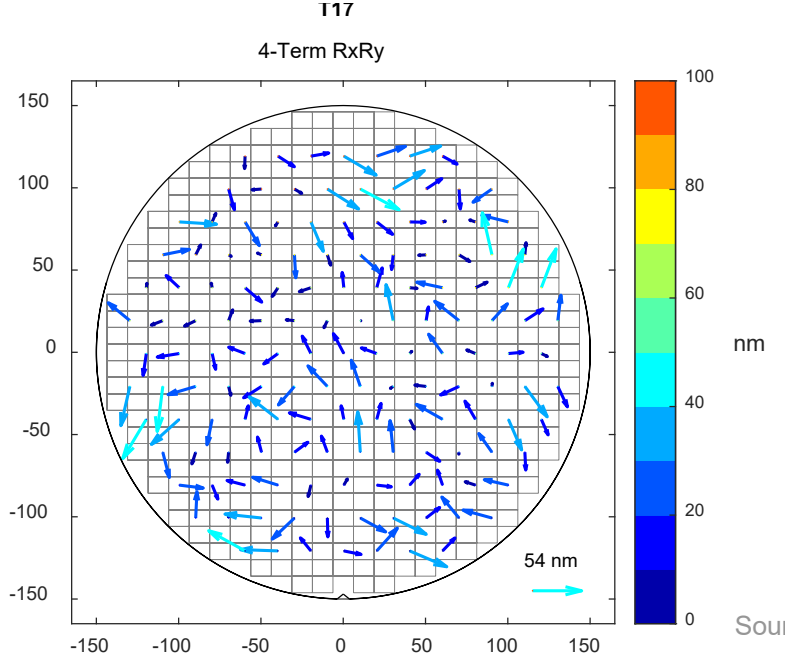
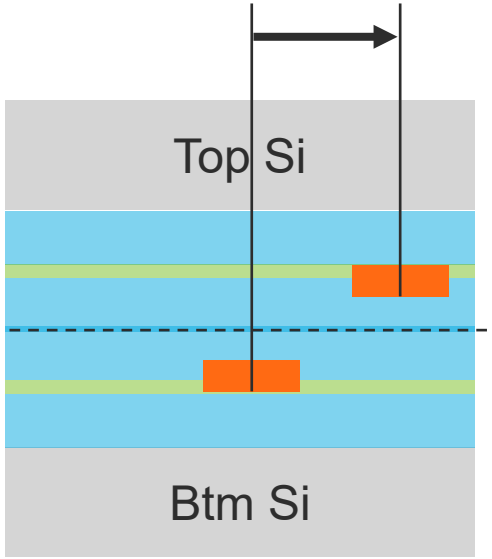


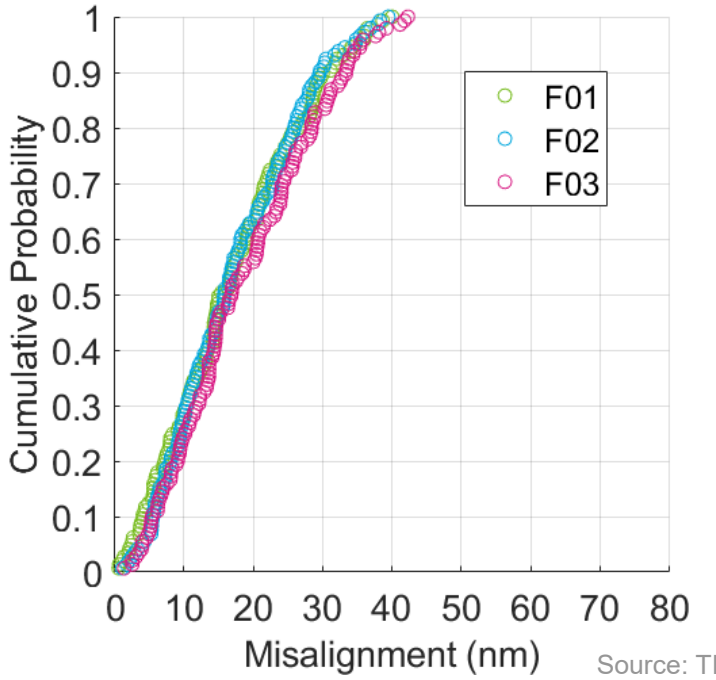
Source: TEL

	Rx	Ry	Rs
Max	41.2nm	49.4nm	50.3nm

Removing Impact of Bond Pad Layout on Misalignment

- Wafers were covered with dielectric and bonded with the optimized bonding recipe to remove effect of the Cu bond pad layout on bonding overlay (aligned fusion bonding)
- Bonding residuals <40nm for 99.5% of points measured, indicating Cu bond pad layout has a significant effect on bonding residuals





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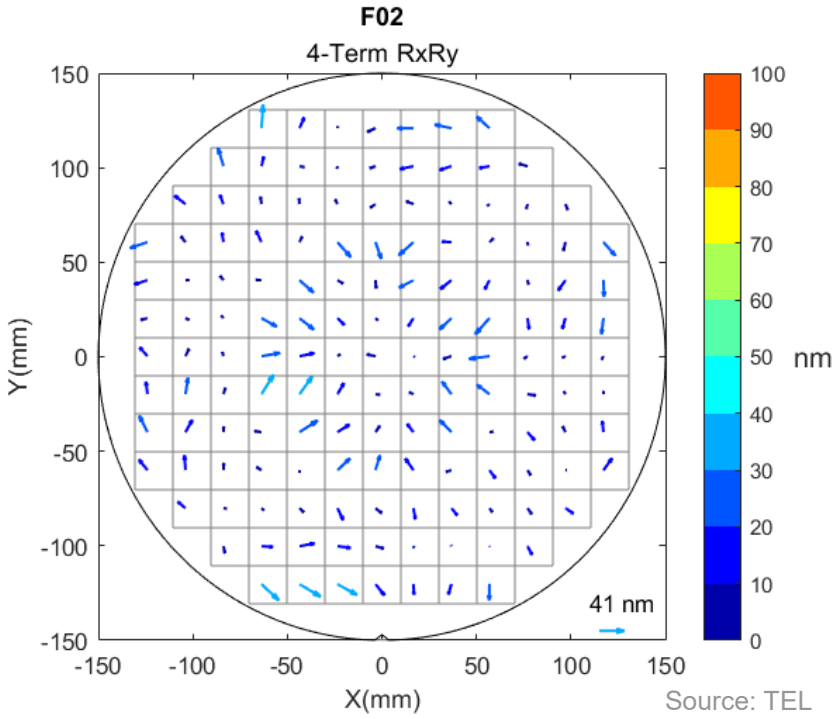

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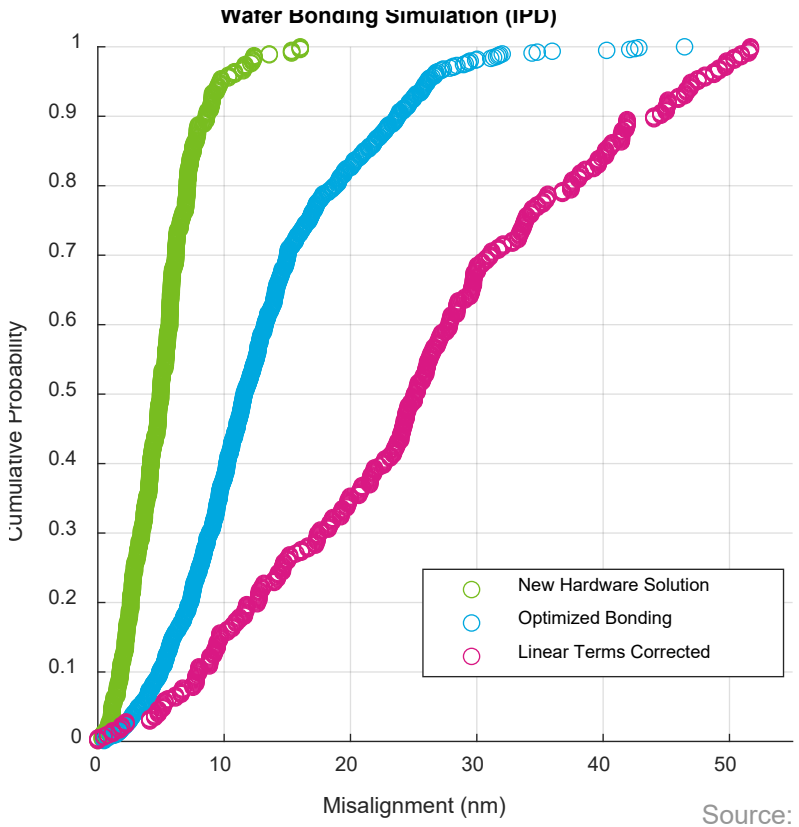
Hardware Solution to Reduce Wafer Bonding Residuals

- New hardware solution designed to reduce residuals from Si substrate shows DxDy <15nm in multi-physics bonding simulation [1]



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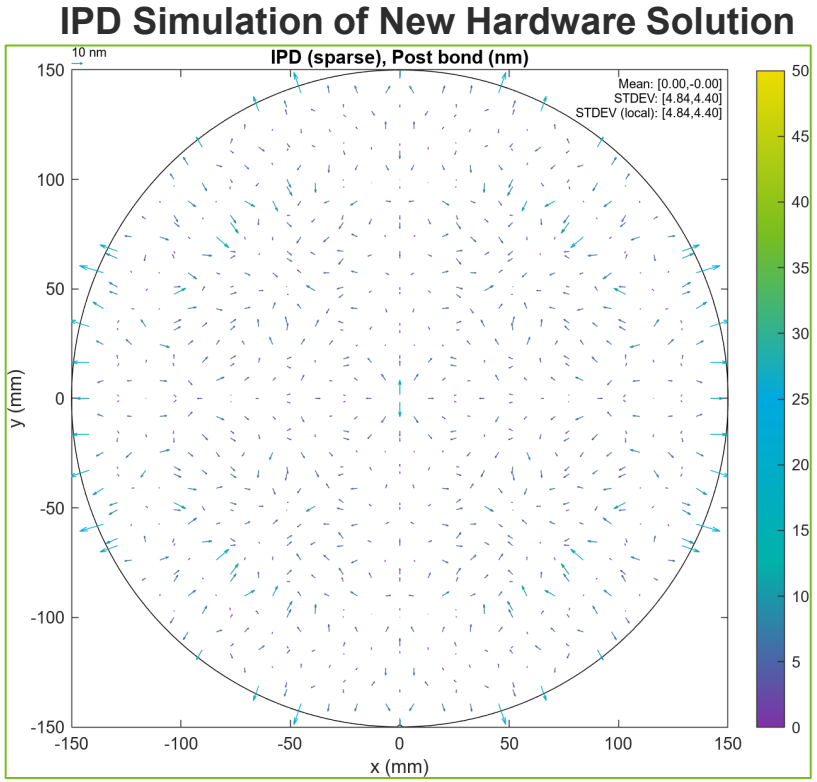

Source: TEL

[1] "Distortion Simulation for Direct Wafer-to-Wafer Bonding Process" N. Ip ECTC 2023

Conclusions and Next Steps

- 140nm pitch bond pad only test vehicle was setup to evaluate bonding
- Void-free bonding with Cu grain growth across the bonding interface was demonstrated at 140nm pitch
- 140nm pitch test vehicle showed bonding residuals <50nm after recipe optimization (same recipe showed <40nm residuals for fusion bonding)
- Multi-physics bonding simulation shows new hardware solution lowers bonding misalignment to 14.6 nm M+3σ

Next Steps

- Multilevel 140nmP test vehicle development for electrical testing across hybrid bonding interface

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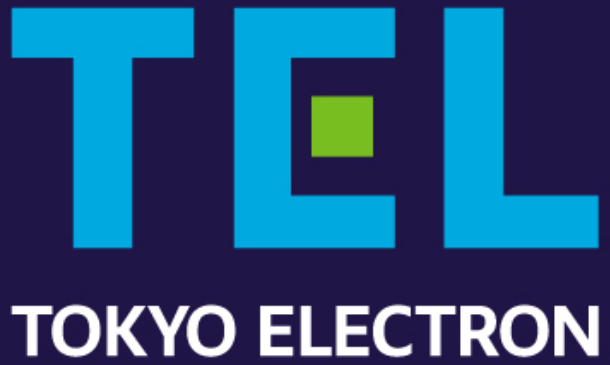
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