TOKYO ELECTRON

Demonstration of <5nm Overlay Distortion for Backside Power Delivery Through Control of Wafer Conditions and Processing

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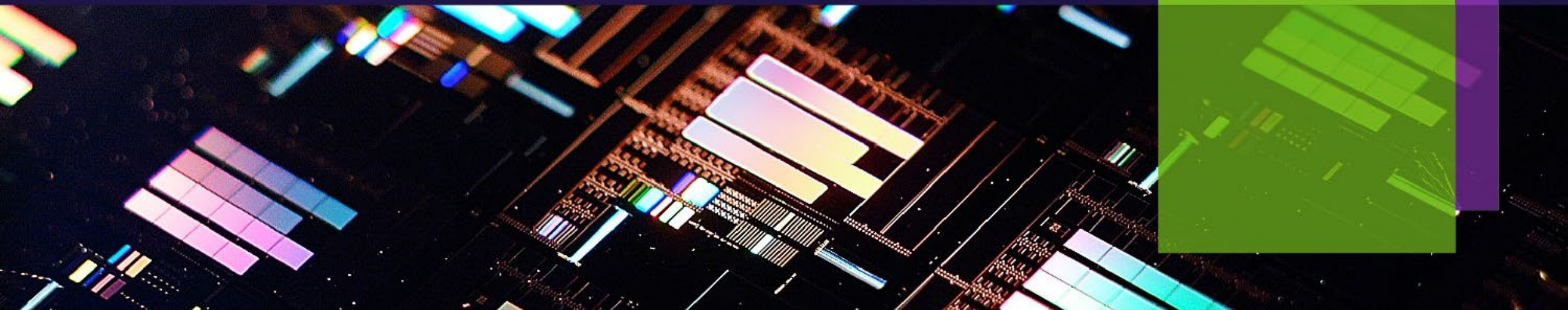


Outline

- 3D Integration Overview
- BSPDN Background
- Distortion Test Vehicle Setup
- IPD Reduction Through Bonding Wave Optimization
- Conclusions and Next Steps

3DI Opportunities Driven by HPC/AI

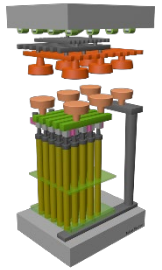
Frontend Processing



BSPDN*1

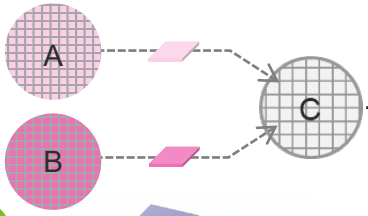


CFET*2



DRAM

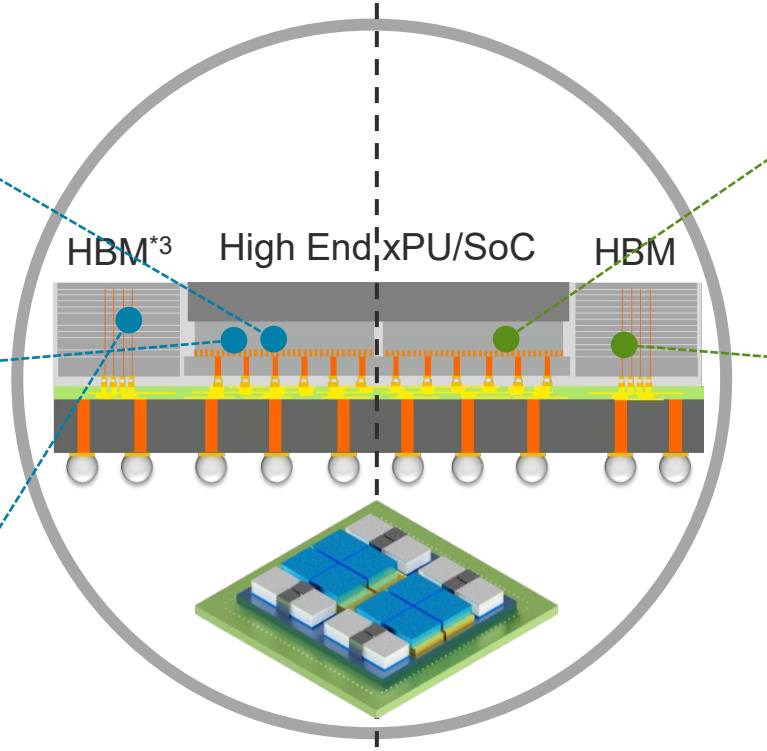
Advanced Packaging



3DIC



Stacked Memory



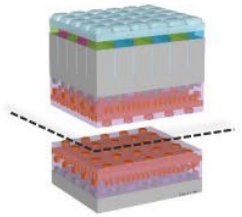
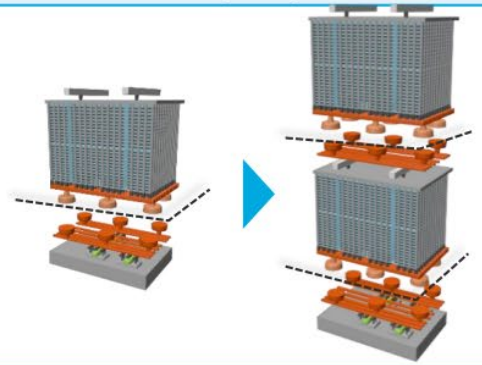
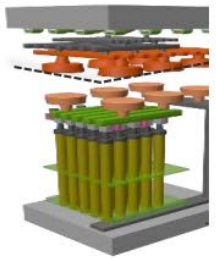
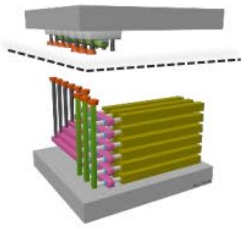
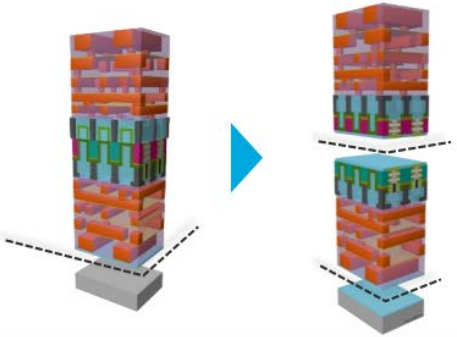
*1 BSPDN: Back Side Power Delivery Network
*2 CFET: Complementary Field Effect Transistor
*3 HBM: High Bandwidth Memory

Wafer Bonding Applications (Advanced Packaging)

Application	Advanced Package	
	Stack Memory / HBM	3DIC
Stacking Device	DRAM Wafer DRAM Wafer + DRAM Wafer + Logic Wafer OR DRAM ( ) Die DRAM ( ) Die + DRAM ( ) Die + Logic Wafer	SoC Disaggregation Device A Wafer + Device AorB Wafer OR A, B, C, Die, Wafer
Bonding	Wafer to Wafer / Die to Wafer (CHB/Fusion)	Wafer to Wafer / Die to Wafer (CHB)
Structure	**Micro Bump** → ***Cu hybrid*** (More stacks) Change • Thinner die / more stacks • High density connection • Better thermal conductance Cu	**Monolithic SoC** → ***3D Stack IC*** SRAM, CPU/GPU, I/O&Peripheral Change • Small formfactor (3D stack vs. 2D) • Higher speed (shorter wiring, no bump) • Lower power (shorter wiring, no bump) • Lower cost (higher yields, easy to mix processes) • Shorter time to market (matured IP block reuse)
Status	R&D	R&D ~ HVM

Source: TEL

Wafer Bonding Applications (Frontend)

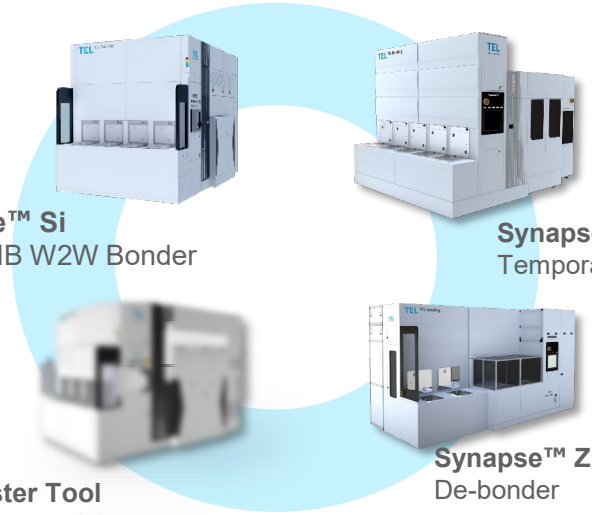
Application	Frontend Process				
	CIS*1	NAND	DRAM		Logic
Stacking Device	BSI*2 Pixel + (Peripheral) + Logic	3D NAND Cell + Peripheral ⋮ + Cell + Cell + Peripheral	VCT*5 DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	3D DRAM (Si Substrate) + Peripheral + Cell + (Si Substrate)	BSPDN Logic + Si Substrate BSPDN & CFET Logic + Logic + Si Substrate
Bonding	Wafer to Wafer (CHB*3/Fusion)	Wafer to Wafer (CHB)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (CHB/Fusion)	Wafer to Wafer (HB*6/Fusion)
Structure					
Status	HVM*4	R&D~HVM R&D	R&D	R&D	R&D~HVM R&D

*1 CIS: CMOS Image Sensor
*2 BSI: Backside Illumination
*3 CHB: Cu Hybrid Bonding
*4 HVM: High Volume Manufacturing
*5 VCT: Vertical Channel Transistor
*6 HB: Hybrid Bonding

Source: TEL

TEL 3DI Product Line-Up

Bonding
(Wafer level / Die level)



Synapse™ Si
Fusion/HB W2W Bonder

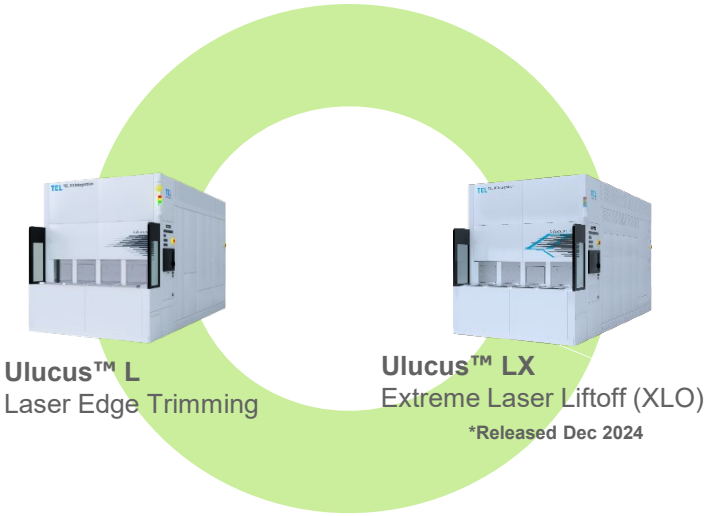
Synapse™ V
Temporary bonder

Synapse™ Z Plus
De-bonder

D2W Cluster Tool
Development activity

- W2W Permanent Bonder
- Temporally Bonder
- De-bonders
- D2W Fusion /Cu Hybrid Bonder

Laser Processing
(Removal Solutions)

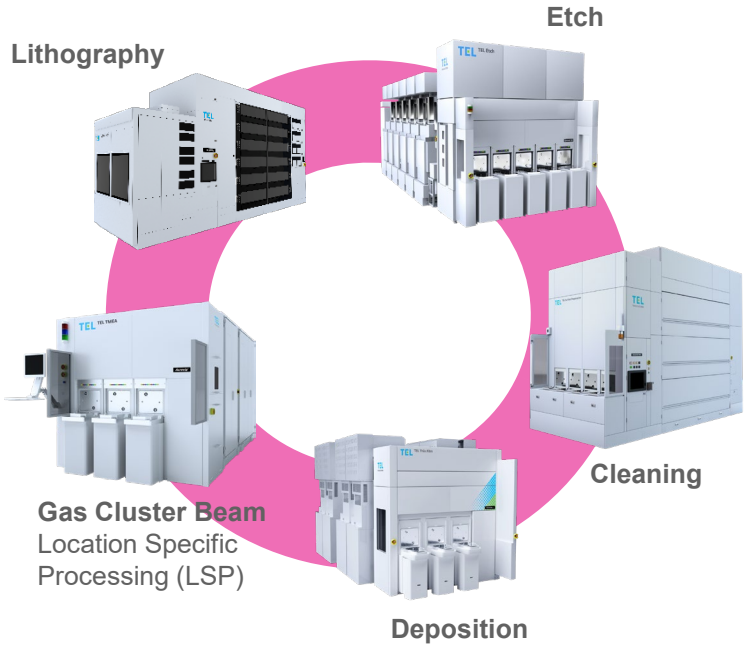


Ulucus™ L
Laser Edge Trimming

Ulucus™ LX
Extreme Laser Liftoff (XLO)
*Released Dec 2024

- Laser Edge Trimming
- Extreme Laser Lift Off

Front End
(Wafer level)

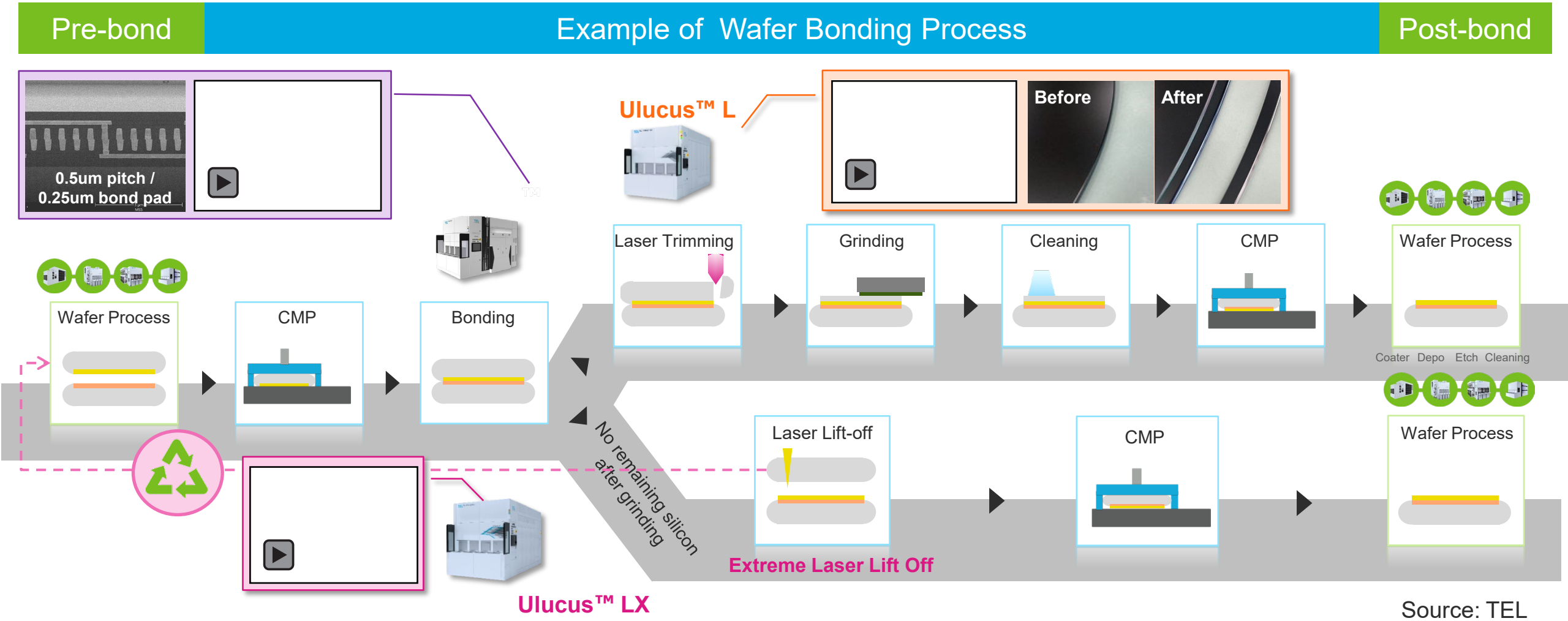


Gas Cluster Beam
Location Specific
Processing (LSP)

- Broad Product Portfolio in front end products
- Leveraging portfolio for integrated learning in 3DI

Source: TEL

TEL 3DI Products for W2W Permanent Bonding Processes

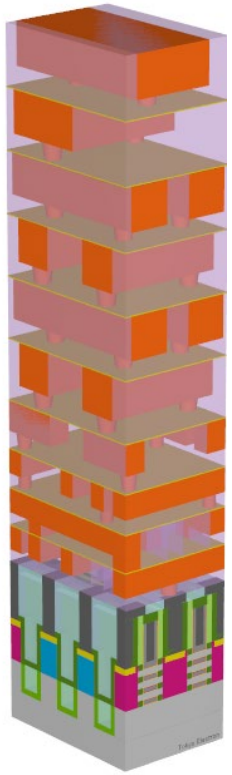


Source: TEL

Enabling next generation wafer bonding processes

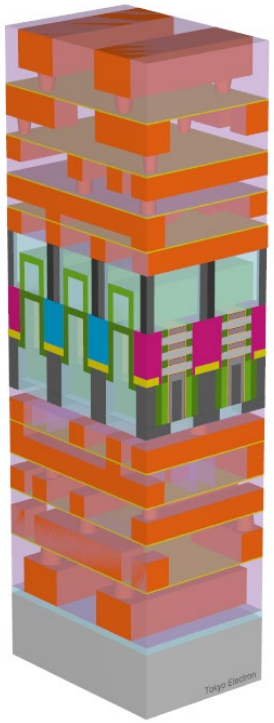
Wafer Bonding Application for Logic Backside PDN: Fusion Bonding

Current structure



Signal & Power

Backside PDN：Power Delivery Network



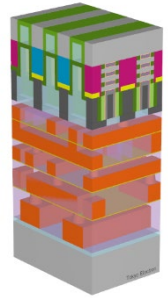
Power

Signal

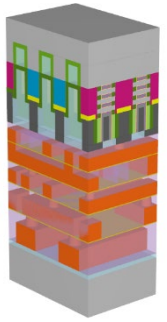
Pursue further scaling without the power wiring bottleneck

Power BEOL (Backside)

Backside thinning

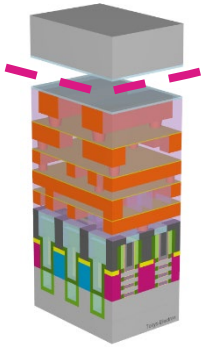


Reverse

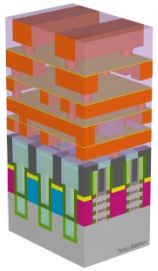


Bulk Si Wafer bonding

Bonding surface



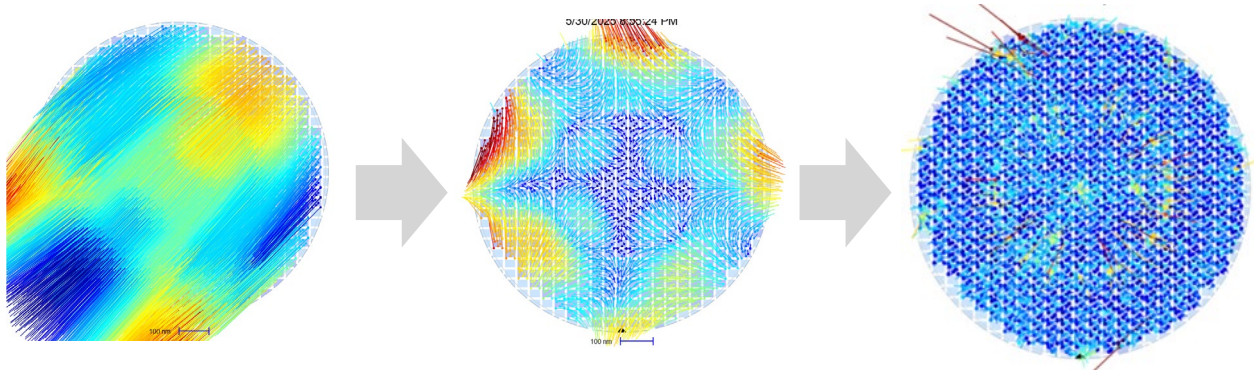
Signal BEOL (Front side)



For BSPDN <4nm Distortion required

Inter-field Correction (W1F1) vs Inter+Intra-field Correction (CPE)

Incoming W1F1 CPE



Source: TEL

CPE6 – Correction Per Exposure (Die Level)

Die Position		Intra-field Parameters					
X	Y	T_X	T_Y	R_s	R_a	S_X	S_Y
x_1	y_1	T_{x1}	…				
x_2	y_2	T_{x2}	…				
…	…	…					
x_N	y_N	T_{xN}	…				

Global Linear Corrections

Input

Transformation

Example → Example

- Can rotate, translate, tilt, and expand the **entire word/wafer**

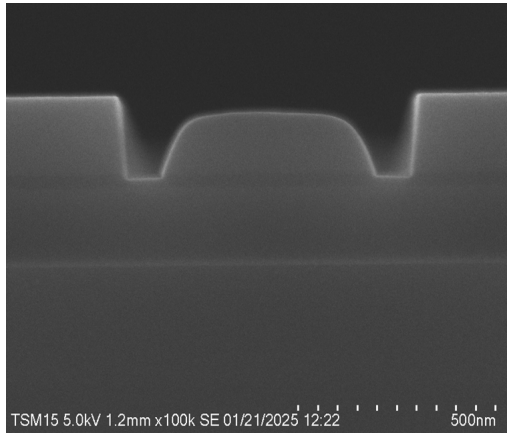
Correction per exposure

Example → Example

- Can rotate, translate, tilt, expand, and distort **each letter/die**

Etch Process Impact on Backside Alignment

- Under etch of alignment features may not be visible from the top but causes serious issues for backside alignment



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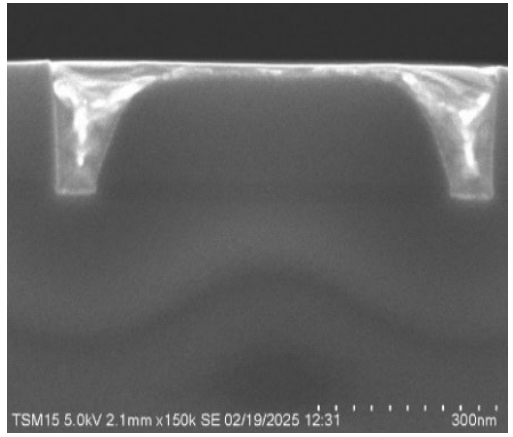

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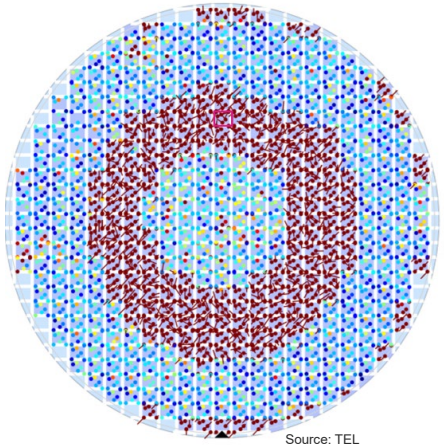
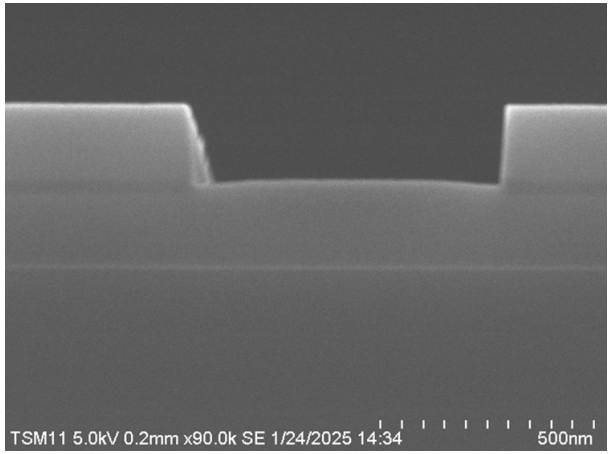

Source: TEL

- By recovering the uniform bottom profile the asymmetry of across the wafer was reduced from >200nm to <3nm.



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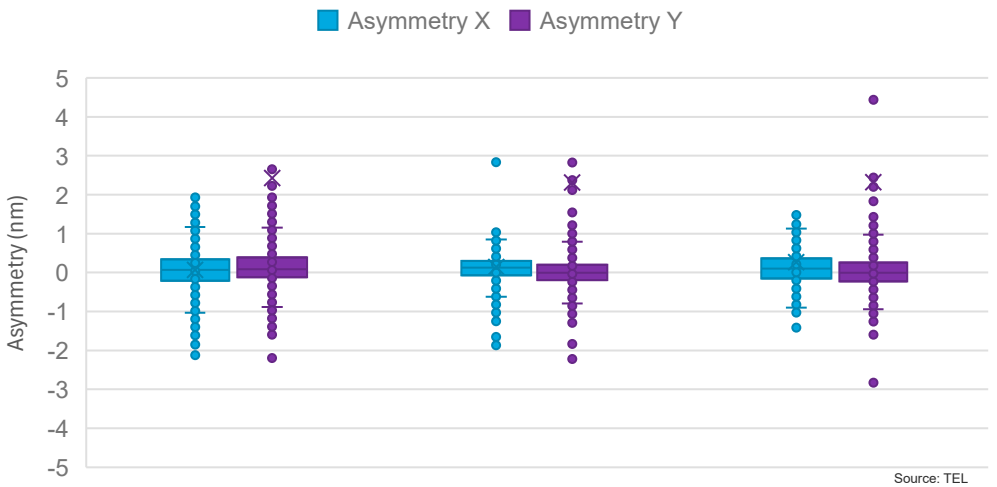


Source: TEL

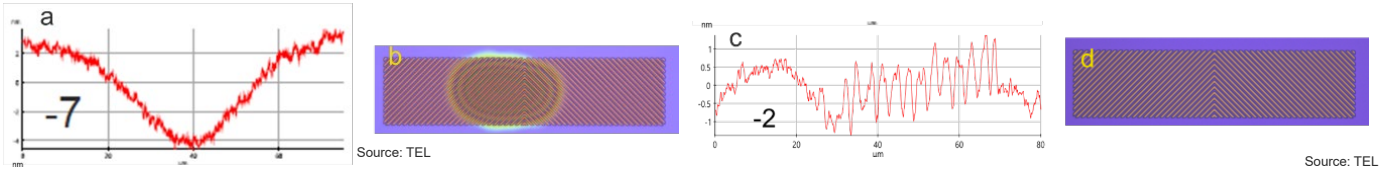
Surface Preparation to Enable High Quality Overlay Post-Bonding

- CSAM shows Void-free bonding, but voids smaller than the pixel size of the scan may still be present

- Small rolloff along alignment marks can create voids at the bonding interface causing alignment failure

Without planarization

With planarization



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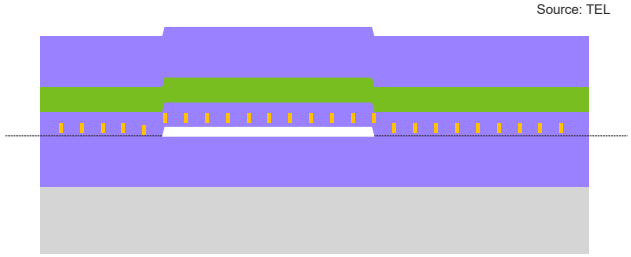

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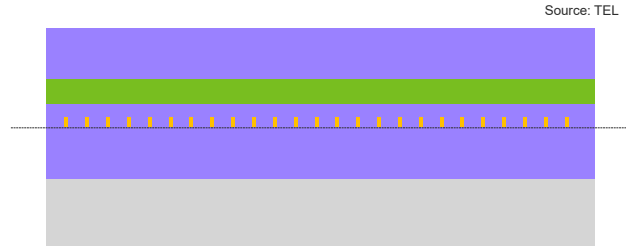

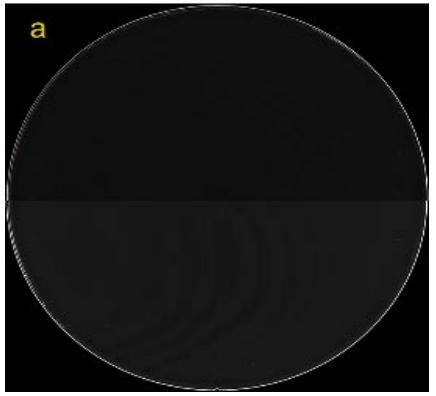

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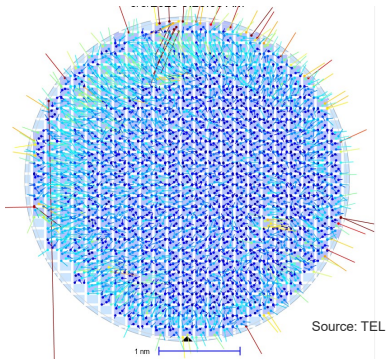


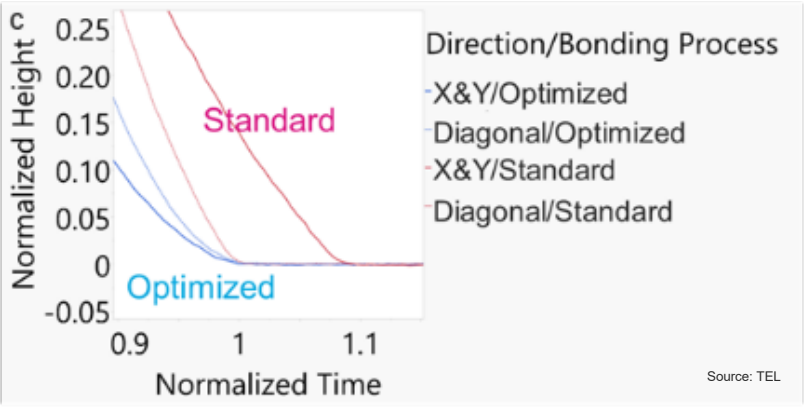
Source: TEL

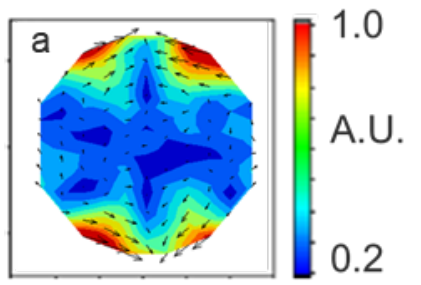
- Yield: 4143/4192= ~99%
- Asymmetry: <2nm M+3σ

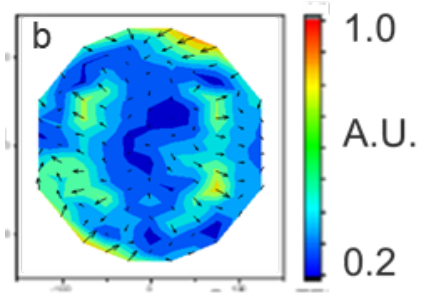
Topography Impact on Propagation Uniformity and Distortion

- Topography on the bonding layer can cause nonuniformity in the bonding propagation rate across the wafer

- Planarization of the underlying features eliminates the difference in propagation rates along different directions and greatly reduces the resulting distortion



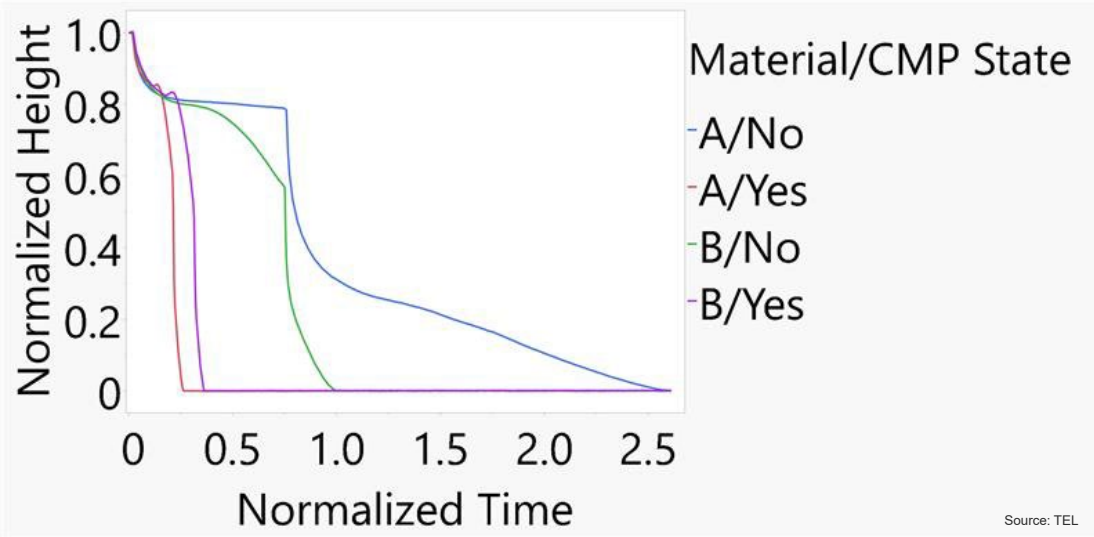


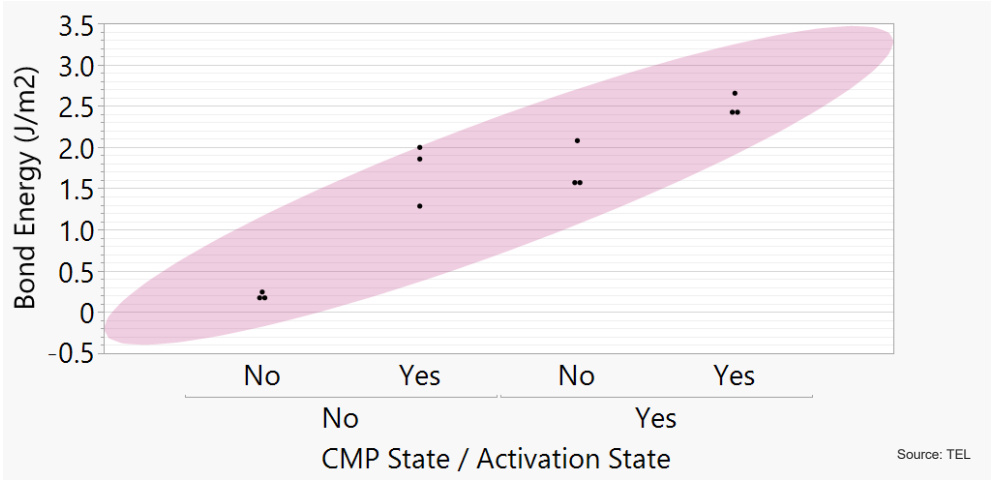


Source: TEL

Impact of Bonding Material and Material Preparation on Propagation

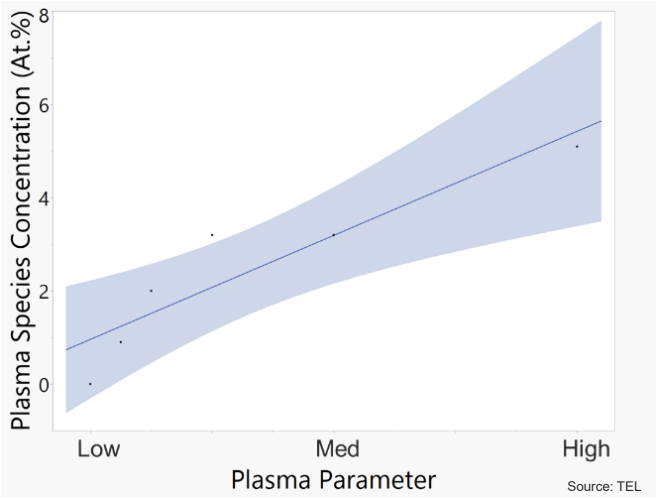
- Lower propagation speed leads to less distortion but lower bonding strength.
- While there can be a wide range of propagation speeds among different materials, after CMP there is little difference between them
- CMP and Plasma activation both create surface active sites to improve the strength of a bond

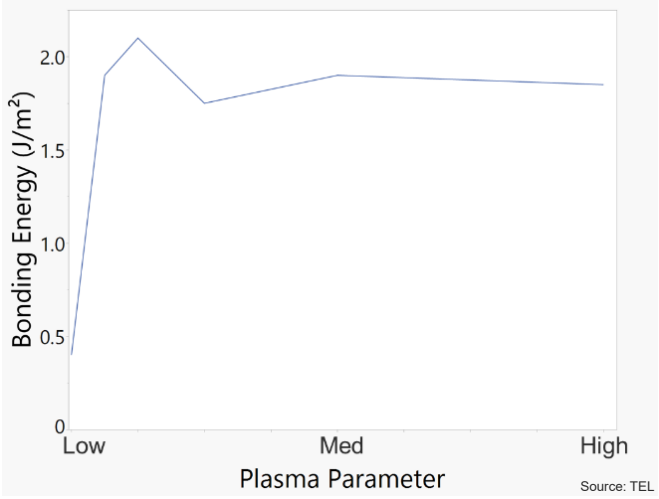


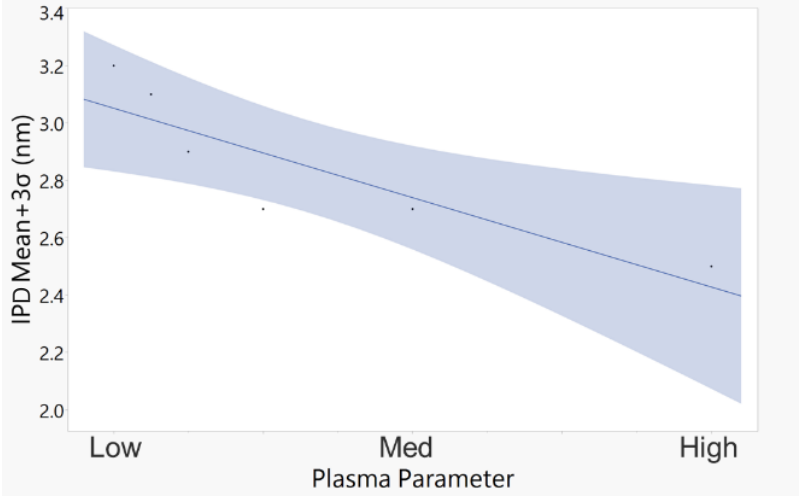


Impact of Plasma Activation on Bonding Quality and Propagation

- Adhesion (hydrogen bonding) controls propagation speed but post-anneal strength is due to covalent bonds
- Introducing passivating species during activation can reduce adhesion without impacting bond strength
- Optimization of plasma parameters can enable decoupling of the propagation speed from the bonding strength



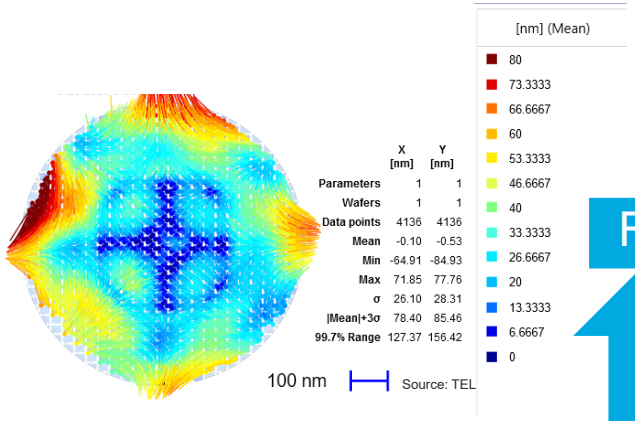




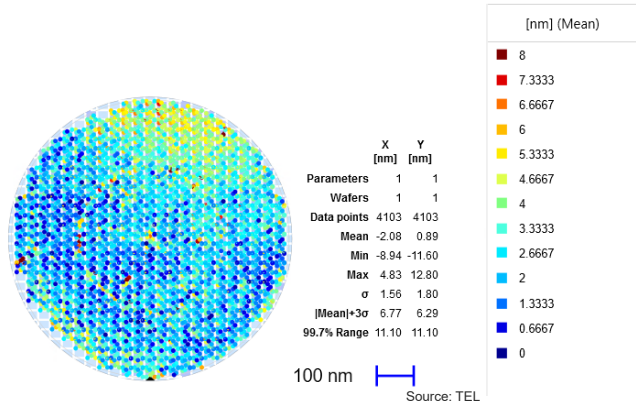
Integration Improvements on BSPDN Overlay

Post-Bond Litho Overlay *(1st Exposure)*

M3S X/Y: 78.4/85.5 nm



Rework w/ CPE6



Post-Bond Litho Overlay *(2nd Exposure)*

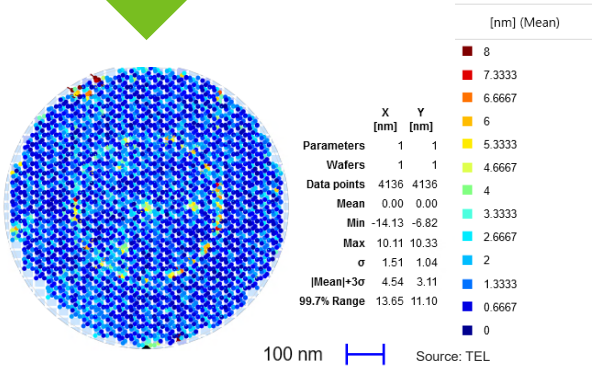
M3S X/Y: 6.77/6.29 nm

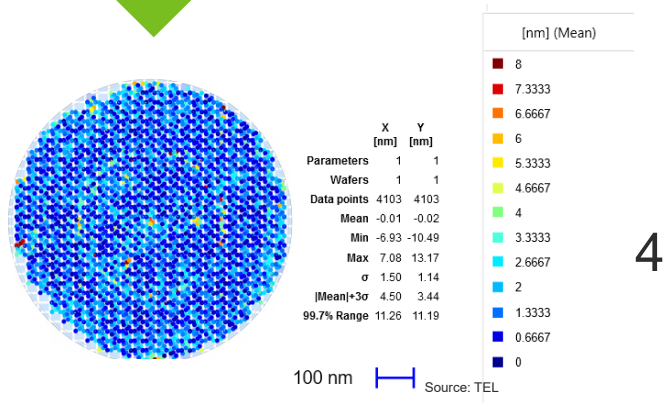
CPE6 Simulation

Feedback

W1F1 Simulation

M3S X/Y: 4.54 /3.11 nm





M3S X/Y: 4.50 /3.44 nm

Conclusions and Next Steps

- BSPDN implementation requires new processing considerations and co-optimization across multiple areas of the integration flow
- Voids smaller than the resolution of CSAM can impact bond and alignment quality of subsequent processes
- Upstream processing and surface preparation play a critical role in controlling the overlay distortion after bonding
- Optimization of the bonding process and integration enables <7nm on-product overlay after CPE6 which is <5nm after linear terms are removed

Next Steps

- Isolation and elimination of bonding signatures from the on-product overlay

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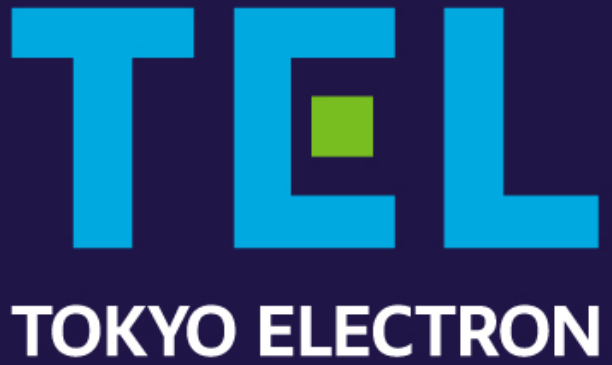
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