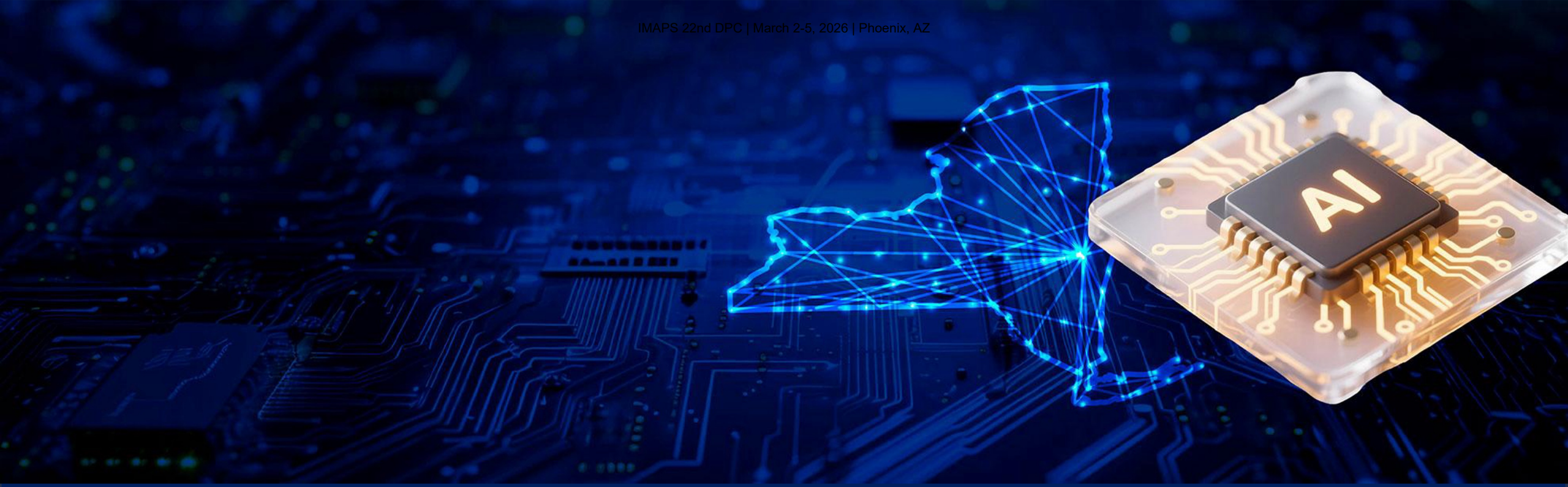


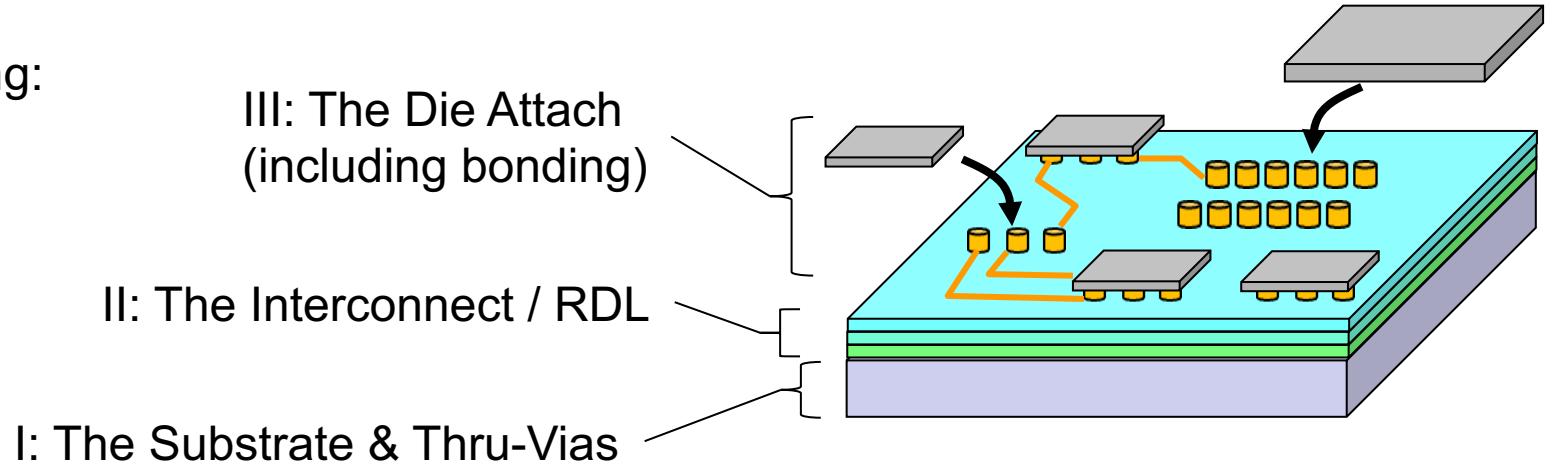
Glass-on-Glass: Unlocking Opportunities for Packaging

Bill Taylor (FuzeHub)
Yunjiang Ding, Lei Li, James Hwang (Cornell University)
5 March, 2026

FUZEHUB

A View of Packaging and an Important Distinction

- Simple view – 3 parts to packaging:



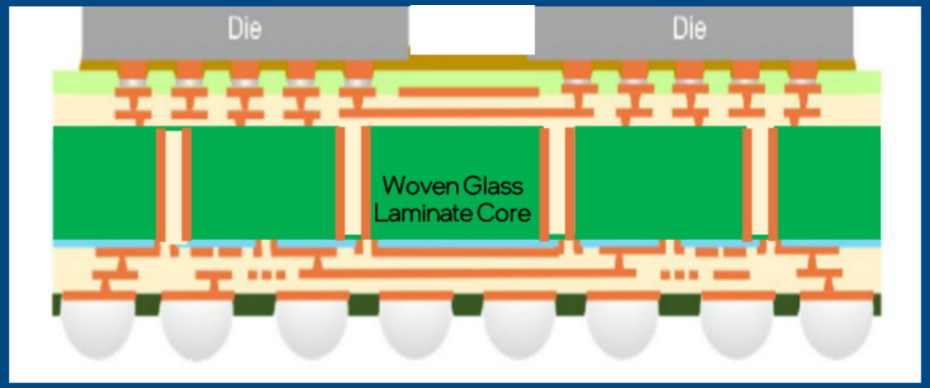
- We <u>do have</u> the flexibility, and we <u>should have</u> the engineering prowess, to assess each component as we work to solve the increasingly difficult challenges being thrown at the packaging world.

- People assume that “Glass Substrates” must also mean we keep using polymer RDL. ➔ NO!

Switching to Glass Substrate, but keeping polymer RDL, limits performance and counteracts glass’ advantages.

Motivation for Glass Core Substrates

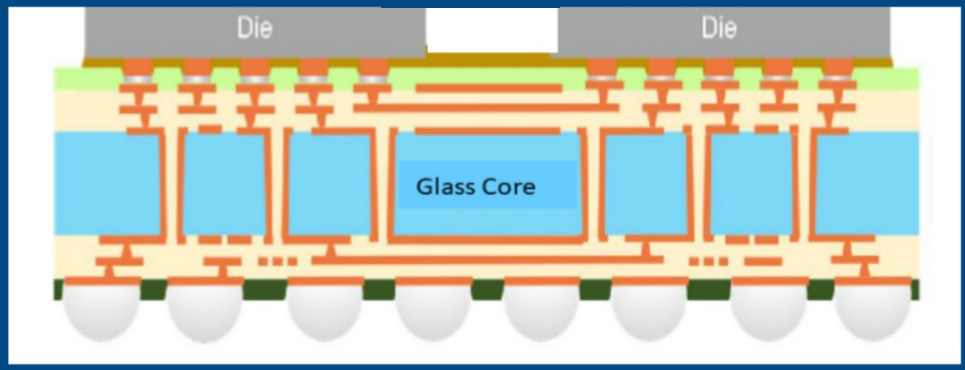
Organic Substrate



Organic substrates leverage traditional PCB-like cores with woven glass laminates

- Provides a low cost, easily manufacturable material set with off the shelf laminates available from leading suppliers

Glass Core Substrate



Glass core substrate enable significant improvement to both electrical and mechanical properties

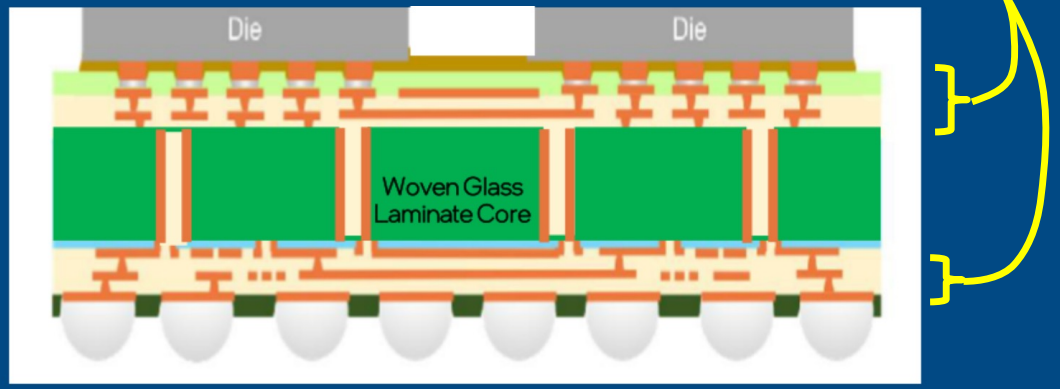
- Tunable Modulus and CTE closer to silicon → Large form factor enabling
- Dimensional stability → Improved feature scaling
- High (~10x) through-hole density → improved routing and signaling
- Low Loss → High speed signaling
- Higher Temperature capability → Advanced Integrated Power Delivery

Glass Core has similar properties as Si → Dimensional stability and ability to scale

*Based on internal analysis of Intel products and projections of future Intel products

Motivation for Glass ~~Core Substrates~~ RDL

Organic ~~Substrate~~ RDL

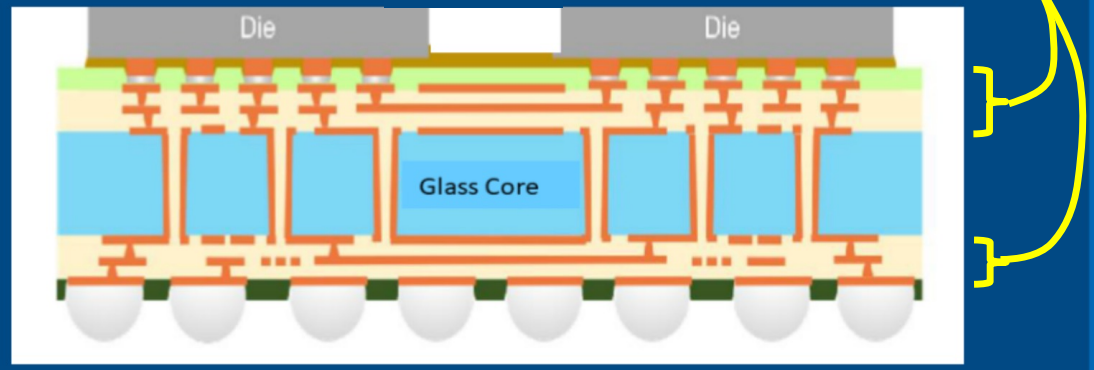


Organic substrates leverage traditional PCB-like cores with woven glass laminates

- Provides a low cost, easily manufacturable material set with off the shelf laminates available from leading suppliers

All of the same arguments apply!

Glass ~~Core Substrate~~ RDL



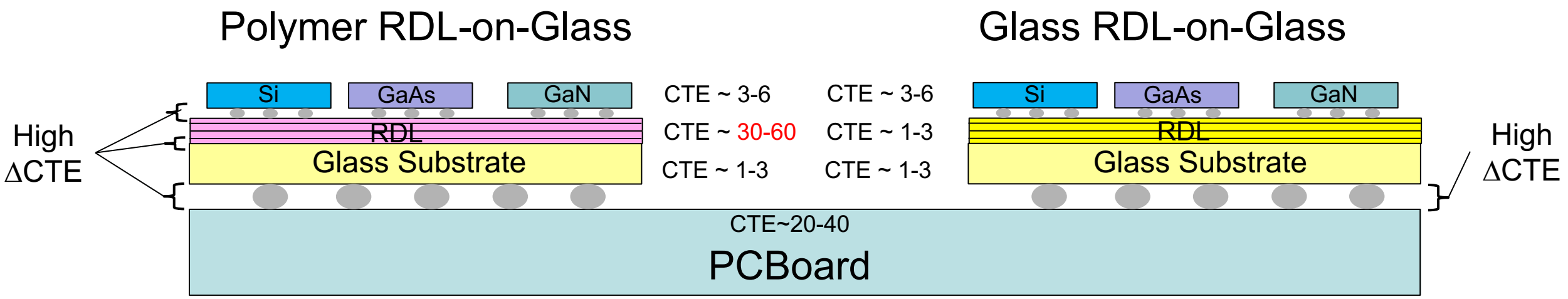
Glass core substrate enable significant improvement to both electrical and mechanical properties

- Tunable Modulus and CTE closer to silicon → Large form factor enabling
- Dimensional stability → Improved feature scaling
- High (~10x) through-hole density → improved routing and signaling
- Low Loss → High speed signaling
- Higher Temperature capability → Advanced Integrated Power Delivery

Glass ~~Core~~ RDL has similar properties as Si → Dimensional stability and ability to scale

*Based on internal analysis of Intel products and projections of future Intel products

Thermal Expansion Mismatch



- Polymer RDL, with its CTE 50x larger than glass, causes problems.
  - Cooling down from processing temp results in built-in stress (warpage)
  - One example of this is “SeWaRe” peeling / cracking, esp. post-dice
    It is still a major problem delaying adoption of glass substrates.

- **Glass (SiO_2) RDL would eliminate SeWaRe. Completely.**

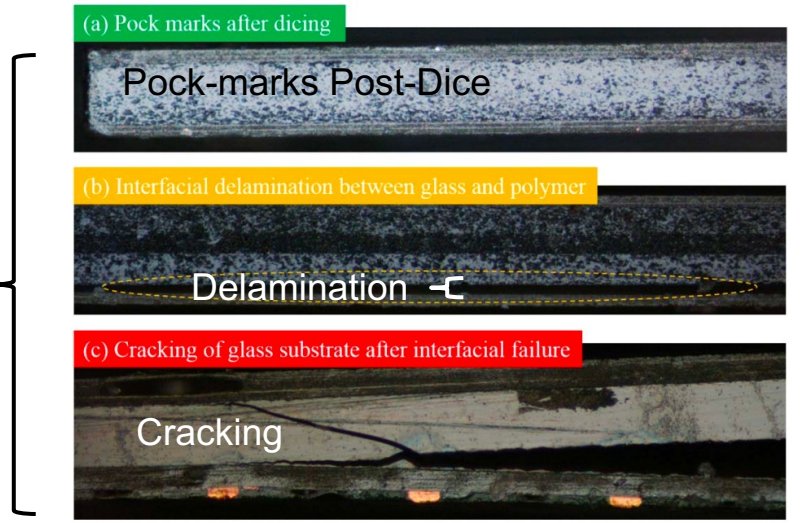
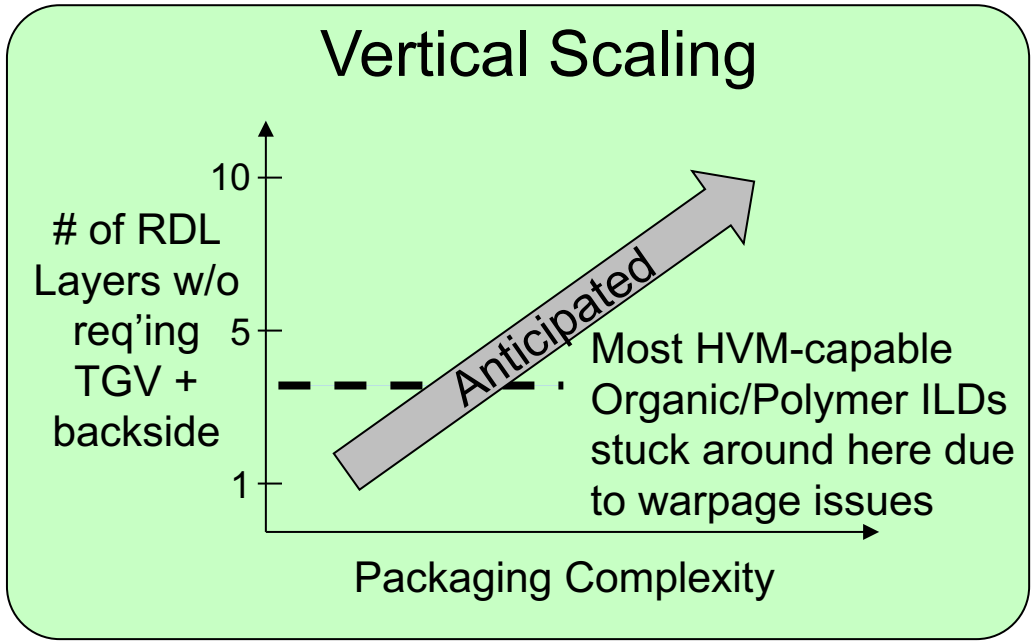


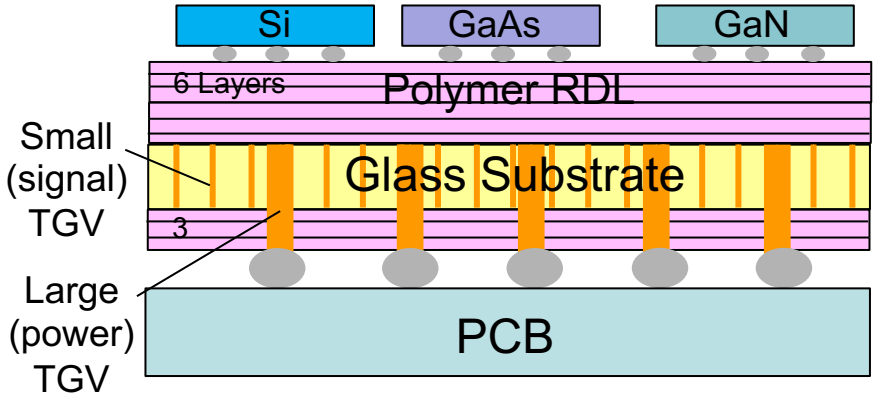
Fig. 2. Optical inspection of glass substrate edge to show failure classification: (a) pock marks after dicing (green), (b) interfacial delamination between glass and polymer (orange), and (c) cracking of glass substrate after interfacial failure (red).

McCann et al., “Prevention of Cracking from RDL Stress and Dicing Effects in Glass Substrates”, *IEEE Trans.Devoce and Mat’ls Rel. (2016) 16 pp 43-49*

*In this work, “Polymer RDL” implies Cu lines in a polymer dielectric using an additive process, and “Glass RDL” implies a Cu lines in SiO_2 dielectric, using a damascene process.

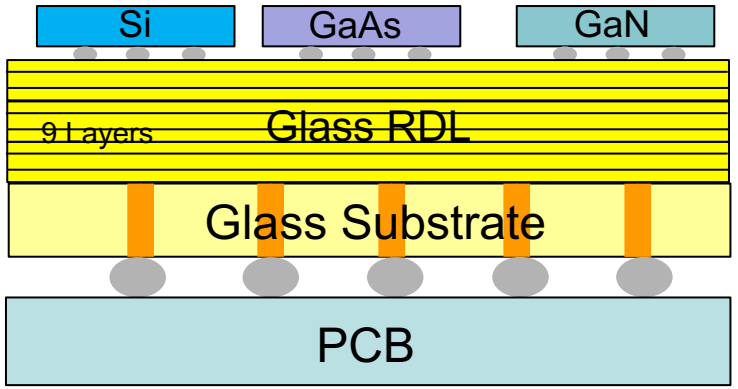
Vertical Scaling





Polymer RDLs Top and Bottom

Balance stress by 6/3 top/bottom
Requires both small (signal) TGVs and large (power/IO) TGVs.
Reliability drops:
=> Many more TGVs
=> Small diam = higher stress
$\sigma \sim \Delta CTE * \Delta T * 1/r$

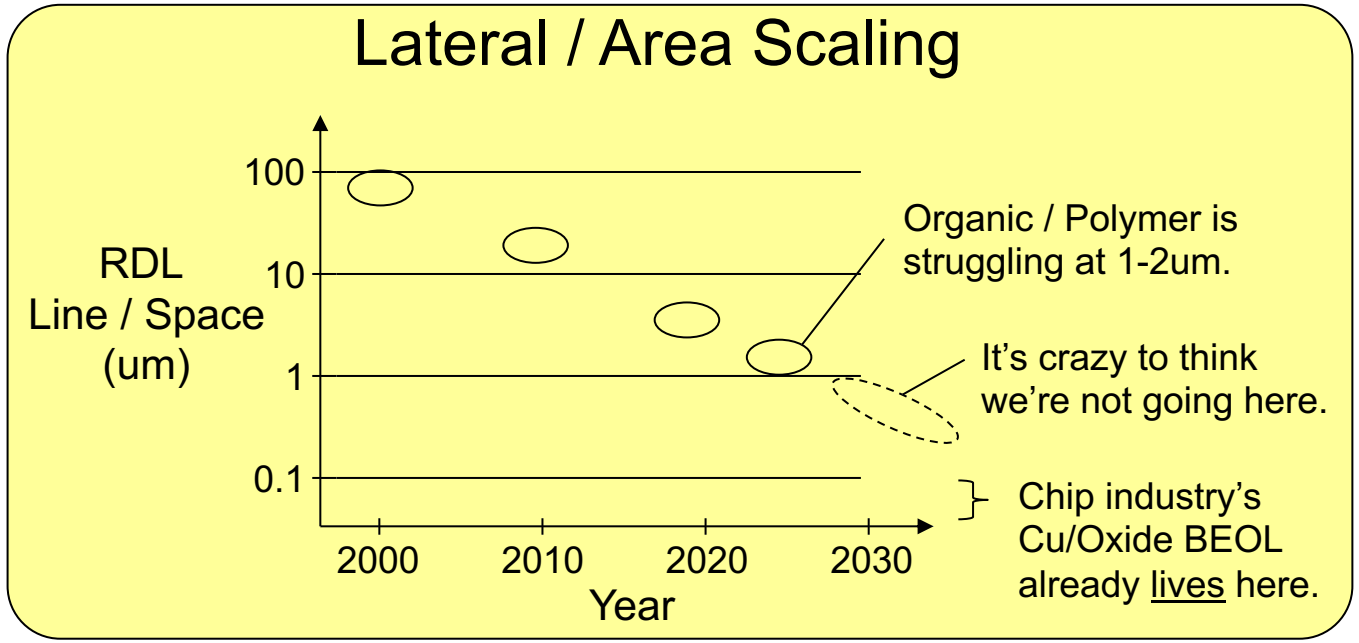


Glass RDLs Top Only

All 9 layers of RDL on top side.
No small (signal) TGVs !
Reliability improves:
=> Only Power/IO TGVs required
=> Many fewer TGVs
=> Large diam = lower stress
$MTTF \sim r^2$

- Stresses in polymer RDLs limit you to maximum 3-4 layers before warpage is too much.
- Current POR: Put 3-4 layers on backside / balance the stress. ➔ Mandates signal vias thru substrate.
  - Not all TGVs are equal. Power/IO TGVs ~80um diameter. Signal TGVs ~30um diameter and very dense.
  - Small diameter = higher stress ($\sigma \sim \Delta CTE * \Delta T * 1/r$), and lower reliability ($MTTF \sim r^2$).
- Avoid that altogether – use Glass RDLs. All RDL can be on top side of wafer. Design is much simpler.
  - Chip fabs do 10 layers of dual damascene "Glass RDL" (Cu/SiO2 BEOL) every day, with no significant warpage.
  - Fine-pitch TGV becomes an option for the designer, not a necessity.

Lateral Scaling

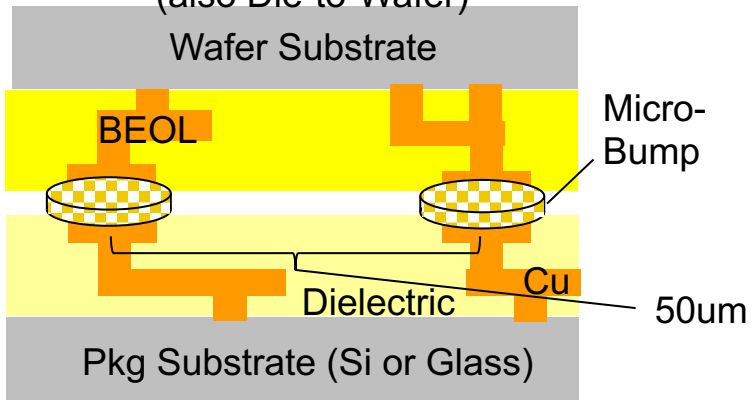


- RDL Linewidth scaling is undeniable. With pressure increasing on packaging it will not stop.
- Advances in polymers, to enable better L/S and Line-Edge-Roughness will continue, BUT…
  - Will it be possible to make those changes, while maintaining/improving tan-δ, moisture, hybrid-bonding, … ?
- In contrast, Cu/SiO2 BEOL is already capable of 10x smaller dim's, with all of the other good properties.

Scaling Demands = Bonding Demands: The Advantage of Glass ILD

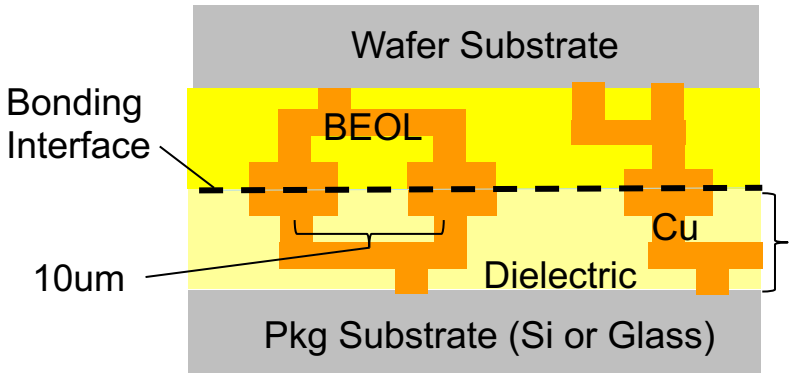
MicroBumps

Wafer-to-Wafer
(also Die-to-Wafer)

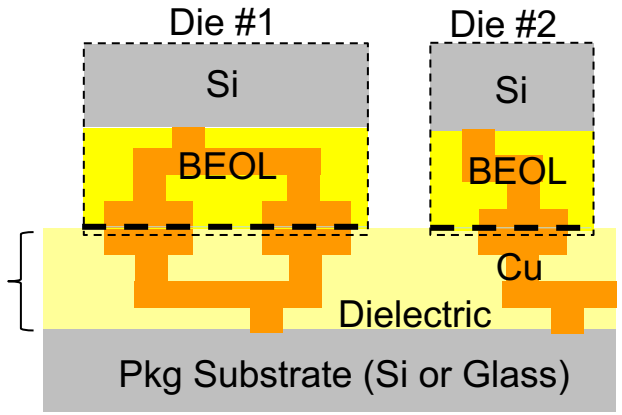


Hybrid* Bonding

Wafer-To-Wafer



Die-To-Wafer

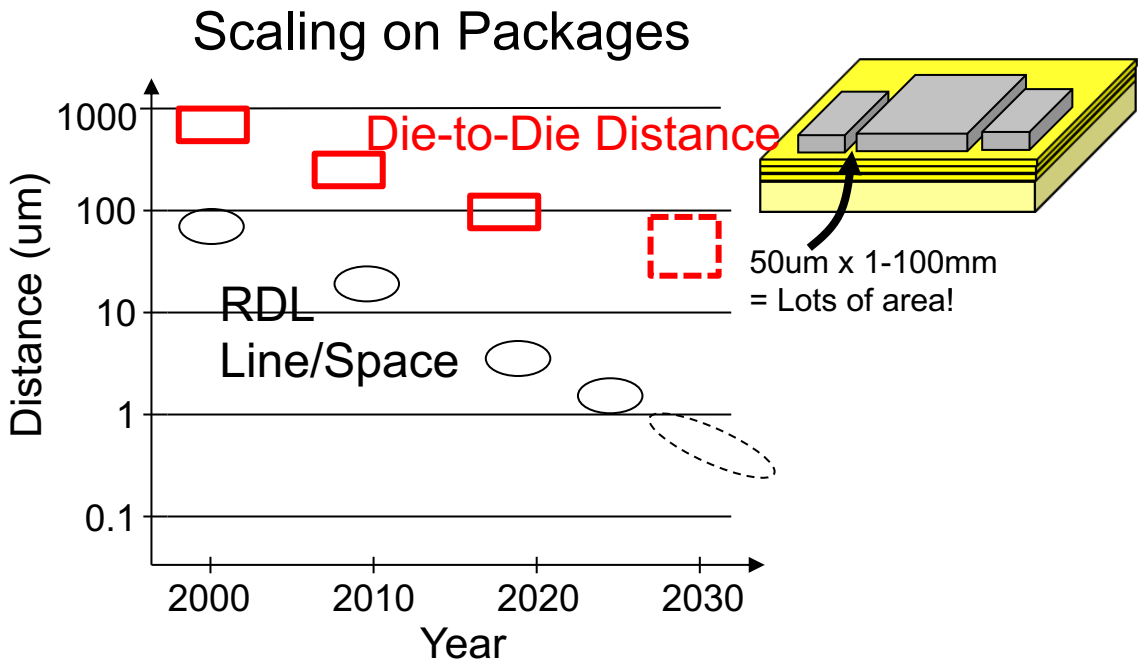


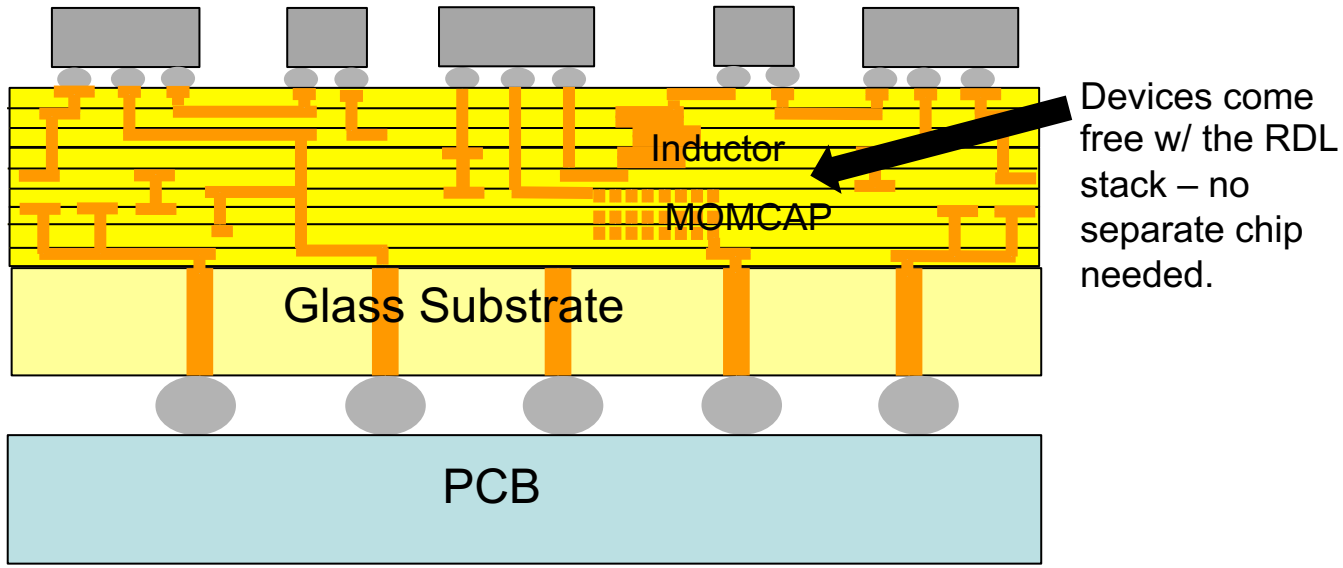
- When attaching Die-to-Wafer or Wafer-to-Wafer, desire fine-pitch connections
  - MicroBumps = 30-50um pitch
  - Hybrid Bonding = <10um pitch ✓
- If the ILD is organic/polymer, hybrid bond is very difficult.
  - Stiffness / Deformation req'ts to enable bonding will limit options for hitting other req'ts (CTE, loss, etc.)
- Hybrid bonding of Cu/Ox is SOTA, years ahead of polymer.

	MicroBump	HybridBond
Polymer ILD	Yes	No
Glass ILD	Yes	Yes

*Hybrid Bonding = both Cu and Ox are present on the bonding surfaces. Cu-Cu bonds and Ox-Ox bonds are formed.

SiO2 RDL Accelerates The Introduction Of Devices Inside The RDL





- As packaging accepts more responsibility, every region will be used – including the space between the die.
- Large area, low resolution devices (inductors/caps) are too expensive for a 3nm chip: use a separate chip, or RDL.
- Cu/SiO2 devices already exist in foundry PDKs, as Cu/SiO2 BEOL structures. With reliability already proven.
  - ➔ Copy/Paste into a Glass RDL package.
- Developing these devices in polymer is not desirable: It costs $, takes time, and will be an inferior device.

… but Organic/Polymer ILDs have Lower Dielectric Constant!

- Agreed. SiO_2~3.9 F-SiO_2~3.4 SiCOH~3.2 Polymers~3.3 to 2.7 — Nice!!
- But, there are more things involved than just ε.
  - Loss Tangent
  - Processing: Substrate warpage, line-edge-roughness
  - In-the-field thermal expansion match to other materials
  - In-the-field maximum temperature and mechanical shock tolerance (military)
  - Moisture absorption
  - Adhesion, including wafer bonding
  - Materials reliability knowledge
  - Past experience helps Time-to-Market – can I piggy-back off of current CMOS knowledge?

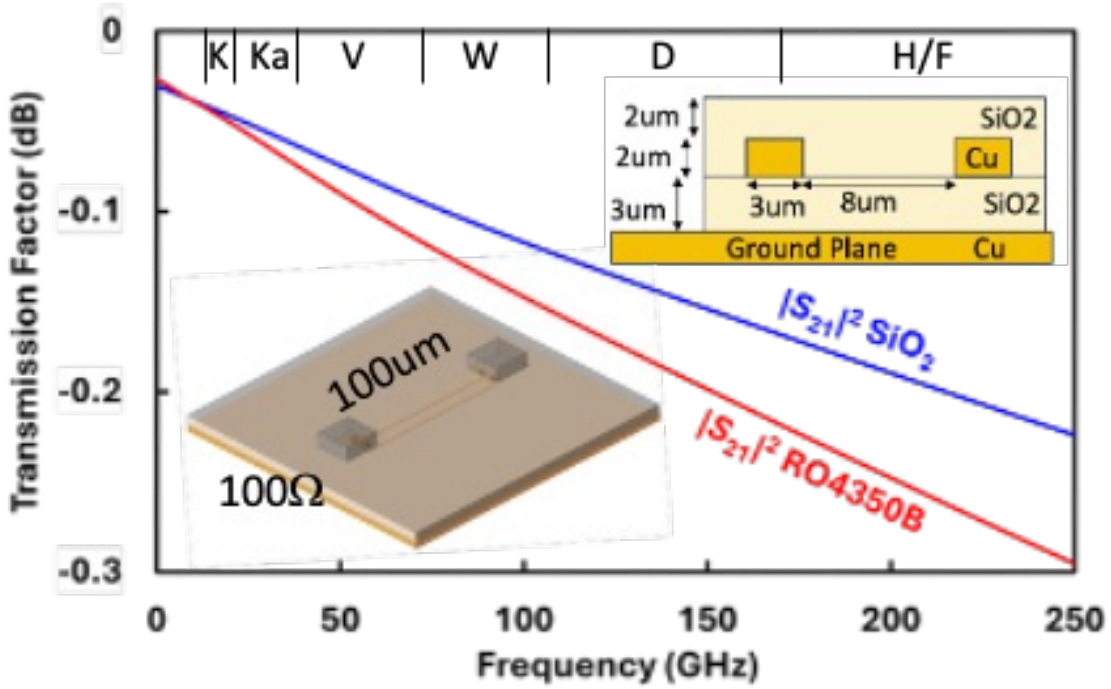
Example: I'd like an inductor in my RDL.
Glass ILD wins on Q and Parasitics (tan-δ), density (#RDL layers), thermal/mech stability, known reliability, and years of existing designs in CMOS BEOL, which can be copied to the RDL.

Example: I want to run a photonics signal from one chip to another.
Glass ILD/SiN WG wins on Δn, loss, stability wrt Temp & Moisture, plus years of experience / reliability testing of that same Glass/SiN structure on SiPh chips.

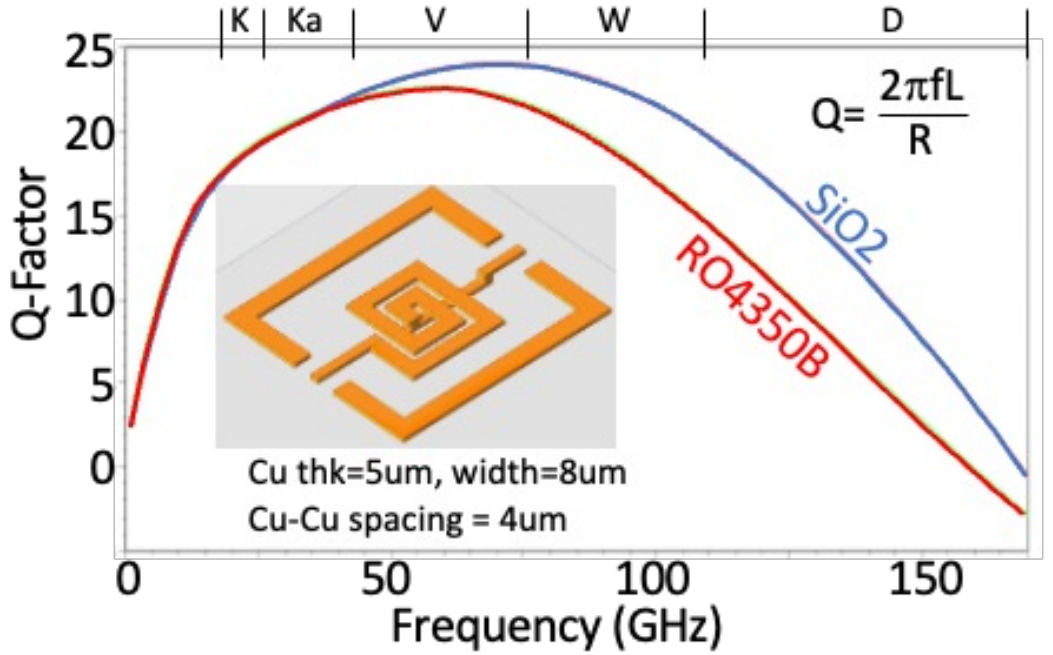
Example: My RF transmitters are optimized as separate chips from my power amp. Run the signal from PA to TX.
Glass ILD wins on IL (tan-δ), attenuation (skin-effect/LER), stable ε wrt Temp & Moisture.

SiO2 RDL Enables Better Devices

Transmission Line



Spiral Inductor



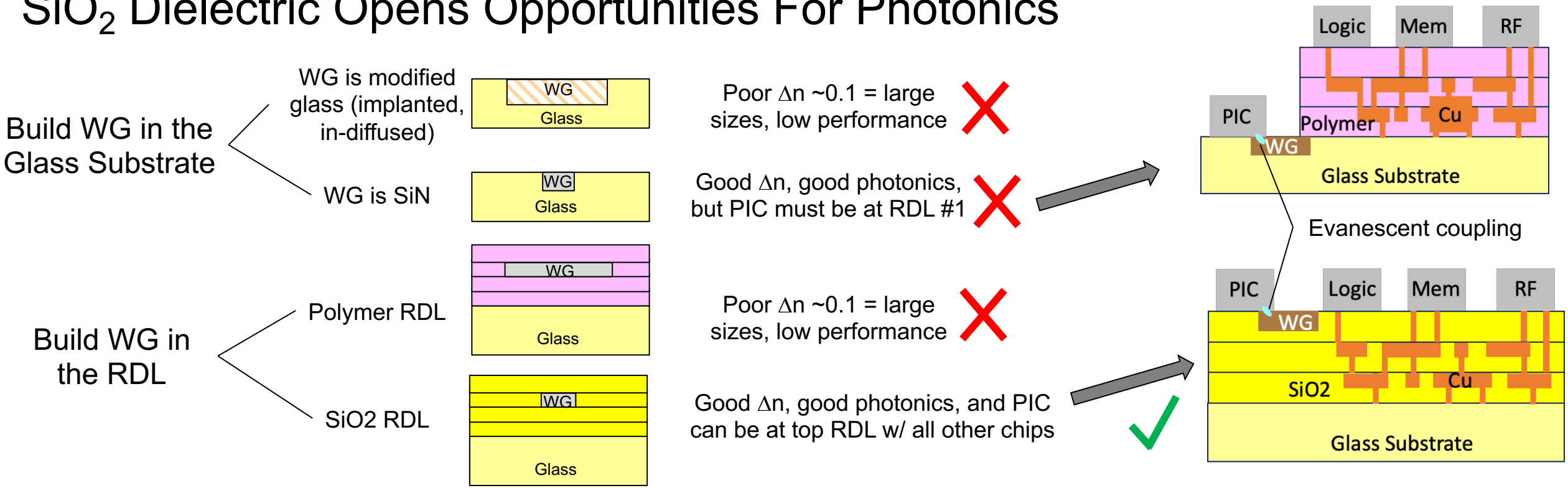
- Using SiO2 as the RDL dielectric allows improved device performance, especially for high-freq applications.

  ➔ Innate material properties of glass

- And further … Glass' superiority becomes even more clear when looking at typical reliability extremes – inorganics naturally shift less than organics.

Property	SiO2	Polyimide (PI)	Benzocyclobutene (BCB)	Polybenzoxazole (PBO)
Dielect Const ε (1GHz)	3.9-4.2	3.1-3.5	2.6-2.7	2.9-3.2
Loss Factor tan-δ (1GHz)	0.0002-0.001	0.002-0.008	0.0008-0.002	0.002-0.006
Thermal Stability	1000C	350-400C	350-400C	350-400C
CTE (ppm/C)	0.5-1.0	30-60	40-50	50-60
Young's Modulus (GPa)	70-80	2-5	2.9-3.2	2-3
Moisture Absorption (%wt)	<0.1	1-3	0.1-0.3	0.2-0.5
Breakdown Voltage (MV/cm)	8-10	3-5	4-5	4-5
Thermal Conductivity (W/m-K)	1.0-1.4	0.1-0.2	0.2-0.3	0.2-0.3
Processability	PECVD <400C	Spin-Coat	Spin-Coat	Spin-Coat
Adhesion to Metal	Good	Excellent	Excellent	Excellent

SiO_2 Dielectric Opens Opportunities For Photonics



- Co-Packaged Optics requires off-chip photonics (waveguides). How best to do this?
- The Die-to-RDL transition causes loss. Waveguide size differences exacerbate this.
  - Waveguide dim's dominated by $RI_{core}/RI_{cladding}$. Higher ratio = smaller dim's, tighter turns.
  - Waveguide on PIC = SiN Core /SiO2 Clad (1.9/1.45) gives ~500nm wide x 300nm high.
  - Waveguide in RDL = Polymer/Polymer (1.6/1.5) gives ~5000nm wide x 3000nm high.

  } 10x size difference! = Loss!
- An SiO_2 RDL enables SiN/SiO_2 Waveguide - the same process used in chip fabs!
  … So, same materials & dim's as the die photonics = Less Loss
  AND, it allows PIC to be at top level of RDL! Huge simplification in packaging.

Reliability

- Extremely important, and can be time-consuming. Best to plan for it now.
  - Temperature min & max
  - Thermal shock (up/down)
  - Mechanical shock
  - Signal (electrical or photonic) stressing
- Every time a material is changed, reliability must be checked (= time & money).
- The Cu/Ox system has been in the chip industry for decades. Materials and structures are well-understood. This should lead to shorter learning curves for package reliability.
- Compare this to Organic / Polymer ILDs. Yes, they are tunable for different characteristics, but reliability must be checked for each of these.

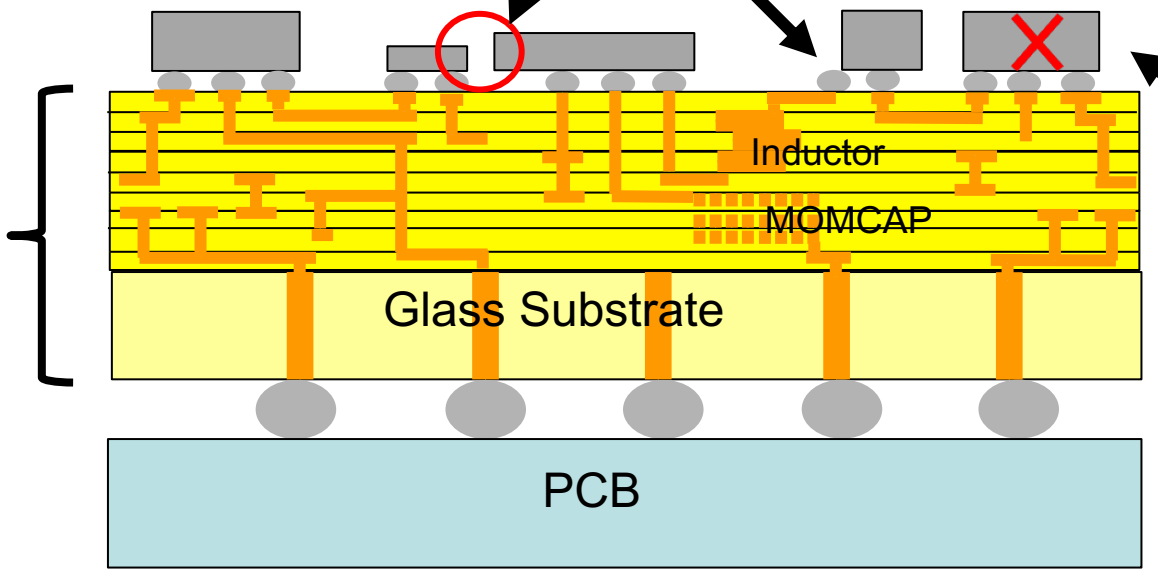
Package Yield

Systematic Yield

Die come from multiple vendors
Wiring design & die spacing affects system delays
Pick-N-Place accuracy

Parametric Yield

Wiring Sheet Rho
Contact chains
Basic Inductance
Basic Capacitance
TGV Conductivity



Random Defect Yield

Bad Die

- Analogy to Yield in the Chip World:

  Yield = Parametric Yield x Systematic Yield x Random Defectivity Yield

This needs to be >98%.
No questions asked.

You can't hit this if you're straining to pattern line/space.

This is where you want to spend your development engineering time

"Incoming QC"

Specialty Applications

- For High-Temp / High-Stress applications (incl. Military):
  Polymers will not work – they decompose above 350C
  If the Cu/SiO2 chip can withstand the extremes, a Cu/SiO2 package can –
  It's no longer a materials problem – it's a structure problem (much more solve-able).
  This drastically improves timelines.

- Hermetic packaging: Polymers are always an issue, and thus require additional packaging (metal, ceramic, glass) to provide hermeticity.
  ➔ … so just use Glass to start with!
  Hermeticity comes for free (now just a structure/design problem)

Some Thoughts On Cost

- The first and strongest push-back: … but Damascene Glass is too expensive!
  Right. But that's also what the industry said about:
  - Plate/Polish Cu instead of Dep/Etch Al for BEOL
  - HiK-Metal Gate
  - Epi Source Drain

  ➔ In the end, the benefits of scaling / performance outweighed the cost.
  Chipmakers made the switch, and never looked back.
  A big change is not an endpoint – it is a starting point. It opens up unforeseen horizons.
- A reasonable estimate is 25-30% more for damascene Glass RDL, vs. Polymer RDL.*
  - But remember: RDL is only a portion of the total packaging cost (Substrate, TGVs, Die-Attach, Add'l Passives)
- Time is Money. Faster development (copy/paste from BEOL) is a significant win.
- Packaging is not an afterthought – it now lies directly in the scaling critical path.
  ➔ The Semiconductor Industry cannot continue to place greater demands upon packaging and assume it'll come free.

Summary

- Switching to glass substrates, but maintaining polymer RDL, is hindering progress.
- Damascene Cu/SiO2 is a well-proven, high-volume production technology

  ➔ The tools, experienced people, even devices w/ reliability data already exist.
- Damascene Cu/SiO2 would simultaneously and immediately:
  - Eliminate packaging's Line/Space scaling concerns for 20 years
  - Enable 10+ layers of RDL, w/o requiring fine-pitch TGV (easily meets multi-chip, complex wiring)
  - Enable complete flexibility for hybrid bonding (die-to-package, package-to-package)

  } Scaling
  - Enable significantly enhanced RF performance (20-100 GHz), across broad temperature ranges
  - Enable 100 GHz+ operation (polymers will not work here), so no need to re-develop

  } RF
  - Enable high-performing photonics – SiN/SiO2 as top-level RDL is an ideal photonics layer
  - Eliminate the need for chips at multiple levels in the package - all can just sit on top of RDL stack.

  } Photonics
  - Eliminate most reliability concerns, since it's already been thoroughly tested
  - Enable extreme environments – if the chip can do it, the package can do it
  - Greatly simplify hermetic packaging

  } Reliability & Specialty
  - Drastically reduce development timelines

  } Time-to-Market

➔ Glass-on-Glass is worthy of a serious evaluation