

Bump on Flexible Lead for Wafer Level Packaging

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Abstract

A chip-to-substrate interconnect technology is introduced which uses flexible structures to accommodate the CTE mismatch between the chip and PCB substrate and consequently should be reliable without underfill. Increased flexibility, i.e. purely elastic response, of the bumps can lead to an increase in the reliability of large Flip Chips. To achieve a high flexibility, the lead-free bump is located on a flexible lead. The flexible lead consists of a copper line embedded in a polymer-bridge which is located over an air gap. For a small bump height, which is necessary to achieve a small package height, the stress due to CTE mismatch is then accommodated within the flexible lead. FEM simulations were performed and prototype chips have been designed and fabricated using wafer level packaging processing methods, such as photolithography, electroplating and wet-etching. The process flow and assembly of the flexible interconnects without underfill are presented and discussed. Key words: Wafer Level Package, WLP, flexible

Introduction

Chip Size or Chip Scale Packages (CSPs) are widely used in portable electronic equipment like cellular phones, because of their smaller size and better applicability to high-frequency devices than traditional lead-type packages like the thin small outline package (TSOP).

Wafer Level Packaging (WLP), which simply extends the back-end of line (BEOL) in chip production, is a packaging process where the package is fabricated directly on the wafer. The wafer is then singulated by dicing and the resulting CSPs are mounted onto printed circuit boards (PCBs).

A frequently observed failure mode in these packages is solder fatigue [1, 2]. A mismatch of the coefficient of thermal expansion (CTE) between the silicon chip and the PCB causes thermal stress in the package due to the mounting of the CSPs onto the PCB. The chip and board are too stiff to contribute much to the accommodation of the thermal mismatch, therefore in WL-CSP the solder joints have to carry the entire load. Particularly for large-size chips (about 100 mm²) like DRAMs or ASICs this becomes a serious problem.

A common approach used to overcome this problem is to use an underfill between chip and substrate. Here, the underfill ties chip and substrate strongly together. To accommodate the thermal stress

the whole system will bend. This in turn reduces the load on the solder balls and thus the accumulated inelastic strain within them, which increases the reliability of the system [3-5]. Recently low-k interlayer dielectric (ILD) materials are the focus of research to improve electrical performance of microprocessors. Bending of the chip will ultimately induce cracking and delamination of the mechanically weak low-k ILD materials [6]. Furthermore, underfilling is an additional process step during the assembly which increases the assembly time and cost.

Therefore, in recent years several compliant interconnect technologies [7-13] have been studied to eliminate the need for underfill. One way to increase the reliability of the solder joints is to increase their height by using larger solder balls [7] and by providing an additional copper- [8], solder- [9] or polymer- [10, 11] post. Using this approach means, as the chip size increases, the standoff distance of the interconnects must also increase. To achieve good reliability also for large-size chips without increasing the overall package height, an additional compliancy in x-y-direction is necessary. To accommodate unevenness in the PCB a compliancy in z-direction is also important. Georgia Tech therefore invented the so called "Sea-of-Leads (SoL)" [12, 13]. One type of SoL, the "slippery type" SoL [12] has a good compliancy in all directions, but is not easy to handle during board assembly. Another type, the SoL with embed-

ded air gaps [13], is specially designed for out-of-plane (z-direction) compliancy.

In this paper a bump-on-flexible-lead (BoFL) wafer level package is introduced (Fig. 1). To achieve a high flexibility in x-, y- and z-direction, the lead-free bump is located on a flexible lead. The flexible lead consists of a copper line embedded in a polymer-bridge which is located over an air gap.

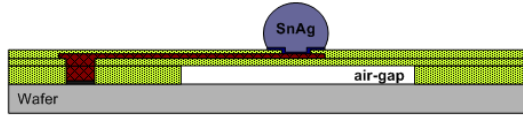


Fig. 1: Bump-on-flexible-lead (BoFL)

Simulation

3D Finite element models were built to compare the conventional WLP with the bump-on-flexible-lead WLP. The objective is to compare different designs prior to fabrication by numerical means in order to obtain the influence of the some geometric key parameters with respect to optimised, i.e. lowest stress. This can be done by Finite-Element simulations. The simulation was done by using the commercial software ANSYS. A simplified model is used for this study, to reduce calculation time. In addition, as this study is only meant to be a qualitative comparison between the different package types, a gain in absolute accuracy is not important for the time being. It is made use of the fact that the highest stress during thermal cycling appears on the outermost bump, which is a good approximation for a flip-chip without underfill [5]. Figure 2 shows the 3D FE model of a banana-shaped BoFL.

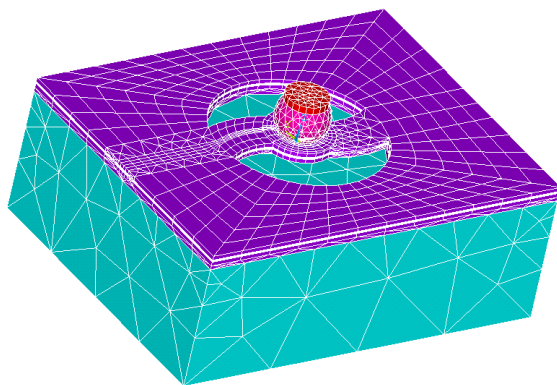


Fig. 2: Finite element model of a banana-shaped bump-on-flexible-lead.

The bump is 65 μm in height and the contact area on the pad is 100 μm in diameter. On top of the bump 17 μm copper is added, which represents the PCB pad. On chip side, the bump is located on a polyimide bridge, with the embedded copper lead. The geometry data as i.e. thickness of the copper layer, are the same as reported in the fabrication section of this paper. For the simulation, all materials are assumed to have elastic behavior. The material data used for the simulation is given in the Table I.

Table I: Material data

Material	E [GPa]	PR	CTE [ppm/K]
Si	168	0.3	2.8
Cu	97	0.35	16.5
SnAg	44	0.36	21
Ni	230	0.3	12.5
PI	2.5	0.3	41

Two other 3D-FE models were built, a bump-on-flexible-lead with a straight lead and a conventional WLP. For the conventional WLP, the same geometry was used, but here, the air gap was filled with polyimide.

In the calculations, the materials were – for a first try - assumed to be joined and stress free at room temperature. The planar displacement applied in x- and y-direction is calculated by the following equation

$$u = DNP \cdot (CTE_{PCB} - CTE_{Si}) \cdot \Delta T \quad (1)$$

where u is the displacement, DNP is the distance to neutral point, i.e. the distance from the chip centre to the outermost bump, CTE is the coefficient of thermal expansion of the material noted in subscript (PCB or Si) and ΔT is the change of temperature. By using this equation, one assumes that the silicon and the PCB will be at the same temperature and will not bend. For a $1 \times 1 \text{ cm}^2$ die with a $CTE = 2.8 \text{ ppm/K}$ joined to a PCB with a $CTE = 13 \text{ ppm/K}$, the displacement in x- and y-direction is $u_x = u_y = 4.5 \text{ }\mu\text{m}$ under a temperature change from 25°C to 125°C .

It is observed, that for the conventional WLP the highest stress appears in the bump and in the bump pad, while for the BoFL WLP the highest stress is in the copper lead. The von Mises stress in the copper of a BoFL is reduced by half of the magnitude compared to the conventional WLP (not depicted).

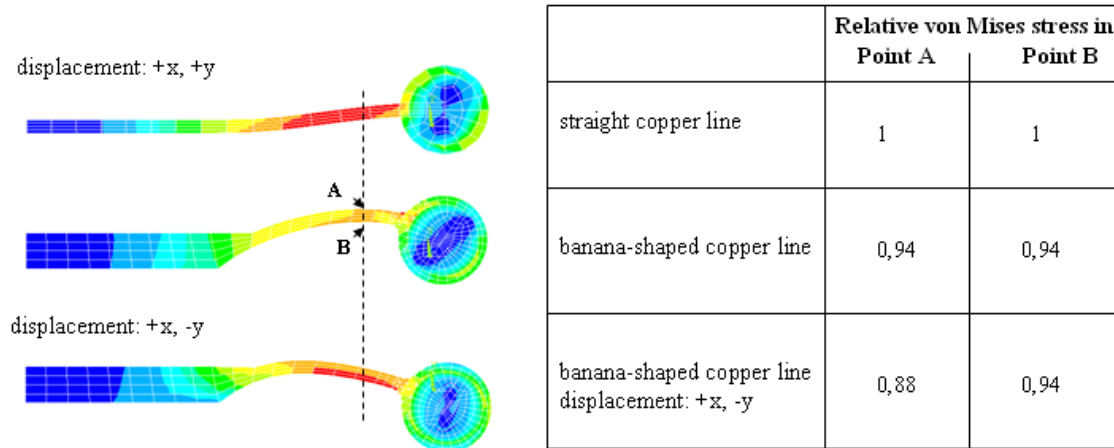


Fig. 3: Von Mises stress distribution of a BoFL WLP with a straight and a banana-shaped copper lead for different directions of x-y displacement

To further reduce the stress in the copper lead of the BoFL WLP, the shape of the copper lead was modified. Figure 3 shows the von Mises stress distribution in a straight copper line and in a banana-shaped copper lead for displacement in x-y-direction. Since the banana-shaped copper lead is not symmetric, the influence on the direction of the applied displacement was also studied. To compare the simulations, the von Mises stress of two areas in the lead (labeled with A and B in Fig. 3) are compared. The von Mises stress serves as an estimate for the 3D stress to potentially induce plastic strain which in return could serve as failure criterion in a reliability analysis. The simulations show, that the stress in the copper trace of the flexible WLP can be reduced by modifying the shape of the copper lead. Furthermore, a dependence on the direction of the applied displacement on the overall stress can be seen. Due to the relative gentle bow of the banana-shaped copper lead, the effect of the shape on the overall stress is not so high. The influence of the lead geometry for further stress reduction will be investigated.

So far the simulations represent only a very rough approach to a qualitative study in order to get first indications as to what direction to advance further investigations. In a further study the process conditions have to be included in the simulations as well as plastic material properties for copper and rate-dependent material data for solder and polymer [4, 14].

Fabrication

150 mm wafers with copper daisy-chain test patterns were used for electrical and mechanical evaluation of the bump-on-flexible-lead WLP. Two different chip types, a DRAM-type (10 mm x 5 mm)

and a Flash RAM-type chip (5 mm x 2.5 mm), with different bump pitches (700, 500 and 150) number of I/Os (54 and 43) and different lead designs were fabricated (Fig. 3 and Fig. 4).

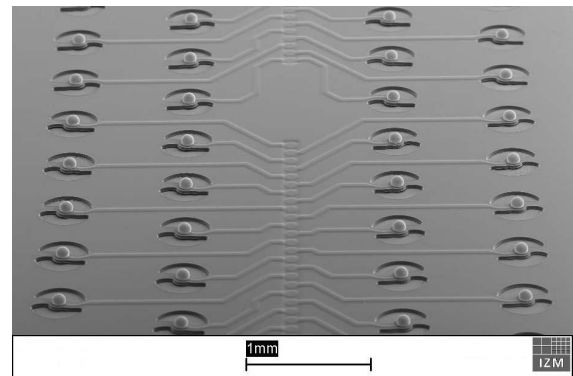


Fig. 3: SEM picture of a DRAM-type chip with bump-on-flexible-lead WLP

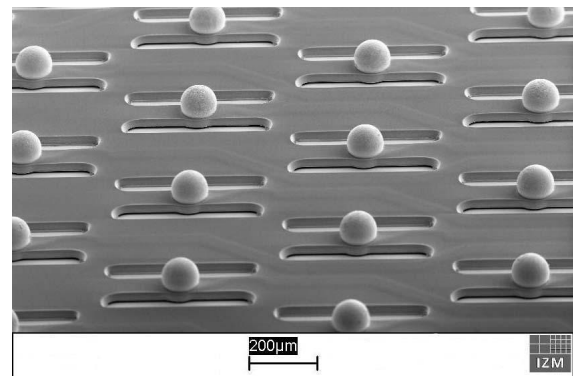


Fig. 4: SEM picture of a Flash RAM-type chip with bump-on-flexible-lead WLP

A schematic sectional drawing of the process flow is shown in Fig. 5. First, a 15 μm copper sacrificial layer was electroplated. In the same process step, copper studs were electroplated on the chip pads (Fig. 5a). A thin Ti:W (100 nm) and 300 nm Cu layer was sputtered uniformly over the entire wafer. Ti:W serves as a diffusion barrier and the sputtered Cu as the plating base. A positive working photoresist (AZ 9260) was used to create the plating mask. After plating the copper sacrificial layer, the plating mask and the sputter layers were removed.

Here, copper was used as the sacrificial layer due to both the ease of deposition of this material through electroplating as well as the ability of the polyimide to withstand the standard copper etchants. An aluminium sacrificial layer could also be used [15]. Since aluminum is deposited via evaporation, the thickness of the sacrificial layer would be limited to a few micrometers.

Then, a thick polyimide (Du 7320) passivation layer was deposited onto the wafer by spin coating. To provide an access to the copper layer, the polyimide was planarized by chemical mechanical polishing (Fig. 5b).

Subsequently, a second polyimide layer was deposited to form the bridge over the sacrificial layer. Using a photolithographic mask, the polyimide was patterned and then developed. After the cure, the polyimide layer had a thickness of 5 μm or 10 μm (Fig. 5c). Polyimide (Du 7320) is used as the mechanical material for several reasons. First, polyimide is a standard material used for WLP acting as passivation layer. Also, it can elongate significantly under thermo-mechanical stress, which is crucial for the flexibility of the structure. Finally, polyimide is under residual tensile stress [16], which holds the structure above the wafer surface after release.

In the following step electroplating of the copper redistribution layer was done in the same way

as the electroplating of the copper sacrificial layer. (Fig. 5d) Here, the thickness of the copper was 5 μm . Different types of copper lines were fabricated; a straight line, a banana-shaped (Fig. 6) an s-shaped and a curl-shaped copper line (Fig. 7).

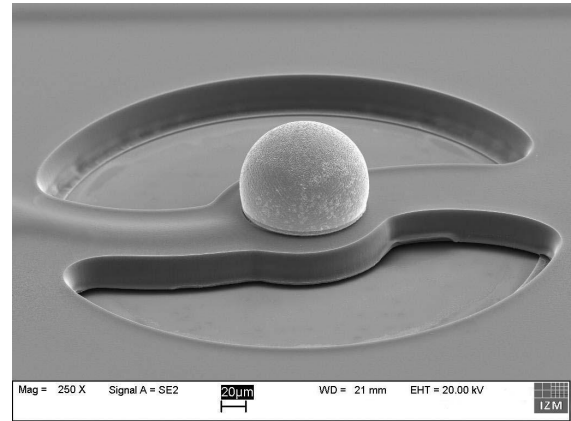


Fig. 6: SEM picture of a banana-shaped bump-on-flexible-lead

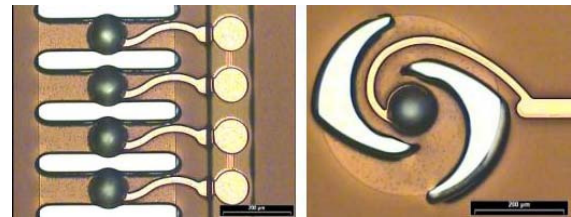


Fig. 7: Microscopic picture of an s-shaped (150 μm pitch) and a curl-shaped bump-on-flexible-lead.

Then a polyimide soldermask layer was deposited (Fig. 5e). The patterning was done in the same manner as before. The resulting thickness of the polyimide layer above the copper was 5 μm .

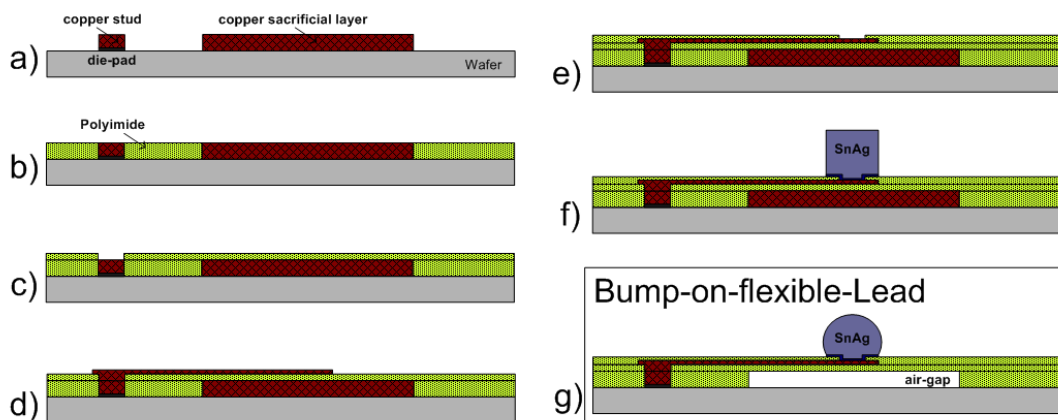


Fig. 5: Process-flow of the bump-on-flexible-lead (BoFL)

The next process step was the electroplating of the under bump metallization (UBM) and the SnAg solder bump (Fig. 5f). The UBM consists of a sputtered Ti (20 nm) adhesion layer, and a sputtered Ni (300 nm) plating base. To obtain a reliable solder interconnect, an additional 5 μm of nickel was electroplated [17, 18]. The diameter and the height of the bumps were 100 μm and 70 μm respectively. Figure 8 shows a cross section of a bump-on-flexible-lead after the electroplating of the SnAg bump. The copper sacrificial layer beneath the bump is clearly visible. Before the preparation of the cross-section, the sample was sputtered with thin gold. This was done to obtain a good visible boundary between the sample polyimide and the embedding material.

In the following step, the solder bumps were reflowed. To release the flexible leads, the copper sacrificial layer was wet etched for approximately 30 minutes in a copper chloride solution (Fig. 5g). Finally, the wafers were diced. During dicing the chips were protected with a photoresist. Figure 9 shows a cross-section of a completed bump-on-flexible-lead.

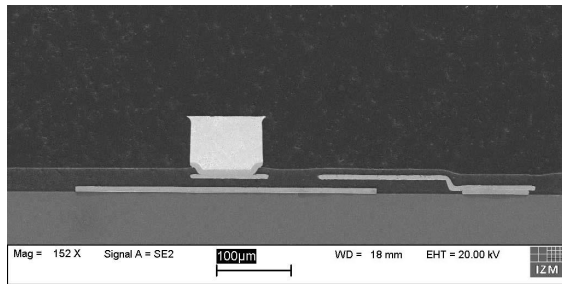


Fig. 8: Cross-section before reflow and before etching of the copper sacrificial layer beneath the bump.

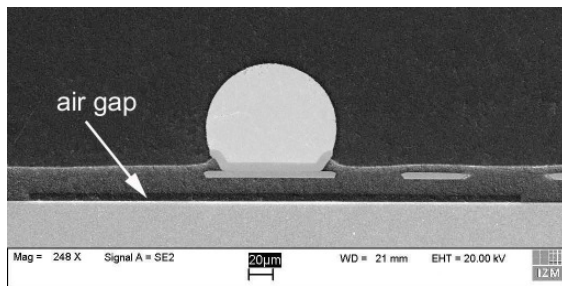


Fig. 9: Cross-section of a completed bump-on-flexible-lead WLP with air gap

Assembly

For reliability tests, the chips will be assembled on low cost single sided FR-4 boards. The metallization of the PCB consists of 17 μm laminated copper, 5 μm nickel and a thin flash gold layer. The soldermask has a thickness of 13 μm and openings of 150 μm diameter.

Chips were already assembled using a fine-placer with a split optic. The chips were dipped in flux (30 μm) prior the placing onto the FR-4 board. Reflow was done in a convection oven with a peak-temperature of 262 $^{\circ}\text{C}$. In Figure 10 a cross-section of an assembled chip is shown. The height of the SnAg bumps after assembly was 65 μm .

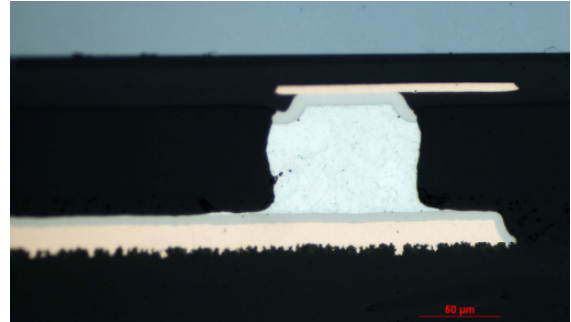


Fig. 10: Microscopic picture of a bump-on-flexible-lead WLP mounted on a PCB

Summary

The fabrication and assembly of a flexible Wafer Level Package has been demonstrated. The bump-on-flexible-lead (BoFL) WLP can be fabricated using the same process techniques, such as photolithography and electroplating, used in conventional WLPs. First FE simulations illustrated the ability of the BoFL WLP to reduce the stress in the solder interconnects which is introduced by the CTE mismatch of the silicon and the PCB. This in turn will lead to a higher reliability of the assembly. Future work will include further design optimization, more detailed modelling, and reliability tests of the assembly.

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References

- [1] J.H. Lau. Thermal Stress and Strain in Micro-electronic Packaging. Van Nostrand Reinhold, New York, 1993.
- [2] H. Reichl, A. Schubert, and M. Töpper. Reliability of Flip-Chip and Chip Size Package. Microelectronics Reliability, (40):1243–1254, 2000
- [3] A. Schubert, R. Dudek, E. Auerswald, A. Gollhardt, B. Michel and H. Reichl: Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation. 53rd Electronic Components and Technology Conference

- rence, New Orleans, USA, May 27-30: 603-610, 2003.
- [4] B. Wunderle, R. Dudek, B. Michel and H. Reichl, "Thermo-Mechanical Reliability of Power Flip-Chip Cooling Concepts", 54th Electronic Components and Technology Conference, Las Vegas, USA, June 1-4, 2004: pp. 427-436, 2004.
 - [5] M. Spraul, W. Nüchter, B. Wunderle, B. Michel, "Comparison of Lifetime Predictions with 3D Finite Element Models of a High Density Flip Chip without Underfill on LTCC", Proc. 6th EuroSI-ME 2005, Berlin, Germany, pp. 441-447, 2005.
 - [6] C.J. Zhai, U. Ozkan, A. D. Sidharth, R.C. Blish, R. N. Master, "Investigation of Cu/Low-k Film Delamination in Flip Chip Packages", Proceedings of the 56th Electronic Components and Technology Conference (ECTC), San Diego, California, May 30-June 2, pp. 709-717, 2006
 - [7] S.-Y. Jang, T.-S. Park, Y.-S. Kim, J.-W. Jeong, J.-J. Bang, D.-K. Kang, "Wafer Level Package Solder Joint Reliability Study for Portable Electronic Devices", 55th ECTC, Lake Buena Vista, Florida, May 31-June 3, pp. 660-664, 2005
 - [8] T. Kawahara, "Super CSP™", IEEE Transaction on Advanced Packaging, Vol. 23, No. 22, pp. 215-219, May 2000
 - [9] M. Töpper, J. Auersperg, V. Glaw, K. Kaskoun, E. Prack, B. Keser, P. Coskina, D. Jäger, D. Pether, O. Ehrmann, K. Samulewicz, C. Meinherz, S. Fehlberg, C. Karduck, H. Reichl, "Fab Integrated Packaging (FIP): A new Concept for High Reliability Wafer-Level Chip Size Packaging", 50th ECTC, Las Vegas, Nevada, May 21-24, pp. 74-80, 2000
 - [10] G. Gardner, B. Harkness, E. Ohare, H. Meynen, M. Vanden Bulcke, M. Gonzalez, E. Beyne, "Integration of a Low Stress Photopatternable Silicone into a Wafer Level Package", 54th ECTC, Las Vegas, Nevada, June 1-4, pp. 170-174, 2004
 - [11] R. Dudek, H. Walter, R. Doering, B. Michel, T. Meyer, J. Zapf, H. Hedler, "Thermo-mechanical design of resilient contact systems for Wafer Level Packaging", EuroSimE, Delft, The Netherlands, April 24-26, pp. 1-7, 2006
 - [12] B. Dang, M.S. Bakir, G. Lo, K.P. Martin, J.D. Meindl, "Assembly and Reliability Assessment of Sea-of-Leads Compliant Wafer Level Package", International Symposium on Microelectronics, Long Beach, California, November 14-18, pp. 7-14, 2004
 - [13] M.S. Bakir, H.A. Reed, H.D. Thacker, C.S. Patel, P.A. Kohl, K.P. Martin, J.D. Meindl, "Sea of Leads (SoL) Ultrahigh Density Wafer-Level Chip Input/Output Interconnections for Giga-scale Integration (GSI)" IEEE Transactions on Electron Devices, Vol. 50, No. 10, pp. 2039-2048, 2003
 - [14] Dudek, R. (2006) Characterisation and modelling of solder joint reliability, in Mechanics of Microelectronics (eds G.Q. Zhang, W.D. van Driel and X.J. Fan), Springer, pp. 377-468.
 - [15] M. A. Schmidt, R. T. Howe, S. D. Senturia, J. H. Haritonidis, "Design and Calibration of a micro-fabricated Floating- Element Shear-Stress Sensor", IEEE Trans. on Electron Devices, vol. 35, No. 6, pp.750-757, 1988
 - [16] Y.-J. Kim, M. G. Allen, "In Situ Measurement of mechanical properties of polyimide films using micromachined resonant string structures", Transactions on components and packaging technology, vol. 22, no. 2, pp. 282-290, June 1999
 - [17] K. O'Donnel, D. Gupta, P. Silberud, C. Lopper, L. Dietrich, M. Töpper, "Characterization of reaction rates and intermetallic phase formation for Cu, Ni and NiV UBM layers with SnPb and lead-free SnAg solders", 5th Annual SECAP East Asia Seminar Series, November 2004
 - [18] B. Ebersberger, R. Bauer, L. Alexa, "Qualification of SnAg Solder Bumps for Lead-Free Flip Chip Applications", 54th ECTC, Las Vegas, Nevada, June 1-4, pp. 683-687, 2004