

Packaging of GaAs Chips for Use in RF MCM Products

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Abstract

Incorporation of GaAs devices in a multi-chip module (MCM) process in which the chips are put down first, followed by buildup of their interconnect structure, presents several problems. First, GaAs devices are much thinner than the silicon chips and passive components that are typically used. Second, a low impedance electrical connection to the backside of the GaAs device is usually required. And third, it is desirable to surround the chip with a metal shield structure. All three of these issues have been addressed with a chip scale package fabricated from sheet copper stock. This package is fabricated by etching cavities through the sheet to form the die cavity. Next, Kapton film is bonded to one side of the sheet, to form the package bottom. Then, the entire chip cavity is metalized with gold. The metallized sheet is then mounted to a thermal release tape so that the individual carriers can be diced from the substrate. The device is bonded to the bottom of the carrier with conductive adhesive. The fully assembled package is then removed from the thermal released tape after the curing the conductive material. The package has proven to be robust, fully compatible with the MCM assembly process, and also offers some benefits with respect to thermal management.

Key Words: multichip module, GaAs, chip scale package

Introduction

A packaging technology was developed for bare die GaAs devices that allows them to be embedded in multi-chip modules (MCM) fabricated by a chips first assembly process^[1]. This packaging approach addresses three issues associated with the GaAs die; (1) it increases the die thickness to match that of the module components, (2) it provides a low impedance backside connection to the die, and (3) it surrounds the die with an electrical shield. In what follows, we briefly describe our initial approaches to packaging the GaAs die and the observed issues associated with them. Next, we describe our successful packaging process and proceed to evaluate both its thermal and electrical performance as a function of various construction features. Finally, we suggest how this packaging concept may also be useful in surface mount applications.

Package Design

The package design for integrating the GaAs devices with the MCM process went through several iterations. The original concept for the design was an all-metal can. There were two different fabrication approaches explored. The first approach was a combination of machining and lapping processes. The second was a wet chemical etch process. Issues were seen in both approaches. In the mechanical

approach, an array of device diameter openings of 0.034in was drilled to a depth of 0.005in within a 0.008in thick Cu shim stock. The outer frame of the carrier was drilled centered about each hole to a depth of 0.006in, Figure 1.

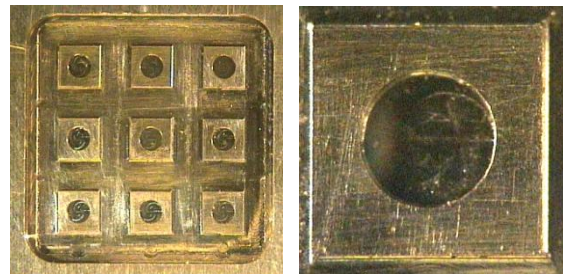


Figure 1. Optical images of 3 x 3 carrier array within the frame (left) and higher magnification view of one of the carriers within the array (right).

The carrier frame was then sputter coated with Ti followed by Au to provide the electrical contact for the backside of the die. Once the sputter process was completed, the carrier frame was mounted upside down to a sheet of thermal release tape. The backside of the frame was then lapped. The amount of material needed to be removed to separate the array into individual carriers was 0.002in. However, the thermal release tape material was compliant and

the center of the arrays bowed significantly, therefore the carriers could not be separated. Another concern with this mechanical approach was the repeatability of drilling to the 0.005in depth within the 0.008in thick Cu material.

Using the same dimensions as the in-house mechanical process (0.060in x 0.060in x 0.006in thick with a 0.005in deep 0.034in diameter hole), individual copper carriers were fabricated by an outside supplier using wet-etch chemical processing. However, closer investigation of these etched carriers showed there was a taper in the pocket's diameter from the top surface of the carrier to the bottom of the pocket, Figure 2.

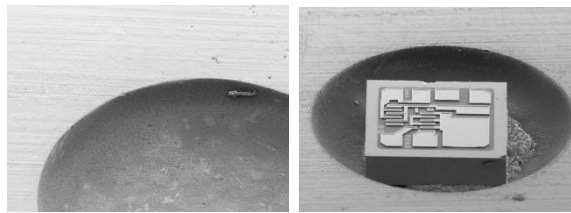


Figure 2. Scanning Electron Microscopy (SEM) images of chemically etched carriers (left) as-received and (right) containing a GaAs die.

The taper at the pocket's bottom on the chemically etched carriers may result in the dies not sitting flush inside the pockets, as shown in Figure 2. This could potentially lead to cracking during the lamination process which involves both vacuum and pressure for stacking the dielectric material used for the interconnect layer on top of the components. To ensure that the bottom of the chemically etched carriers is flat, the diameter would need to increase. The overall dimensions of the carrier would possibly have to increase to accommodate vias from the above metal layer. This could potentially limit future design goals of reducing the overall size of the module.

To remedy the issues seen in both designs for an all-metal carrier, a concept was developed which incorporated a polyimide film with a copper frame to form the carrier. The polyimide film has a total thickness of 1.0mil, consisting of 0.5mil Kapton HN and 0.5mil R-Flex 1000 adhesive (Rogers Corporation). This film served as the backing, or bottom, of the carrier. For the first phase of this design, all the features for the carrier were machined in-house. However, metal and polyimide burs were observed, on both the top and bottom surface in some cases, Figure 3.

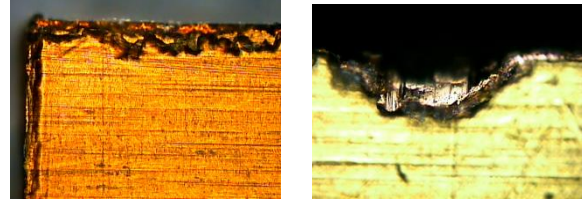


Figure 3. Optical images of polyimide burs observed on the carrier's backside (left) and a metal bur found on the front side (right).

A switch to chemical etch copper frames eliminated a majority of the machining process, Figure 4. This significantly reduced the incidences of metal burs forming on the top surface of the carriers. The throughput of fabricating the carriers was also increased since the etch process was simple and quick, and with the process being a thru-etch, the feature dimensions were kept within the specified tolerances.

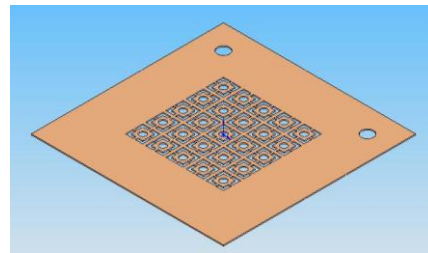


Figure 4. Illustration of an array of copper frame fabricated using a chemical etch process.

To address the issue of Kapton frays being generated along the side and bottoms of the carriers during the final machining step, a laser cutting process was implemented. With the use of the laser, a profile program was created to score the dielectric material on bottom of the substrate, Figure 5. The laser cut is made in board of the final cut to ensure that the machining tool would only be cutting through the metal substrate.

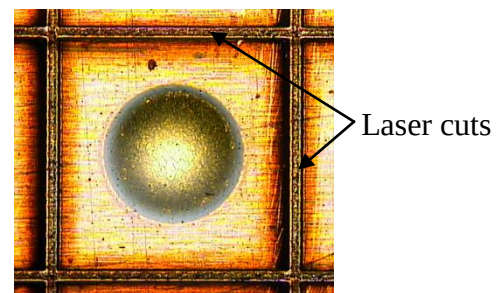


Figure 5. Optical image of the backside of a carrier within the array after laser processing.

Fabrication

In the current process, the chemically etched copper frames are fabricated by TECH-ETCH, Inc. Each substrate, 1.0in x 1.0in x 0.005in, contains 25 frames in a 5 x 5 array. After visual inspection, a sheet of the polyimide material described earlier is laminated to the backside of the substrate, Figure 6.

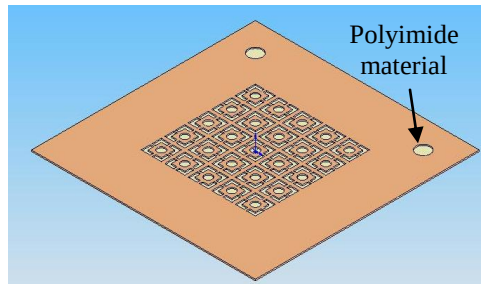


Figure 6. Illustration of the carrier substrate with polyimide material laminated onto the backside.

After lamination, the substrate is placed into a vacuum oven for a minimum of 12 hours at 120°C to ensure that any residual solvents are driven off prior to the sputter deposition process. An adhesion layer of 1000Å of titanium is deposited followed by 1000Å of gold. The sputtered metals coat both the top surface and the interior of each of the carriers, Figure 7.

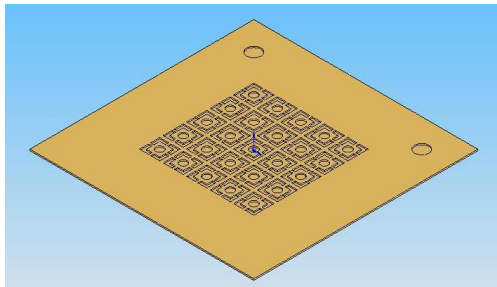


Figure 7. Illustration of the carrier substrate after Ti/Au sputter deposition.

After sputter deposition, the backside of the substrate undergoes a laser process which removes the polyimide material around the individual carriers. As stated earlier, this process was implemented to reduce the chances of burs forming on the backside of the carriers due to the machining process used for singulating the individual carriers. Prior to singulating the carriers after the laser process, the substrate is placed on a thermal release tape. This allows the carriers to be singulated, but the CNC machining tool does not cut through the release tape, thus allowing them to still be arranged in a substrate form. Keeping the carriers, now individualized, in this arrangement serves two main purposes. One, the

form factor of the substrate (1.0in x 1.0in) is easier to handle than the individual carriers, which are 0.060in x 0.060in. Secondly, the thermal release tape is then mounted to an alumina substrate, which provides a robust surface for the die placement process, Figure 8.

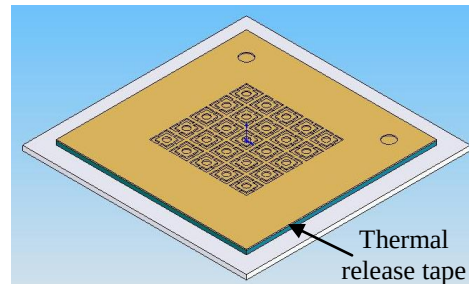


Figure 8. Illustration of the carrier substrate mounted to an alumina substrate using a thermal release tape.

Prior to placing the GaAs dies into the carriers, conductive epoxy is dispensed inside each carrier using a West Bond Dual Head Die Bonder (West Bond model 7200CR). By using a specific nozzle diameter and dispense settings, the amount of epoxy dispensed can be accurately controlled, Figure 9. The conductive epoxy used is H20E (Epoxy Technology), which is an Ag base epoxy. The epoxy provides both adhesion as well as the conductive path to the backside of the die.

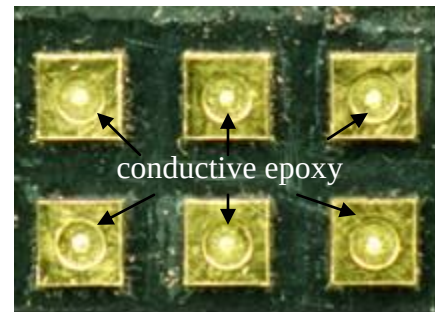


Figure 9. Optical image of several carriers on the thermal release tape after H20E conductive epoxy dispense using the West Bond.

After dispensing the conductive epoxy into each carrier of the array, the entire substrate is then moved to a pick and place machine, where the bare GaAs dies are inserted into each carrier. The FineTech pick and place tool has a vision system with the capability of viewing both the carrier and the backside of the die. This provides the user more accuracy in aligning the bare die to the center of the cavity as well as ensuring the die and carrier edges are parallel to one another, Figure 10.

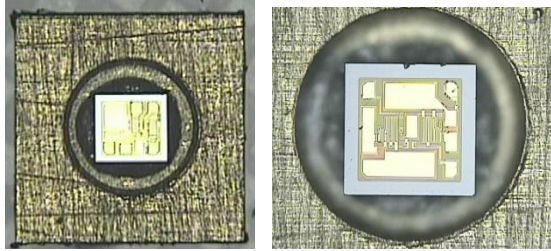


Figure 10. Optical image of a bare die mounted inside the carrier, full view (left) and at higher magnification (right).

Once all the carriers in the array are populated with dies, the substrate is placed in a 120°C oven for 15 minutes. This temperature cures the conductive epoxy and activates the thermal release tape. The individual parts (carrier and die) can then be removed from the tape, and placed into a waffle and gel pack for inspection and testing if required. SEM image of a completed part is shown below in Figure 11.

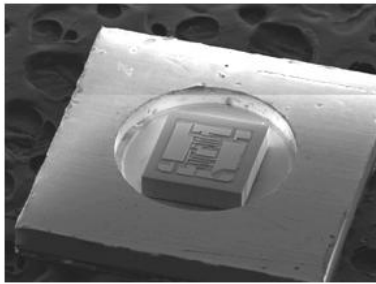


Figure 11. Scanning Electron Microscopy (SEM) image of an individual part (bare die within a carrier).

Performance Modeling

The thermal and electrical characteristics of the die carrier were investigated with the aid of a three dimensional, finite element model of one quarter of the actual structure. Dimensioned, plane views of the model structure are shown in Figure 12. Symmetry boundary conditions are assumed on the x-z and y-z planes, i.e. there are no fluxes of heat or electrical current across these planes, so only a quarter of the actual structure is modeled. A finite element mesh of the model was assembled from 6245, four node, tetrahedron elements that were generated by the program Gmsh^[2]. The elements vary in size by a factor of 10; the smallest are used to model the Kapton film and electroplated copper layer. The largest elements are used on the external surfaces of the structure. A picture of the meshed model appears in Figure 13. The model shown in Figure 12 is comprised of five different materials. The thermal

conductivities and electrical resistivities of these materials are listed in Table 1.

The thermal performance of the die and carrier assembly was evaluated by fixing the temperature of the bottom surface of the alumina substrate at 0°C, while dissipating constant power within the top surface layer of the chip. Figure 14 presents the temperature distribution that is calculated by the finite element program tochnog, when one Watt is dissipated in the chip, i.e. one-quarter Watt in the modeled quadrant^[3]. For this case, the maximum chip temperature is just 11.4°C above that of the substrate bottom surface. The copper block that surrounds the chip is at a constant temperature that is equal to half the maximum chip temperature. This suggests that the thermal impedance of the block is negligible compared to that of the Kapton film and plated copper layer.

In this model, the thermal conductivities are all constants, independent of temperature. So when the chip power dissipation is increased to 10 Watts, all temperatures rise by a factor of 10, but the relative distribution, remains unchanged, as shown in Figure 15. At this power dissipation level, the chip is approaching its upper operating limit.

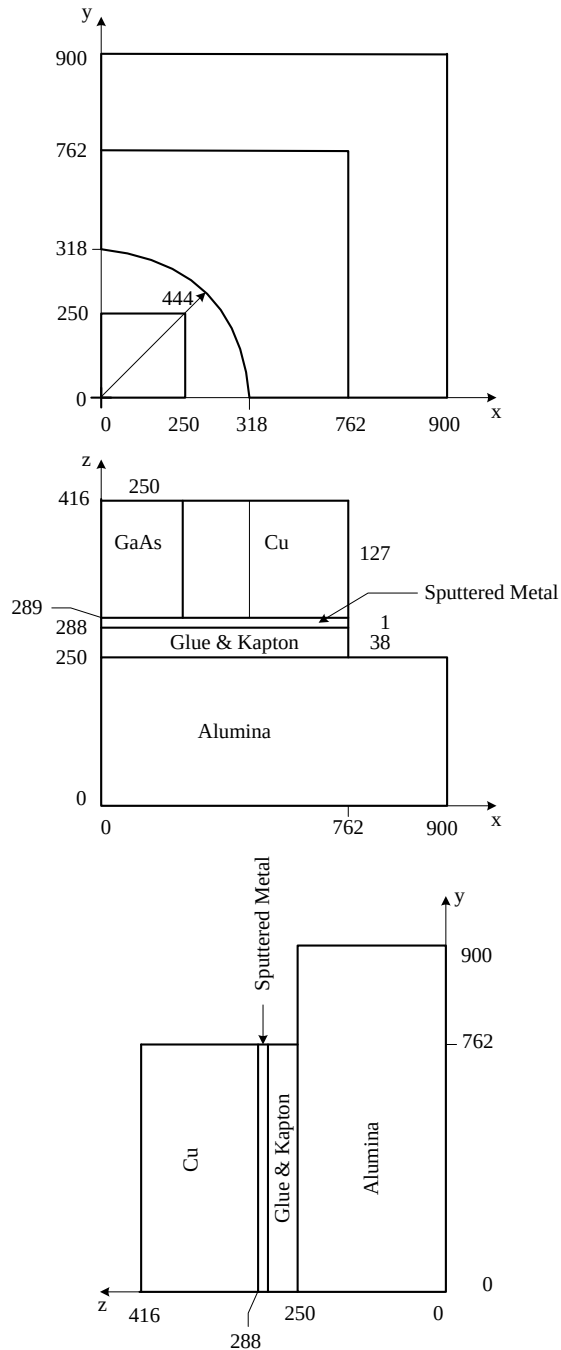


Figure 12. Plane views of structure used for finite element model. All dimensions are in microns. Not drawn to scale.

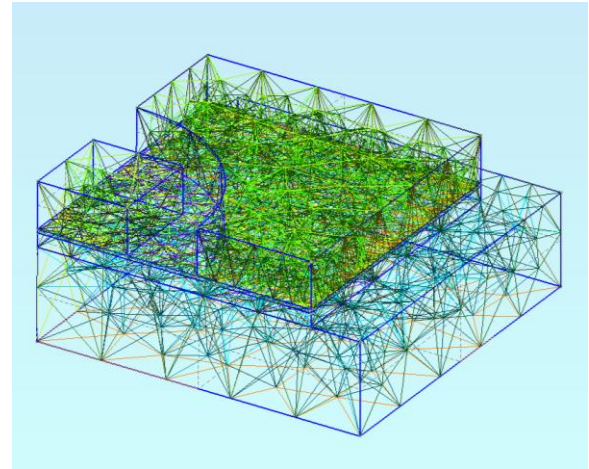


Figure 13. Perspective view of quarter model of die carrier meshed with tetrahedron elements of varying size.

Table 1. Material Properties

Material Type	R	k
	[Ω -cm]	[W/ m K]
GaAs		55.0
Plated Copper	1.00×10^{-6}	200.0
Kapton/Glue	4.00×10^{19}	0.12
Bulk Copper	1.71×10^{-6}	391.0
Alumina 99%	2.00×10^{13}	18.0

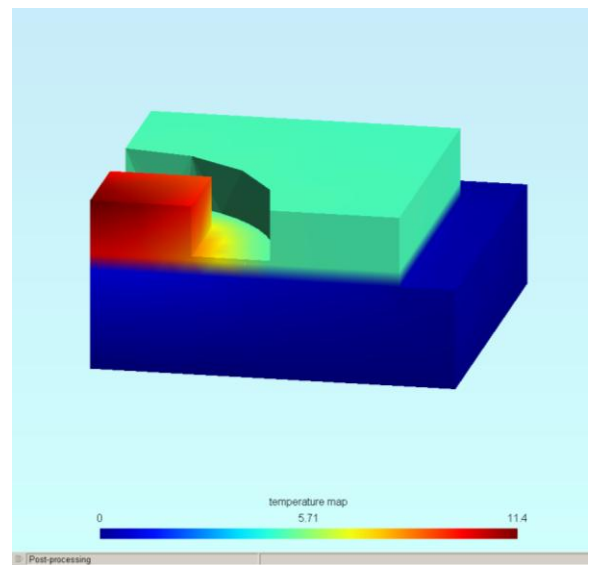


Figure 14. Temperature distribution in standard die carrier assembly with one Watt of power dissipated in chip.

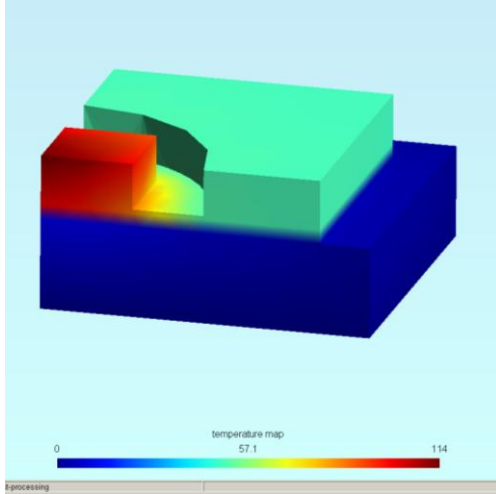


Figure 15. Temperature distribution in standard die carrier assembly with ten Watts of power dissipated in chip.

Two things can be done to improve the package performance. First, the thermal impedance of the plated copper layer could be reduced by making it thicker. Figure 16 shows the temperature distribution, which is achieved by plating the copper film three times as thick as the nominal configuration, with 10 Watts of power dissipation in the chip. This configuration reduces the chip temperature to 93.6°C and raises the temperature of the copper block closer to that of the chip. The temperature of the copper is still uniform, as expected because the Kapton layer presents a very high thermal impedance.

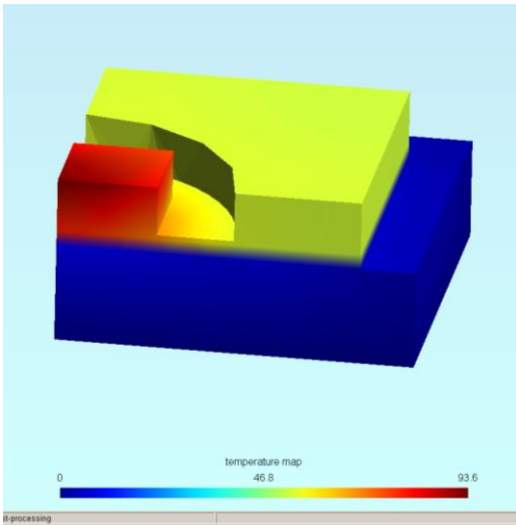


Figure 16. Temperature distribution in die carrier assembly with thick plated copper at ten Watts of power dissipation in chip.

The effect of reducing the thickness of this Kapton layer by a factor of 10, while maintaining the standard plated copper thickness, is illustrated in Figure 17. In this case, the chip temperature is reduced to 44.9°C at 10 Watts of power dissipation. The copper block is uniformly pulled down to the temperature of the alumina substrate. Figure 17 also shows significant temperature gradients in the alumina substrate in the region directly below the chip.

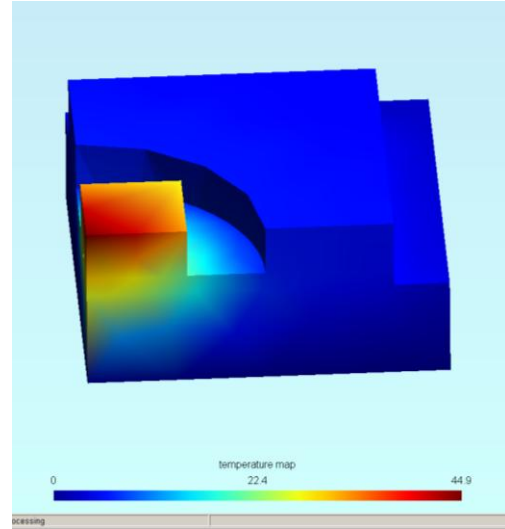


Figure 17. Temperature distribution in die carrier assembly with Kapton one-tenth of standard thickness, at ten Watts of power dissipation in chip.

The electrical resistance of the package was evaluated with the same finite element model that was used in the thermal calculations. The thermal conductivities of the materials were replaced by their electrical conductivities, with one exception. The chip was assigned the electrical conductivity of copper rather than GaAs to facilitate the analysis, to establish a known resistance. The boundary conditions on the model were as follows, the top surface of the chip was set to a zero volt potential, while a potential of one volt was applied to the upper surface of the copper block that surrounds the chip.

The finite element program calculated the voltage distribution throughout the structure. The current flow, I , through the die carrier was computed by dividing the voltage drop across the chip by its resistivity, as given by equation (1).

$$I = \frac{\Delta V_{chip}}{\rho_{Cu} h_{chip} / A_{chip}}, \quad (1)$$

Where ΔV_{chip} is the voltage drop across the chip, ρ_{Cu} is the electrical resistivity of copper, h_{chip} is the chip thickness, and A_{chip} is the cross sectional area of the chip normal to its thickness dimension. The model resistance was then obtained by dividing the voltage drop across the package by the current value obtained from equation (1). The actual package resistance is one-quarter of this model resistance, since equal currents flow through each quadrant. An example of a computed voltage distribution appears in Figure 18. This plot shows that most of the voltage drop occurs across the plated copper film, as expected.

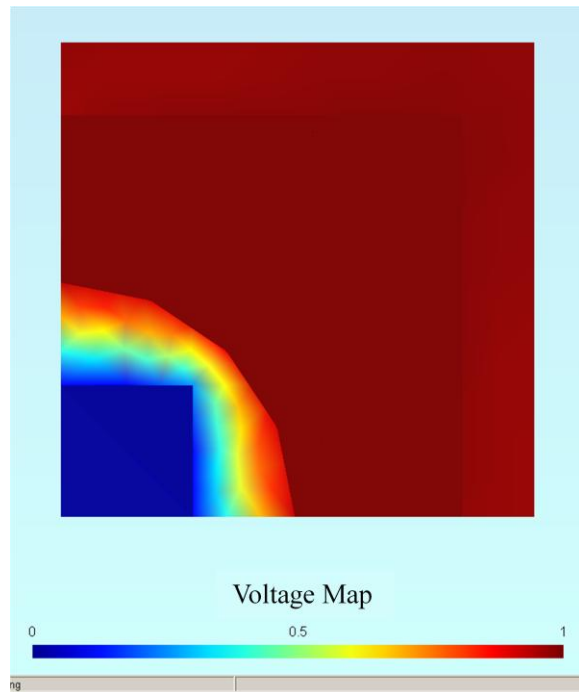


Figure 18. Voltage distribution in package with top surfaces of chip and copper block held at potentials of 0 and one volts respectively.

The sensitivity of the package resistance to the thickness of the plated copper film was investigated by varying the electrical conductivity of the film. This approach was taken, rather than changing the physical thickness of the film, because it becomes increasingly difficult to obtain a suitable mesh as the film thickness is reduced. Since the film is relatively thin compared to the rest of the structure, we do not believe that this approach introduces significant error into the calculation. The results of these calculations are summarized in Figure 19, which shows die carrier resistance plotted against conductivity of the copper film. At the nominal conductivity of copper, 60 [1/ Ohm micron], the package resistance is about one milli-Ohm. This package resistance only increases to

15 milli-Ohms if the copper is one-tenth of its nominal thickness value.

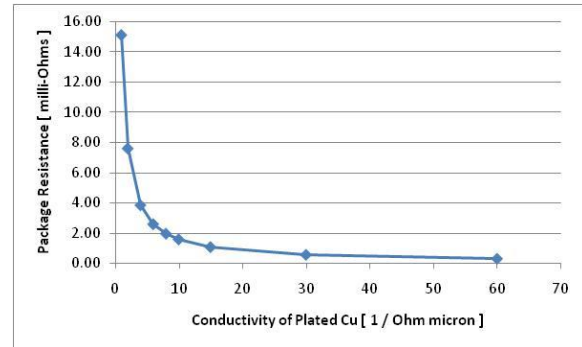


Figure 19. Dependence of package resistance on electrical conductivity of the plated copper layer. A proportional change in copper thickness, at constant electrical conductivity, would generate the same curve.

Summary

A novel chip carrier has been developed, which allows bare die GaAs devices to be incorporated into multichip modules with no changes to the assembly process. This carrier provides three important functions. First, it matches the die thickness to that of other silicon devices in the module. Second, it provides a low-impedance, electrical connection to the backside of the die. Third, the carrier provides an electrical shield around the die.

Finite element calculations indicate that the die carrier is also an effective heat spreader for devices dissipating less than ten Watts. The limitation on power dissipation is the Kapton and adhesive film that bonds the carrier to the module substrate. An all metal carrier, of similar design, but fabricated by electroforming, could be directly bonded to the substrate to achieve a substantially improved power handling capability.

Finally, even though this carrier was designed to be embedded within a multichip module, we believe that it could be useful for surface mount assemblies as well. If the die was manufactured as a flip chip device, then the assembly could be mounted on a circuit board as illustrated in Figure 20. The outline of the copper can could be modified to enhance convective cooling.

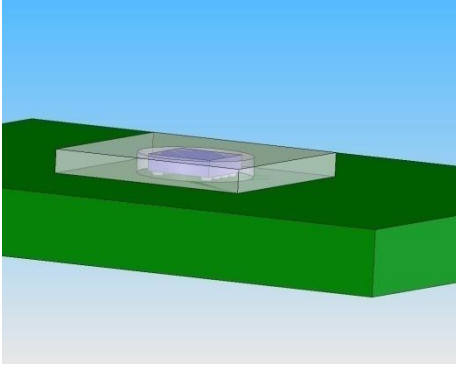


Figure 20. An illustration of the package design as a flip chip component on the surface of a circuit board

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