

High density interconnect for a high pin count optical IC

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Abstract

An interconnect solution was developed to connect a large 21x45 mm² optical IC with 2500 I/O's to its driver electronic boards by means of a flexible printed circuit with multi-level bond pads. The bond pad pitch of the IC was 72 µm pitch (2 row staggered), but the limited available volume, the extreme requirements for mechanical and thermal stability of the IC as well as some boundary conditions to guarantee the signal integrity made it necessary to develop a complex 5 level interconnect structure in combination with fine pitch aluminium wire bonding.

Out of several interconnect options a preferred architecture was chosen. To prove the feasibility of the selected solution, several prototypes were built. The multi-disciplinary approach focused on risk reduction of the assembly process. A lot of effort was put in the design of the IC carrier to achieve the thermal and mechanical stability. The wire bond geometry was carefully defined and also the flex layer build-up was optimized to achieve optimal rigidity.

1. Requirements

Initially the interconnect problem seemed relatively straightforward : realize the interconnect of a large optical IC (21x45 mm²) with 2500 I/Os to its driver electronic boards. The bond pad pitch of the IC was 72 µm arranged in 2 staggered rows.

The challenge however lay in fulfilling the additional requirements which limited the number of possible solutions.

Stability requirements

The application required an extreme positional accuracy and stability of the IC. (see Table 1). The initial XY positional accuracy of $\pm 16 \mu\text{m}$ was not considered a problem, but the short term positional stability of $0.2 \mu\text{m}$ and a die tilt stability of $< 3 \mu\text{rad}$ required the IC to be mounted on a very rigid holder. To avoid any mechanical vibration being transmitted to the IC, the electrical interconnection between the IC and the driver boards also had to function as a mechanical de-coupling. The IC itself dissipated up to 15 W so an active cooling solution was needed to keep the temperature rise of the IC below 1.5 °C at full dissipation.

Table 1 : IC Mechanical & thermal requirements

	INITIAL	SHORT TERM
X / Y position	$\pm 16 \mu\text{m}$	$\pm 0.2 \mu\text{m}$
Z position	$\pm 20 \mu\text{m}$	$\pm 0.75 \mu\text{m}$
Rx/Ry tilt	$\pm 500 \mu\text{rad}$	$\pm 3 \mu\text{rad}$
Temperature	$\Delta T < 1.5^\circ\text{C}$	$\Delta T < 1.5^\circ\text{C}$

Limited fan-out volume

Each IC had to be connected to 8 driver boards of 70x320 mm². However, in the final application a total of 14 ICs will be arranged closely together in 2 staggered rows so there was practically no space to fan out the interconnect in the XY plane and most of the interconnect had to be realized using the 3rd dimension i.e. below the IC. As a result of this, the use of a flexible printed circuit was a logical choice.

Routing restrictions

To maintain signal integrity the distance between the IC and the driver boards was limited to maximum 300 mm.

Out of the 2500 connections to be made, about 150 lines were power lines that provide various supply voltages to the IC. All these lines had to be decoupled, meaning that some 150 SMD capacitors had to be

placed somewhere on the interconnect, preferably as close as possible to the IC.

The IC also had about 60 'differential signal pairs' all concentrated in the 4 corners of the chip. To guarantee signal integrity, these lines need to run side-by-side and on the same layer of the interconnect substrate. All other signal lines required ground planes for shielding above and below the tracks.

Figure 1 shows a schematic overview of the requirements.

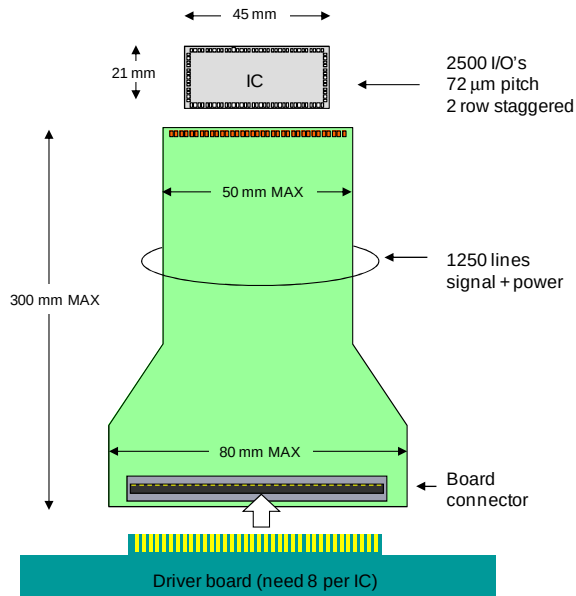


Figure 1 : Interconnect requirements

2. Interconnect options

Three basic options were considered for mounting the IC. (see Figure 2)

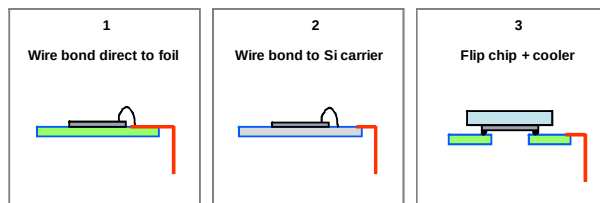


Figure 2 : Options for IC placement

In the first option, the IC is placed active side up on a stable and rigid supporting substrate that also acts as a heat spreader and cooler. The bond pads of the IC are

wire bonded directly to a flexible circuit that carries the signal to the driver boards.

In the second option – a variation of option 1 – a silicon sub-carrier is used. The IC is wire bonded to the sub-carrier first and the signals are then routed from the sub-carrier to the driver boards using a flexible pcb. This flexible pcb is reverse flip chipped or wire bonded to the sub-carrier. The use of a sub-carrier allows for some signal re-routing but also adds another interconnect level to the total chain with a potential negative effect on the total yield.

In the third option, the IC is placed as flip chip over a cavity to allow the optical function. Placement of large high pin count flip chips is challenging, but possible. To guarantee the required IC stability, in particular the die flatness, a combined support / heat spreader would have to be mounted on the back of the IC. Also this option has the additional interconnect level compared to option 1.

After weighing advantages and disadvantages, option 1 was selected as the preferred one.

To avoid any thermo-mechanical stress and deformation that would deteriorate the mechanical stability, all assembly processes had to be performed at (near) room temperature. Therefore aluminium wedge-wedge bonding was selected to connect the IC to the flex foil. This offered a low temperature process capable of pitches down to 40 μm. The connection between the flex and the driver boards was realized with 0.5 mm pitch board-to-board connectors.

3. IC holder

The holder concept

To mount the IC, a 20 mm thick SiC support was developed as IC holder. The SiC material provided the necessary dimensional stability, high stiffness, good thermal conductivity and has a thermal expansion matched to the silicon of the die. Because of the IC's flatness requirements, the use of conventional die attach adhesive or solder was not possible. Instead the IC was mounted on a pin grid structure made on the top side of the holder using powder blasting. The pins were 15 μm high and after an extra grinding step, the top of the pins defined a near perfect flat seating plane for the IC with an overall flatness < 2 μm. The IC position on the holder was fixed by epoxy adhesive dots, applied between the pins.

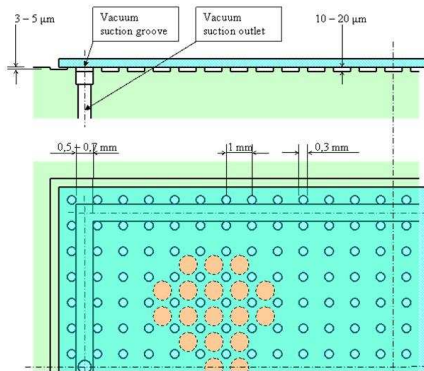


Figure 3 : Pin grid structure

The effect of various pin grid geometries on die deformation was modeled and an optimal solution between maximum support area and sufficient area for adhesion with the glue was found using $\varnothing$ 0.3 mm pins arranged in a grid with 1 mm pitch.

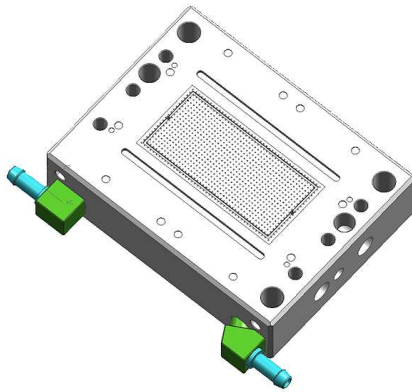


Figure 4 : IC holder

In operation the IC dissipation can reach 15W so active cooling was required to ensure that the temperature increase of the IC was kept below 1.5°C. Water cooling channels were made inside the carrier, 2mm below the pin chuck structure.

Adhesive application

Dispense jetting was used to apply small dots of adhesive between the pins of the seating plane. The dots have to be slightly higher than the pin height to ensure good contact with the IC. Initially it was found that it was not possible to make adhesive dots higher than 10 μ m due to the wetting behaviour of the powder blasted SiC surface. Fumed Silica filler particles were added to the adhesive to change its rheology. No negative effect on either E-modulus or shrinkage was measured. By adding 6 wt% of filler it was possible to make adhesive dots higher than 10 μ m.

Thermal shrinkage and potential build-up of thermo-mechanical stress was avoided by curing at room temperature, but the effect of cure shrinkage could not be avoided completely. Balancing the E-modulus and the cure shrinkage of the adhesive material resulted in a maximum deviation of 4 nm of the IC between the pins.

IC placement

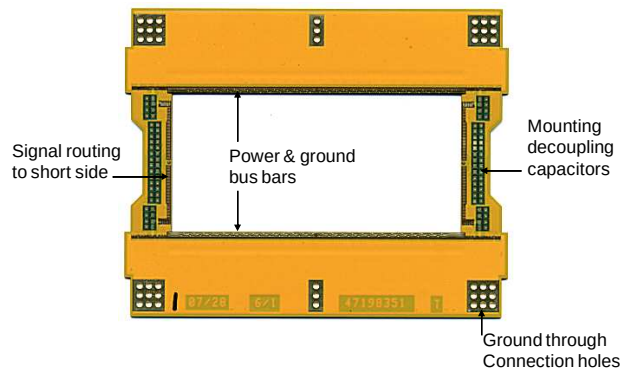
A semi-automatic die placer was used to align and place the IC on the pin chuck. The IC backside was in direct contact with the studs and vacuum applied through a groove in the holder was used to pull the IC flat against the pins. Vacuum (at 0.5 bar) was maintained during the complete curing cycle. The effect of the vacuum on the die flatness was measured to be less than 0.1 nm.

4. Interconnection

Decoupling and grounding board

Because of the high wiring density and the limited available space, a separate board was designed to fulfill the decoupling and grounding requirements (See Figure 5). The board had an opening in the middle and was placed around the IC. Decoupling 0402 capacitors were reflow soldered on top and bottom side of this board. A 3 lane bus bar on the inner side allowed short wire bond connection for power and ground to the IC. On the short side of the board there were bond pads to accept signals and control lines of the IC and route them to the interconnection flex.

The board was an 8 metal layer polyimide 'flex' with total thickness of 600 μ m. Only 4 layers were required for routing and grounding. However, to optimize wire bond looping, 4 extra layers were added to increase the total thickness of the board and bring it



almost at the same level as the bond pads on the IC.

Figure 5 : Decoupling and grounding board

In the actual assembly, the IC was placed on the holder first and the decoupling and grounding board was placed over it. Because all processes had to be done at room temperature, a hybrid bonding solution was developed to mount the decoupling and grounding board on the holder. A double side adhesive tape was applied on the bottom side of the board. The tape was selected for best creep and peel performance and ensured the initial adhesion of the board to the IC holder. The 100 μm thick tape was pre-cut in a specific pattern that allowed for several open “channels” (see *Figure 6*).

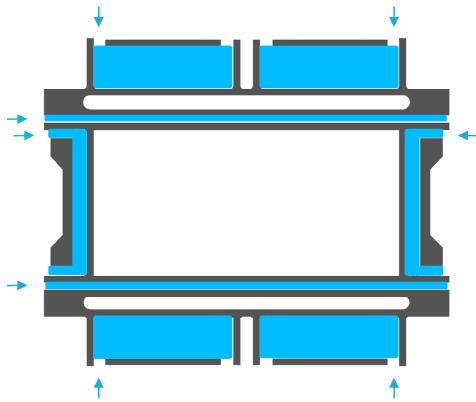


Figure 6 : Bottom adhesive pattern
(gray=adhesive tape, blue=liquid adhesive)

A dedicated tool with visual alignment was used to place the board on the IC holder, with the IC fitting exactly in the central opening. The spacing between the board and the IC being only a few hundred μm .

Because the adhesive tape has instant adhesion, the position of the board on the holder was fixed immediately after placement. The assembly could now be taken out of the assembly tool and transferred to another tool where a low viscosity epoxy adhesive was allowed to flow capillary and fill the open channels between the board and the holder. In this way, the adhesive tape secured the initial positional accuracy until the liquid adhesive was fully cured. At the same time the tape also avoided possible bleeding of the liquid epoxy and possible adhesive contamination on the IC or the board.

Interconnection flex foil

Routing 1250 lines from each side of the IC within a width of 50 mm (see Figure 1), would require 20 μm lines and spaces (in 1 layer) on the flex foil. This pitch can be manufactured by most high end flex foil vendors for small board sizes, but for trace lengths up to 300 mm a more relaxed pitch is required to get an acceptable yield. Therefore a 4 level flex foil was

developed. This allowed us to relax the track pitch to about 150 μm but also made routing easier and get a higher flex foil yield.

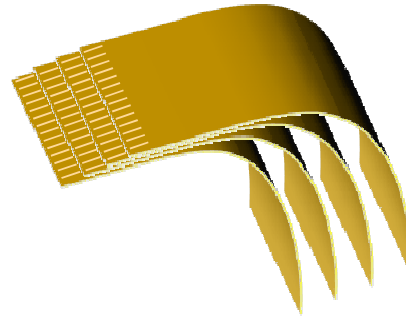


Figure 7 : 4 level interconnection flex foil concept

The interconnection flex foil consisted of 4 similar levels or “packages” (see *Figure 7*). Each package consisted of a 3 metal layer multilayer with a signal layer sandwiched between 2 ground layers. At one end of each package the signal layer was made accessible to create about 300 bond pads that connected to the IC. At the other end of the package two 240 pin board-to-board connectors (0.5 mm pitch) were mounted to connect to the driver boards.

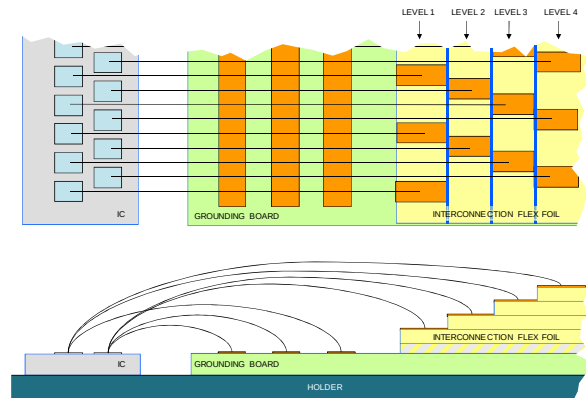


Figure 8 : Interconnect

At the bond pads end the 4 packages were shifted over 500 μm to create a staircase-like structure with bond pads on 4 levels. The 4 packages were bonded together only at the end of the bond pads while the remainder was kept separate so that each package could be routed easily to its corresponding controller board.

The most challenging issue was the staircase structure for the bond pads. Special pressing techniques were used to ensure the flatness of the bonding pads, to keep the alignment of the 12 metal

layers within spec and to avoid glue outflow between the packages from contaminating the bond pad area.

On each of the 4 levels, 500 μm of the Cu track was exposed, but only 215 μm could be used as bond pad area. A no-bond zone of 15 μm at the 'tip' was excluded because of potential contamination from the foil cutting process. Another 270 μm zone was defined at the other end of the pad for bond tool clearance and for glue outflow from the flex foil pressing process.

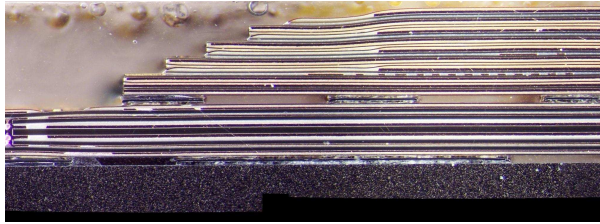


Figure 9 : Microsection of flex foil and grounding board mounted on the holder

Because the wire bonding pads were located at the extreme end of the foil, special care was taken to ensure sufficient inherent stiffness of the lower package in case the interconnect foil would not be perfectly bonded to the underlying grounding board. Therefore an additional 150 μm stiffener was added under the lower package.

Separate alignment structures were added for each level to ensure the required inter-layer alignment accuracy.

Mounting the interconnection flex foil

Before assembly of the interconnection flex foil on top of the grounding board, the 0.5 mm pitch connectors were reflow soldered and the foils were pre-bent into their final shape.

The assembly itself was done using a dedicated placement tool (see Figure 10). The wire bond pads on the flex foil were visually aligned to the wire bond pads on the IC. For the assembly the same process was used as for the decoupling and grounding board i.e. a combination of adhesive tape and room temperature cured liquid epoxy.

To achieve a low resistance ground connection over the entire electrical path between the driver boards and the IC, grounding vias in both the grounding board and the interconnection flex foil were connected by means of solder connections

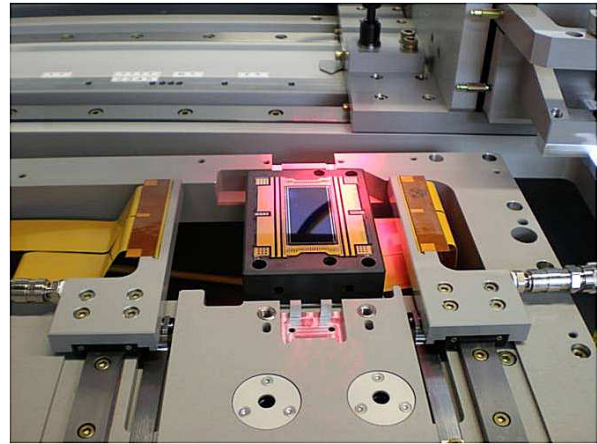


Figure 10 : Mounting the flex foils on the grounding board

5. Wire bonding

Considerable effort was already put into the design of the flex foil and the decoupling board to ensure maximum stability and alignment accuracy of the wire bond pads. The effort of wire bonding was focused on solving the geometric constraints.

Wire sway

Wire bonding was done on a standard automatic Al wedge-wedge wire bonder using 25 μm wire. Using thinner wire would have reduced the wire bond footprint but it would also increase the risk for wire sway and wire shorts. The longest wire loops in our assembly were about 4 mm which is longer than the rule of thumb limit of 100x the wire diameter. Therefore a wire sway test was set up to assess the risks of shorts between wire loops. Test samples with loop lengths between 3 and 7 mm were made and subjected to a 10g acceleration test using 10 frequency sweeps between 10 and 150 Hz for a test duration of 40 min. These tests showed that up to 5 mm loop lengths could be achieved without risk of shorts between the wires.

Wire bond geometry

The overall bonding geometry is illustrated in Figure 8 and Figure 11. In the horizontal plane, wire bonding goes from 2 rows on the IC to 7 rows on the interconnect flex. In the Z direction bonding goes from IC level to 5 different levels, 1 on the grounding board and 4 on the interconnect flex.

Bonding direction was from IC to flex circuit for all wires except for some wires between the grounding board and the interconnection flex. In the bonding sequence first the connections from the IC to the three bus bars were made, then from the IC to the interconnect flex, the lower levels first.

The bond tool was a fine pitch wedge with 45° wire feed angle. The heel of the bond tool was slightly chamfered to avoid contacting the wires from the first rows on the bus bars.

The hybrid flex foil mounting concept proved to be very reliable. Only 2 out of 20 samples showed problems with bondability, both caused by excessive warp of the board

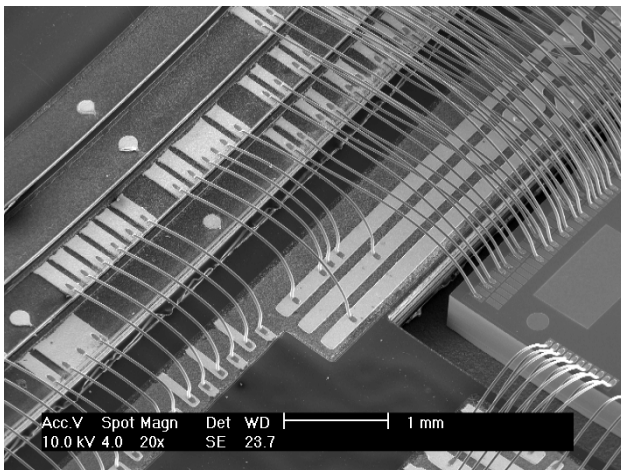


Figure 11 : Wire bond geometry

6. Conclusion

In total 12 assemblies were build during the product and process development phase. After optimization 8 functional pre-prototypes of the complete assembly (*Figure 12*) were built to prove the feasibility.



Figure 12 : Complete assembly

7. Acknowledgement

This project could not have been realized without the collective dedication of all team members from the various technical disciplines of Process Technology, Production Systems and Mechatronics from Philips Applied Technologies. Also the close cooperation with our material vendors is highly appreciated.