

LTCC Materials, Guidelines, and CAM and Test Output Integration for Electronic Design Automation (EDA)

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ABSTRACT

As ceramic industries move into the future, the need for schematic capture, checking, embedded components and elements, 3D checking and new materials integration will continue to grow in the quest for smaller, more complex, and more powerful designs, as well as new manufacturing and assembly processes. To support quick turn, back-to-back design, layout and manufacturing, an LTCC design engineer needs every possible advantage to complete the design quickly without design and manufacturing problems that cause delays.

With the focus on new materials that enable smaller traces / spaces and new processes, it is necessary to integrate these material specifications and process guidelines into the design process and layout software. In order to popularize the use of LTCC technology and rapidly expand production volume, the industry needs to provide materials and promote tools, which reduce time to market for new products.

While both materials and EDA software for the LTCC market have advanced, there has been a disconnect between the parameters designers perceive as acceptable and what manufacturers can produce. It would be ideal for the LTCC layout engineer to select specific materials and have the design guidelines and processes carry forward seamlessly into manufacturing. The result is that the layout engineer would be able to produce CAD files, CAM files and Test files that have been designed for the specific materials and manufacturing technologies, thereby insuring compatibility with the manufacturing processes (Design for Manufacture).

The purpose of this paper is to define what is required of the LTCC industry for the LTCC designers and manufacturers to be truly efficient.

(Keywords: LTCC, Materials, CAM, Design, Guidelines, Test, Integration)

Introduction

The Low Temperature Co-fired Ceramic (LTCC) requirements for schematic capture, checking, embedded components and elements, cavity design, resistor design, CAM output, etc. will continue to grow in the continuing quest for smaller, more complex and more powerful designs, as well as new manufacturing and assembly processes. These required features of LTCC design are needed to dramatically reduce or eliminate the problems experienced in current designs and help fit the design within the required real estate of the substrate/board outline.

Technology

LTCC multi-chip modules are designs where multiple bare die are connected either by wire or direct contact. This technology utilizes dielectric layers and conductive pastes that are baked or fired simultaneously to produce a rigid substrate. The dielectric layers are punched for vias and cavities, and metallization is applied to the dielectric layers using a thick film, screen-printing process. Additional conductive pastes can be applied after the initial firing process.

Materials

The use of LTCC materials within a design system should include a library of dielectric and paste materials that a user can select from. The library of materials should be customizable by the user so that materials and parameters can be added or deleted as needed. Each material listing should include all pertinent parameters of the material for use in analysis, simulation, embedded element/resistor creation and manufacturing considerations. The parameters can be categorized as Electrical, Mechanical and Chemical.

1. Electrical parameters:

a. Dielectric:

- i. Breakdown voltage
- i. Dielectric constant
- ii. Loss tangent
- iii. Insulation resistance

b. Conductive paste:

- i. Fired resistivity

c. Resistive paste:

- i. Sheet resistance (ohms / square)
- ii. Shipping tolerance

- iii. Change in resistance per re-fire
- iv. Thermal coefficient of resistance
- v. ESD
- vi. Quantech noise
- vii. STOL

d. Capacitive dielectric:

- i. Breakdown voltage
- ii. Dielectric constant
- iii. Thermal coefficient of capacitance
- iv. Dissipation factor
- v. Insulation resistance

2. Mechanical parameters:

a. Dielectric:

- i. Shrinkage in the X, Y and Z-axis
- ii. Thickness (unfired and/or fired)
- iii. Thermal coefficient of expansion (TCE)
- iv. Density
- v. Camber
- vi. Surface roughness
- vii. Thermal conductivity
- viii. Flexural strength (4-point bend)
- ix. Young's modulus

b. Conductive paste:

- i. Fired line resolution
- ii. Thickness (dried and fired)
- iii. Coverage
- iv. Viscosity
- v. Wire bond performance
- vi. Via diameter resolution

c. Resistive paste:

- i. Viscosity
- ii. Coverage
- iii. Thickness (dried to fired)

d. Capacitive dielectric parameters:

- i. Viscosity
- ii. Coverage
- iii. Thickness (dried to fired)

3. Chemical parameters for all materials should include recoverable elements for recycling or consideration of environmental impact.

Within the design system a material stackup feature should be available that is tied to the material library for ease of material selection. The selection of each material should automatically load the parameters of the material into the stackup table.

Material Stackup

Material stackup within the design system should be tied to the materials library. As the stackup table is created, the properties of the material are loaded into the table automatically. This data can then be sent to test output integration with simulation software.

Circuit Analysis and Simulation

Circuit analysis and simulation should include an Advanced Programming Interface (API) allowing the creation of intelligent connections to many of the popular analysis systems for:

1. Parasitic Extraction (RLC)
2. Electromagnetic (EM) analysis
3. Circuit simulation
4. Linear Simulation
5. Signal Integrity

Where applicable the design system should allow the return of simulated changes to the design for accurate and rapid updates.

Guidelines

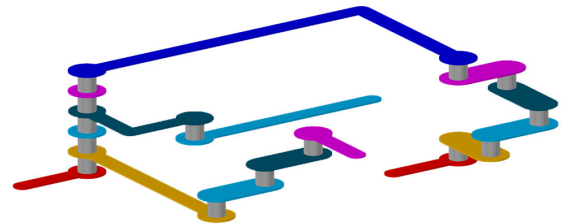
The guidelines for designing a LTCC circuit should be customizable by the user based on the material manufacturer's recommendations and the fabrication facility's process requirements. Global and level guideline settings should include:

1. Minimum spacing for trace to:
 - a. Trace
 - b. Terminal
 - c. Hole
 - d. Via
 - e. Cavity
 - f. Area
2. Minimum spacing for via to:
 - a. Area
 - b. Terminal
 - c. Via
3. Minimum size for:
 - a. Trace width
 - b. Annular ring

Additional consideration should be given to the availability to assign custom entities within the system and have those entities recognize the constraints of standard system entities.

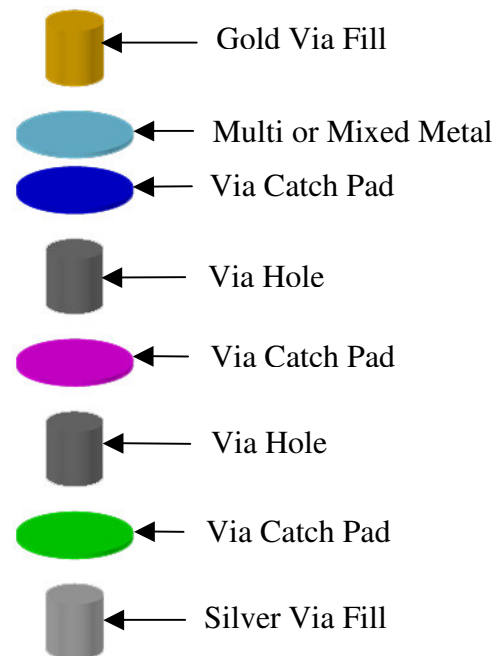
Via Creation

LTCC interconnect technology should be available through a flexible via creation process, which would include support for blind/buried construction for all fired or build-up technologies. Combinations of blind/buried vias will be created as blocks to form stair-stepped vias, tunnel vias (similar to through hole), straight vias, and spiral vias.



3-D stackup of various hybrid technology vias

Via pads (catch pads) should be resizable and removable by level. Support for the addition of via fill and mixed-metal or multi-metal printings for vias should be available.



3-D stackup of various hybrid via entities

Routing

The routing systems will feature online Design Rule Checking (DRC), any angle direction with settable snaps, gridless capability, and object snugging.

Some of the routing systems should support concurrent routing with parasitic extraction readouts while routing. Once the user specifies the material stackup and properties, the routing functions will display the electrical calculations for resistance, inductance, and capacitance during routing.

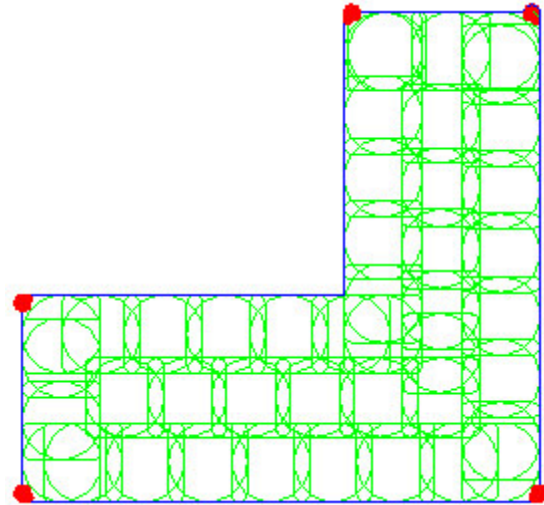
Cavities

With the use of die in cavity, an LTCC design system should allow for the design of cavities parametrically and graphically. The parametric creation of cavities should allow for:

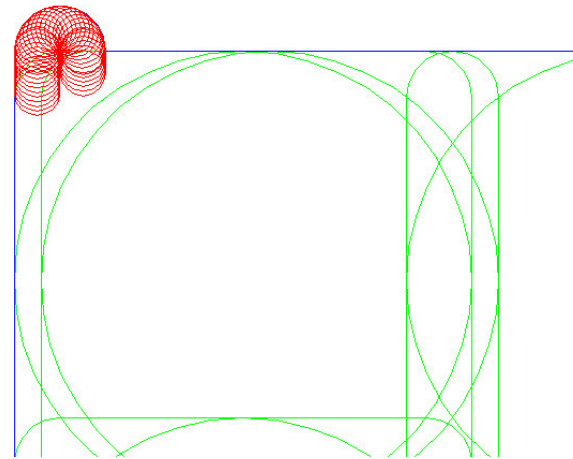
1. Number of levels deep from either side of the substrate.
2. Multiple cavity offsets from the defined base cavity for stepped cavity creation.
3. Assignment of keep out perimeters for vias and traces.

In addition to cavity creation, the fabrication of the cavities needs to be considered in terms of automated punch machine interface. A cavity-nibbling tool would be required and should include:

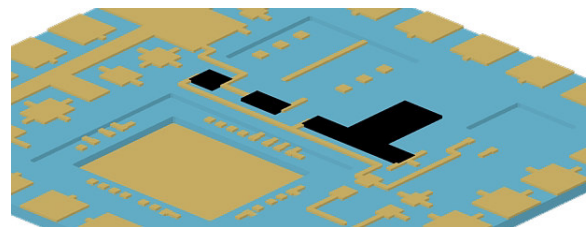
1. The ability for the designer to setup punch tool carousels within the software.
 - a. Assignment of both design to and map to sizes.
 - b. Tool location assignment.
 - c. Tool shape definition, including radius.
 - d. Multiple carousels
2. The separation of punch functions such as nibbles and rubs. Nibbles being the punches along the edge of the cavity and rubs being the large scrub areas in the middle of the cavity.
3. Tool overlap assignment.
4. The ability to create and erase all nibbles and rubs globally, by cavity, by segment or manually.
5. The ability to add corner relief radii.



Cavity nibbles and rubs example



Close up of cavity nibbles (red) and rubs (green)

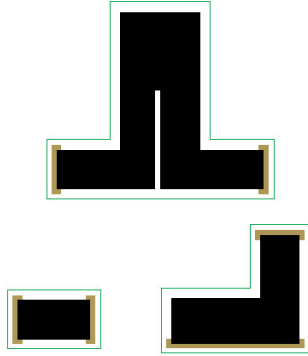


Example of 3D hybrid cavities with circuitry

Printed Resistors

Printed resistors are created with resistive material in specific length/width ratios, eliminating the bulk or size of traditional resistor packages. Specific functions and libraries within the design software should be available and would include:

1. Automatic size calculations based on design rules, and user defined paste characteristics (resistance, aspect ratio, wattage, etc.).
2. Rectangular shaped, Top Hat shaped, Right Angle or L-shaped resistors.



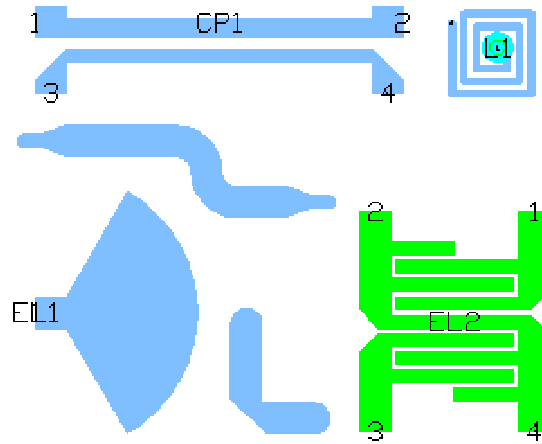
Printed resistor shapes with overglaze outline

3. Process tolerance calculations and automatic tables for processing, such as after firing and trim values and tolerances.
4. Built-in overglaze and keep-outs for paste areas.
5. Serpentine resistors with automatic resistance tuning.

Printed Elements

Like printed resistors, these components are printed or etched, with the difference being that these components are formed with conductive material rather than resistive material.

These elements are created with polygon boundaries, so any shape is possible. All elements would have a dual electrical property, meaning that the elements would be compatible with Layout vs. Schematic (LVS) checks, so that the system does not see a short circuit through the component's circuitry. However, the system should still be able to treat the integral circuitry as intelligent metal, so that DRC checks are still possible. This will provide an intelligent Electronic Design Automation (EDA) system for element components where you can have both electrical and mechanical checking.

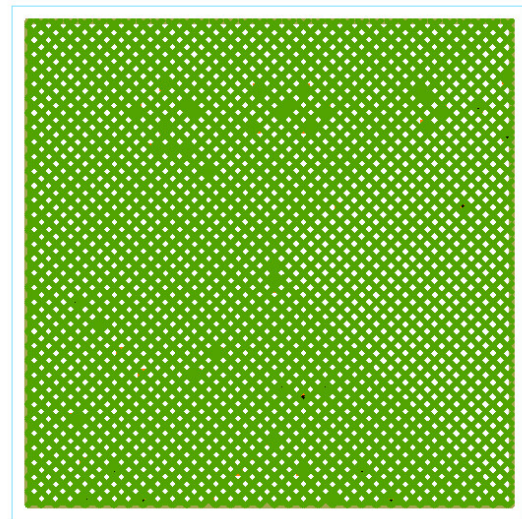


Example of elements

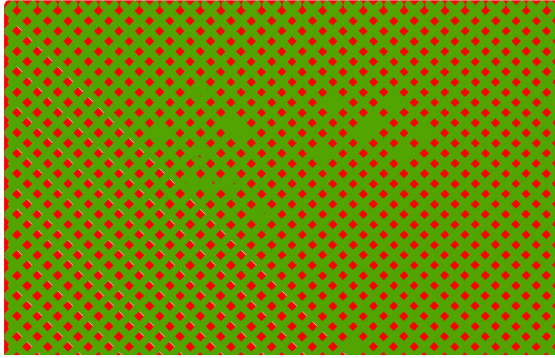
Planes – Ground and Power

Plane creation should be fast and easy with the following plane types being supported:

1. Positive Fill Planes - This is the industry standard method for plane creation, by using a specific fill width to “paint” or “flood” the ground plane. This type of ground plane is used for creating cross-hatched or gridded planes. The ability to offset subsequent gridded planes should be available.

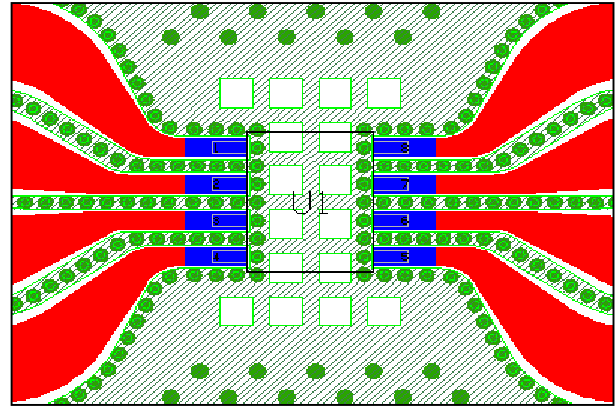


Example of gridded plane with pin hole fills



Example of offset gridded planes

2. **Negative Fill Planes** - This plane type is more efficient than the positive fill method, because only the areas that will be conductor free are painted. However, this is only recommended for use with full planes, or planes where not much routing exists.
3. **Positive Boundary Planes** - An advanced plane that is modeled or enclosed by 0-width polygons, and fill pattern that displays the plane as a hatched area. This newer method allows for very fine details and accurate control over sharp corners. The method is highly efficient for both manufacturing data, as well as for the working database.
4. **Mixed Plane/Routing and Mixed Negative Planes** - All of the positive and negative methods previously mentioned should be compatible with planes that also contain routing. Special commands for negative and mixed negative planes would allow for a highly automated process for definition of ground splits and relief/thermal creation.
5. **Coplanar ground shields** - The creation of ground shields around any trace or object with other commands for creating additional via-based grounding around or on the ground shield.
6. **Automatic Via Peppering** - The capability of creating the ultimate in additional ground plane connections, by peppering every available area of the board with vias, while maintaining DRC settings.



Example of plane and ground shield with peppered vias

The customized creation of metal patterns on the design to control warpage and/or to equalize the metal distribution on any layer should be achieved automatically with standard metal shapes/sizes, or with definition of custom metal patterns.

Additional Design System Considerations

An ideal LTCC design system should also include and support:

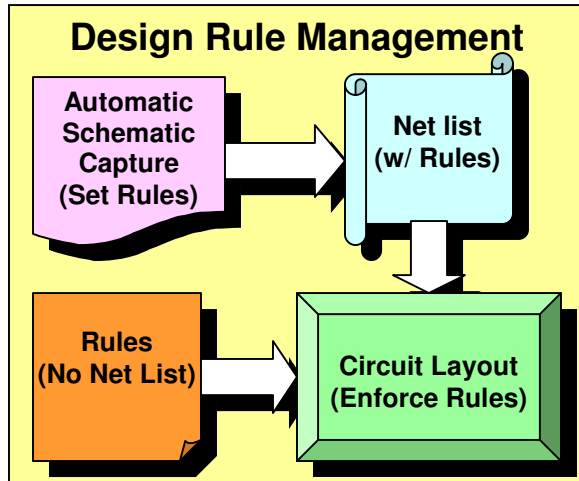
1. An unlimited design environment for the usage of various units of measure, such as Inch, Mils, MM, CM, and Microns. There should be no layer, pin, entity, or unit and angle resolution limits.
2. A flexible system architecture, which includes automatic options for dimensioning and tolerancing, and automatic or semi-automatic fabrication and assembly drawings.
3. Hierarchical construction/architecture for everything, including schematics, symbol and component blocks, design rules, materials, etc. This affords a highly efficient database, for the best performance, ease-of-use, parameter-based programs, etc.

Design Rule Checks (DRC)

Design Rule Checking should be supported through net lists. If the rules are defined in the schematic, they should be transferable to the layout through the net list. Then the program can

automatically use the correct settings for a class of nets, for individual nets, etc.

The program should support global rules, layer rules, region rules, class rules, and individual net rules. In addition, special rules can be set between any of these types, such as class-class and layer-layer.



Test Output Integration

Test output integration should include an interface allowing the output of intelligent data to testing equipment such as a flying probe tester. These interfaces could come in the form of an IPC-D-356 file or an ODB++ file.

CAM Output

CAM output capabilities should include features for setting either the individual layers or the complete batch of layers comprising the output file, whether Gerber or drill/punch format. These features to consider include:

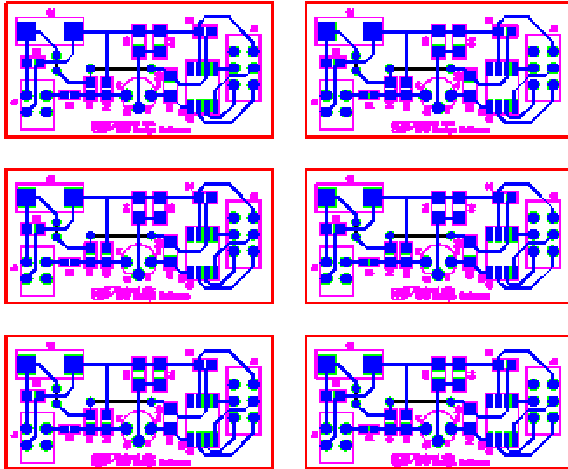
1. Panelization - Layers can be panelized individually or globally.
2. Mirroring – Layers can be mirrored individually, in a batch, or globally.
3. Rotation – Layers can be rotated in a batch.
4. Scaling - Layers can be scaled individually, in a batch, or globally, in the X or Y scale (each direction can be scaled independently).

5. Offsetting – Entities can be offset individually or globally.
6. 0,0 redefinition – Redirecting of the 0,0 point from what was used in the design to what is needed in the output.
7. Optimization – Mainly for drill/punch data, this would redefine the path of the tools by various methods with minimization of length being the most desirable.
8. NC Drill/NC Route/NC Punch - Support for direct input to drill/route/punch machines.
9. Epoxy dispense output – Support for direct input to automatic epoxy dispensing machines.
10. Component placement data – Support for direct input to automatic component placement (pick and place) machines.
11. Wirebond machine data – Support for direct input to automated wirebonding machines.

Artwork Generation

A well rounded set of utilities for artwork generation would be very desirable and would include:

1. Standard support for RS274D and RS274X Gerber.
2. GDSII support for input and output of GDS files.
3. True Type fonts fully supported, either through direct conversion, automatic font substitution, or through pre-processors to optimize the data before conversion.
4. True Arc support, either through direct conversion, or through a vectorization process.
5. Polygon Fill support to convert all custom polygons. In addition, the system should differentiate between “painted” polygons and “scratched” polygons, so that voids are correctly converted.



Example of panelized artwork

Summary

In conclusion, the LTCC design industry has suffered from a lack of true design systems tailored to the unique requirements of advanced LTCC technologies, resulting in long design cycles, slow time-to-market, and lower yields. LTCC design systems must be technology-specific to automate the design and reduce design time. These systems will allow engineers and designers to take advantage of the automation technologies that are present in other design disciplines and yet have long eluded the LTCC design environment.

References:

All information provided by CAD Design Software and DuPont Electronic Technologies.

For more information, please contact:

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