

Estimation of Interconnect Models of SIP (System-in-Package) and POP (Package-on-Package) for IC-Package Co-Analysis and Optimization

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Abstract

In the rapidly booming digital consumer electronic market, System-in-Package (SIP) technology is a powerful means to achieving miniaturizing and manufacturing of advanced high-performance systems. To minimize the number of SIP design iterations due to SSN, jitter, EMI, crosstalk noise, we suggest a new estimation technique that can predict the interconnect parasitics of a 3D stacked package (including POP and SIP) in the early stage of chip design. The approach rests upon the weighting factor (W) reflecting the irregular routability of a substrate design. The weighting factor is carefully characterized by the function of the routing angle and the number of the crossover between logical nets. The technique is demonstrated by application to 3D stacked package design such as POP and SIP. The exact models of each signal net used for post simulation are well bounded between the maximum and the minimum estimation values obtained by the approach. The proposed estimation algorithm shows excellent results compared to the exact models for POP package as well as SIP package. It is expected that chip-package co-analysis and optimization can be well considered by using the presented estimation algorithm.

1. Introduction

In modern mobile hand-held phones, many functions and services are integrated in one chip. Since the small form factor chip set solution corresponding to wireless service is strongly required in ultra-thin small form-factor mobile phone, System-in-Package (SIP) and Package-on-Package (POP) have become promising and powerful solutions. However, as the number of functions integrated in SIP increases and package size decreases, noise margins such as simultaneous switching noise (SSN), crosstalk and jitter also decrease. Moreover, such SIP based structures considerably increase the system complexity thereby giving rise to new signal and power integrity problems [1]. In SIP and POP packages, one of the critical bottlenecks preventing the implementation of the high speed mixed system, which operates up to multi-GHz, is the isolation

of the power and ground voltage fluctuation noise due to the inductance of the package and of the board [2], [3]. Particularly, SSN results in serious performance degradation and system function failures because it reduces the noise margin and increases in the jitter, signal distortion and electromagnetic interference (EMI). Furthermore, unfortunately, the time-to-market has drastically reduced. In order to avoid making timing consuming design iterations in the later design stages and ensure quality manufacturing at lower cost, the circuit designers must take the SIP/POP package parasitics effects into account at the early stage of circuit design [4]. For a robust device design, Pre-SSN and IR drop simulations concerned with the package effects are mandatory in multi-GHz bandwidth interconnect systems. Consequently, a more accurate Pre-SSN and IR drop simulation of a device is necessary to consider the reasonable package effects, especially for a 3D stacked POP/SIP package, as well as the set board conditions [5].

The advantage of a chip-package-board co-design is that the performance of the IC and the noise margin of a 3D stacked package can be optimized together, to obtain the best results about system level design and optimization. However, most chip and package designers often employ an overestimating package model under worst-case scenarios, which may not consider the noise margins of 3D stacked packages because such a model has difficulty in exactly estimating the package model, especially POP and SIP, in the early stage of package design. Without consideration of accurate parasitic effects of SIP and POP, the timing budget as well as the noise margin (including a skew, crosstalk, IR drop and SSN) cannot be evaluated properly during a transient simulation of today's high-performance or next generation VLSI circuits. Also, with ever decreasing design cycles, chip and package designers must be given a proper solution to quickly and efficiently estimate the noise margin of the 3D stacked package. Especially, with respect to SSN noise and signal integrity, it is clear that the estimation of the preliminary package model can help to prevent painful design modifications in the later stages of design, and ensure quality manufacturing at lower cost. However, the parasitic effects of the package such as SIP, POP are

usually unknown until the final stage of the design process. Therefore, it is sometimes unavoidable to revise the design due to the signal and power integrity problems are discovered in the later stage of SIP/POP design. In order to solve these difficulties, we propose a new methodology, which can estimate the interconnect models of the 3D stacked SIP/POP packages without a post-simulation process and provide a good solution for a chip-package co-design. With such interconnect models, chip and package designers can execute the transient simulations and provide guidelines for the selection of the optimal package type in the early stage of SIP/POP package designs.

2. The Proposed Methodology

In this section, the basic concept of the proposed algorithm that can estimate the interconnect circuit model of SIP and POP package in the early stage of package design (before routing on PCB) is presented. It is based on the segmentation method, which divides 3D stacked package into unrouted PCBs and other interconnects such as bonding wire and solder ball, extracts the estimated circuit models of each part, and integrates them into a unified lumped circuit model by using the ABCD parameters. The parasitic model of each part is computed by a scalable model extracted from the interconnect length-dependent empirical formula obtained from a 2.5D field solver. This paper mainly focuses on the estimation of electrical models of unrouted PCB traces in the early stage of design by the use of the weighting factor (W) reflecting the irregular routability on 3D stacked package design.

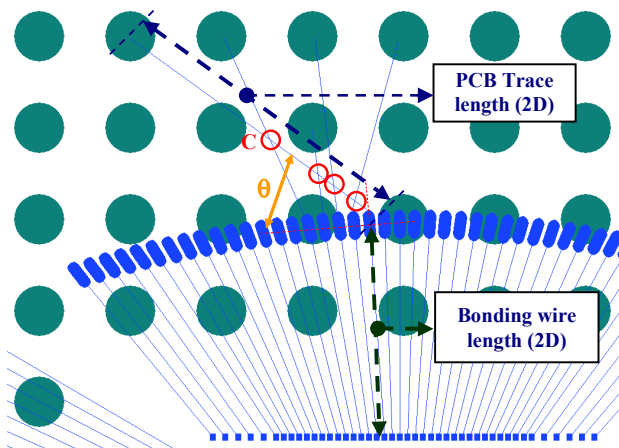


Fig. 1. Parameters of the weighting factor (for example, crossover (C): 4, routing angle (θ): 50°)

Since the weighting factor greatly influences the accuracy of the approach, it is carefully characterized by

critical PCB design parameters such as the routing angle (θ) and the number of the crossover (C) between logical nets, which depend on the substrate PCB of POP and SIP.

The weighting factor as a critical factor of the estimation technique can be represented as the function of the routing angle (θ) and the number of the crossover (C). The weighting factor of this method is defined as follows [6]:

$$W = \sqrt{\frac{a \times (b + |\sin(\theta)|) + (c \times C + d)}{e}} \times \log \left(f \times \left(\frac{(g \times C + h)^{1-|\sin \theta|}}{|\sin(\theta) + j|} \right) \right) + k$$

where

θ = routing angle [radian], C = number of crossover among nets
 $a, b, c, d, e, f, g, h, i, j, k$ = constant

The proposed algorithm can be applied to Single-Chip-Package (SCP) as well as to System-in-Package (SIP) because the structure of a substrate PCB is the same for types, except for the wirebond structure. However, to estimate a model of a POP package, the proposed algorithm is carried out for top ball and bottom ball, respectively.

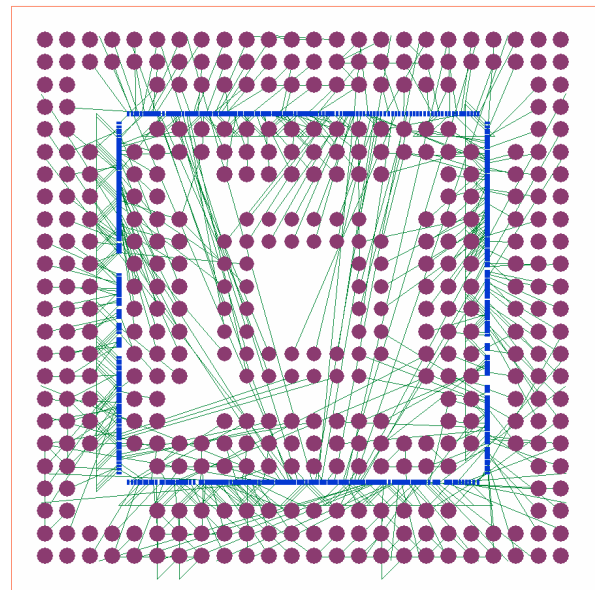


Fig. 2. Rats information for the bottom ball configuration of Package-on-Package (POP) (416 ball-FBGA-13mm x 13mm).

Note that rats represent the logical connection information between the ball and diepad in this paper.

3. Result and Analysis

In order to demonstrate the accuracy of the algorithm to estimate and evaluate 3D stacked package cases, we

consider two types of 3D package designs, the POP and SIP.

A. Estimation of Model Boundary of POP (Package-on-Package)

To verify the ability of the algorithm to estimate the POP type, we carried out an experiment by using a POP package design (416 ball-FBGA-13mm x 13mm) for the mobile application. The logical connection information between the bottom ball and the diepad provided in Fig. 2 can be obtained from the crossover and angle data of each bottom ball.

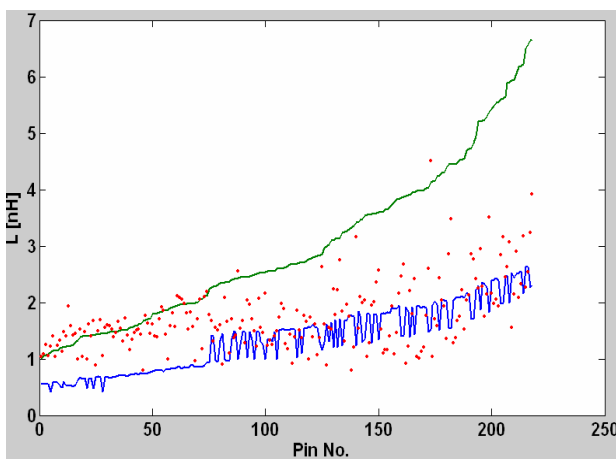


Fig. 3. Comparison of the inductance for post-simulation and estimation (worst & best case) for each signal pin of the bottom ball configuration of Package-on-Package design (416 ball-FBGA-13mm x 13mm). Green and blue solid lines represent the maximum and minimum boundaries of the inductance, respectively, and the red dotted line indicates the exact inductance extracted from the 2.5D field solver.

After reflecting an abnormality on a PCB design by the weighting factor, a parasitic model of a PCB substrate can be obtained in a similar way to the bonding wire case (R_{sub} , L_{sub} , C_{sub} = the empirical formula $\times$ trace 2D length $\times$ the weighting factor). The models of the parts (bonding wire and substrate) are integrated into a final preliminary package model based on the ABCD matrix [6]. In order to compare the boundary estimation accuracy of the proposed method, the overall experimental results for the signal pins of the POP package (416 ball-FBGA-13mm x 13mm) are evaluated and plotted in Fig. 3. As shown in Fig. 3, the exact model of each signal net used for post simulation is mostly bounded between the maximum and the minimum estimation model. Several nets out of the boundaries of the POP model are approximately under maximum 0.74 [nH].

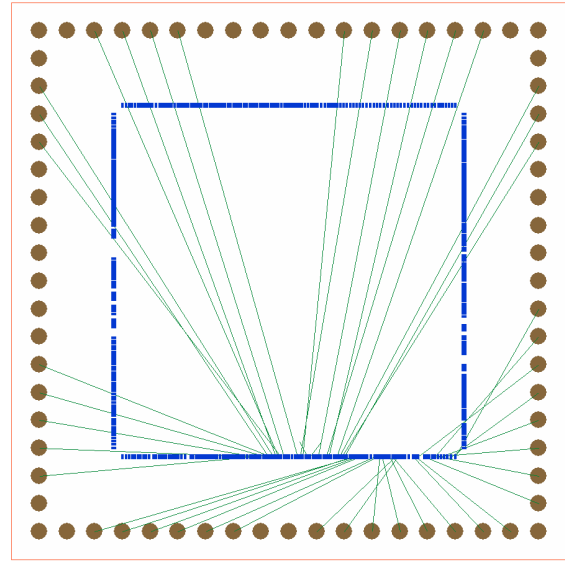


Fig. 4. Rats information for the top ball configuration of Package-on-Package (416 ball-FBGA-13mm x 13mm)

For the case of the top ball of the POP package as described in Fig.4, the exact model of each pin is bounded well between the maximum and the minimum estimation values, as shown in Fig. 5. Thus, for a POP package, the errors in the proposed method converge within a reliability range on the average of 5% to the maximum boundary.

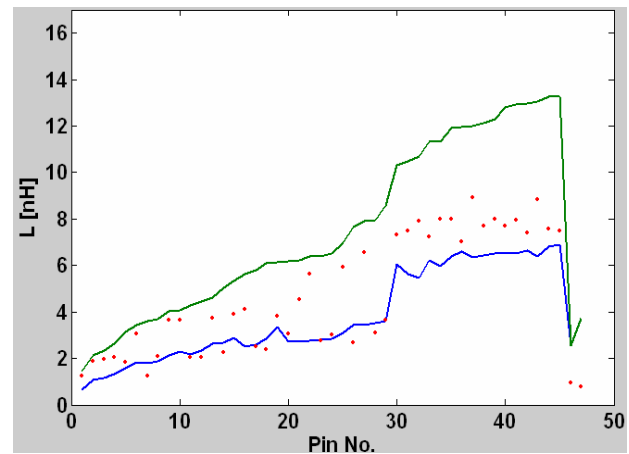


Fig. 5. Comparison of the inductance for post-simulation and estimation (worst & best case) for each signal pin of the top ball configuration of Package-on-Package (416 ball-FBGA-13mm x 13mm). Green and blue solid line represents the maximum and minimum boundary of the inductance and the red dotted line indicates the exact inductance extracted from 2.5D field solver.

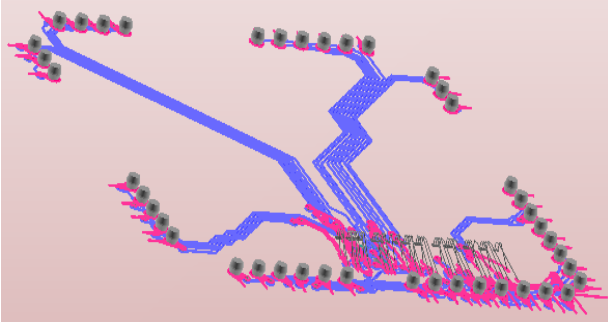


Fig. 6. DDR2 nets connected to the top ball of Package-on-Package (POP)

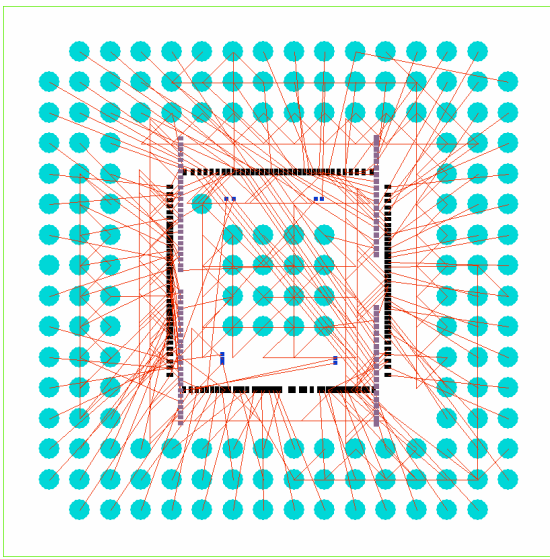


Fig. 7. Rats information of System-in-Package (SIP) with 3 chips (169 ball-FBGA-09mm x 09mm)

The real design of DDR2 nets connected to the top ball of a Package-on-Package (POP) is shown in Fig. 6. As described in Fig. 4, the number of the crossovers between DDR2 nets connected to the top package is under the maximum of 4. Therefore, the ballmap of the DDR2 nets of a top package is assigned well within the risk limit of the weighting factor 3.0.

B. Estimation of Model Boundary of SIP (System-in-Package)

Under the same conditions corresponding to POP package, we carried out an experiment by using an SIP package design (169 ball-FBGA-09mm x 09mm, 4layer PCB) with 3 chips to verify and demonstrate the accuracy of the postulated methodology. As described in Fig. 7, most of SIP packages have a complicated connection between the diepad and ball. In the case of SIP packages with multiple chips, the proposed estimation method can

be used to consider the routing complexity among 3 chips. Therefore, the weighting factor of the SIP package can be obtained from the crossover and angle data of each pin for the 3 chips. Fig. 8 is a 3D view of the SIP package designed for the Fig. 7. An SIP package with multiple chips is extremely complicated because the design of the bonding wire is comparable to that of Single-Chip-Package (SCP). In this section, the proposed algorithm is used to estimate an SIP model. Figure 9 shows the comparison of the inductance between the exact model obtained by the post-simulation and that obtained by estimation (maximum & minimum) for each signal pin of the SIP package. As one can see in Fig. 9, the exact model of each pin is bounded successfully between the maximum and the minimum estimation model of the proposed method. The errors of this method converge within a reliability range of 1 [nH] for all signal nets.

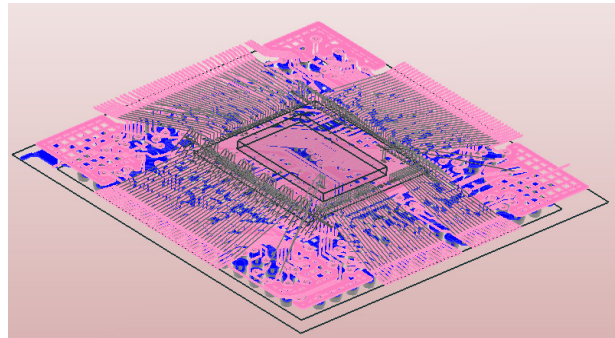


Fig. 8. 3D view of SIP package (169 ball - FBGA - 09mm x 09mm)

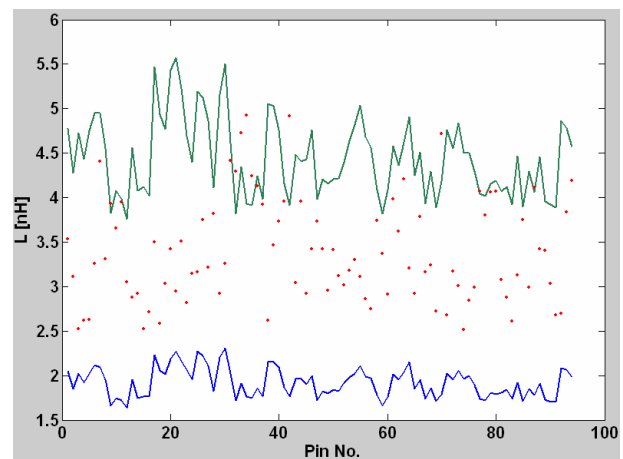


Fig. 9. Comparison of the inductance for post-simulation and estimation (worst & best case) for each signal pin of the System-in-Package (SIP) (169 ball-FBGA-09mm x 09mm). Green and blue solid line represents the maximum and minimum boundary of the inductance and the red dotted line indicates the exact inductance extracted from 2.5D field solver with the package design shown in Fig. 8.

As indicated in Fig. 3, Fig. 5 and Fig. 9, it is clear that the presented estimation technique has the ability to estimate and evaluate the interconnect models of 3D stacked packages including SIP and POP within a reliable range of error rate.

4. Conclusion

In this paper, we introduce an effective estimation technique, which can estimate successfully the interconnect models of a 3D stacked packages in the early stage of the design. The accuracy of the proposed technique is verified with experiments using the SIP and POP package designed. The experiments on the two types of the 3D stacked packages (SIP and POP) indicates that the new approach estimates the model boundary with the accuracy comparable (the errors of the proposed method are under 1 [nH]) to that of the exact model. Therefore, the proposed algorithm offers much promise as a new estimation method, especially for 3D stacked package types. It is expected that IC-package-board co-analysis and package optimization in the early stage of the system design can be achieved easily by using the presented estimation technique of 3D stacked packages.

5. References

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