

Understanding Power Integrity in System Designs

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ABSTRACT

Designing optimal power supply scheme for high speed digital systems has become a great challenge in recent years as designs move towards low voltage systems with high current capacity and high data rates. The fundamental problem that designers face today is how to efficiently provide sufficient and stable power supply to core circuitry and IOs on chips through printed circuit boards (PCBs) and packages. To achieve such design goal in low voltage systems, low impedance path has to be designed and implemented on the entire power delivery network, i.e. power consumption over packages and PCBs needs to be minimized and controlled within design budget.

This paper first discusses the three important aspects of Power Integrity (PI), sufficiency, efficiency, and stability. It emphasizes that IC designers need to be aware that a low power device will not work properly if power consumption on package and board is not carefully analyzed and managed. The paper then presents how power delivery system (PDS) should be designed, modeled, analyzed, and verified using IC/package/board co-design methodologies. Finally, it demonstrates co-design and co-simulation flows of package-aware IC power design, chip-aware package/board power design, and system power delivery validation. With the presented flows, designers are able to identify power delivery problems and correct them by modifying chip, package, or board designs to achieve sufficient, efficient, and stable power supply in low voltage systems.

The paper originates the three fundamental aspects of power integrity: sufficiency, efficiency, and stability; and implements chip/package/board co-design flows for system power designs

I. Introduction

Power delivery system (PDS) design has become more difficult with the requirements of increasing switching speed and decreasing power consumption. Optimized low-power designs play a critical role in ensuring the successes of today's electronic products. The modeling and analysis methodologies that provide solutions to power delivery system design are the key to optimizing a power delivery system. Power Integrity (PI) was then introduced several years ago, as a means to develop such methodologies.

Unlike signal integrity (SI) analysis, power integrity deals with the phenomena on power delivery paths from a voltage source to active devices (ICs) through boards and packages, as shown in Figure 1. It is important to understand that only active devices consume power,

while other components on a power delivery path, such as printed circuit boards (PCBs) and packages, serve as the system interconnection in a passive way. Although the interconnects are not supposed to consume power, some power does escape from the system due to the loss of interconnects. Therefore, the fundamental requirement of power delivery system is to find a means to minimize power loss on PCBs and packages and to ensure sufficient voltage and current supplies to the desired devices at the times they are needed. This requirement is in fact the design goal of a power delivery system, which can be specified as follows:

- Capability to deliver sufficient power to designated devices (chips) at required times (Sufficiency)
- Capability to not deliver power to devices that do not consume power at required times (Efficiency)
- Capability to maintain stable power supply to designated devices (chips) at required times when

noises from other parts of the design interfere (Stability)

This paper first summarizes the methods that minimize voltage loss on PCBs and packages using the target impedance concept and decoupling strategies. It then demonstrates how the goal of power integrity can be satisfied through design, implementation, and verification within the Cadence design environment.

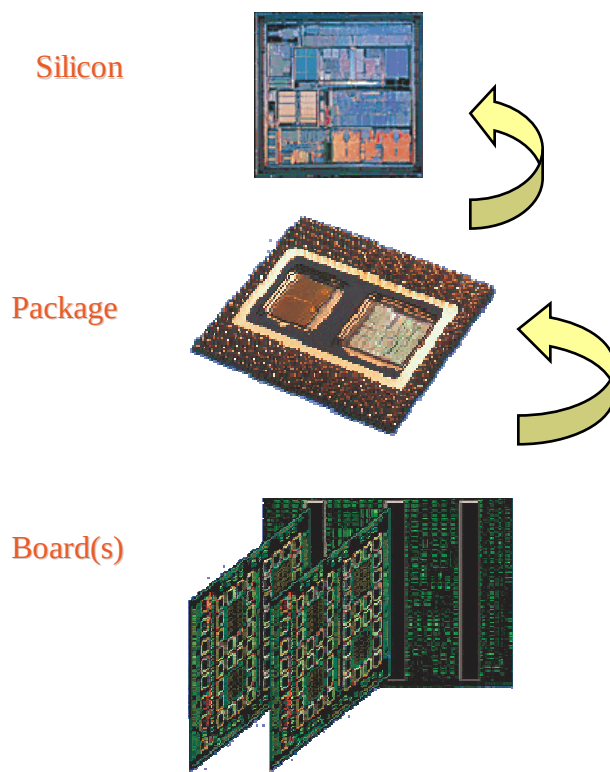


Figure 1. Power delivery system

II. Low impedance path of power delivery system

As it has been discussed above, a well behaved power delivery system should provide sufficient power supplies efficiently to the required devices at required times. A power delivery system is ideal when there is zero voltage loss on its delivery path, i.e. PCBs and packages. In addition, any disturbance imposed on the delivery path should have no impact on power variation to any active devices. Although, in reality, zero-loss delivery path is impossible to achieve, it sets up the design goal of reducing any resistance (or impedance) to power supplies on the path.

1. Impedance of power delivery system

The faster signaling of high-speed digital interconnects on package and board comes with faster edges and transients, requiring a proportionally wider bandwidth in the power delivery network. For example, in order to make an active device (chip) with fast signaling work properly, it may have 10A total transient current and require 50mV maximum ripple on the power delivery network. The design requirement here is to maintain the voltage ripple budget (50 mV) when the worst case transient current (10A) occurs. Since voltage ripples and the worst case transient current can happen at any frequency point, we can define the target impedance in the frequency domain to represent this requirement, as shown in equation (1).

$$Z_{target} = \frac{(power_supply_voltage) \times (allowed_ripple)}{current} \quad (1)$$

For the above example, equation (1) gives 5mΩ of target impedance throughout a wide frequency range. In practice, the target impedance which is effective at all frequencies is not achievable or necessary. A maximum frequency f_{max} is then defined for each particular design as Figure 2 shows.

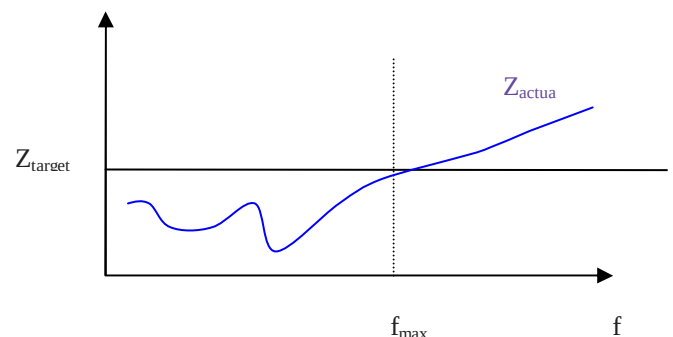


Figure 2 Target impedance defined as frequency independent

It is clear, from equation (1), that voltage changes can be controlled within the budget as long as the impedance of power delivery path is reduced to be below the target impedance within the required frequency range.

2. Power delivery path and its design procedure

A power delivery path includes plane configuration on boards and packages, trace routing of power and ground nets, location of decoupling capacitors, and spreading of power and ground pins of chip and packages. A standard procedure for package and PCB design of power delivery paths with low impedance can be summarized as follows:

- Specify impedance values at required frequencies;
- Design physical stackup of boards and packages to include sufficient plane layers or routed power supply and ground nets;
- Obtain frequency domain spectrum of available decoupling capacitors (based on their ESR and ESL values);
- Select decoupling capacitors with desired numbers and values;
- Place decoupling capacitors at effective locations.

Designers can find many references [1] [2] discussing design of low impedance of power delivery paths on packages or PCBs using the methods described above.

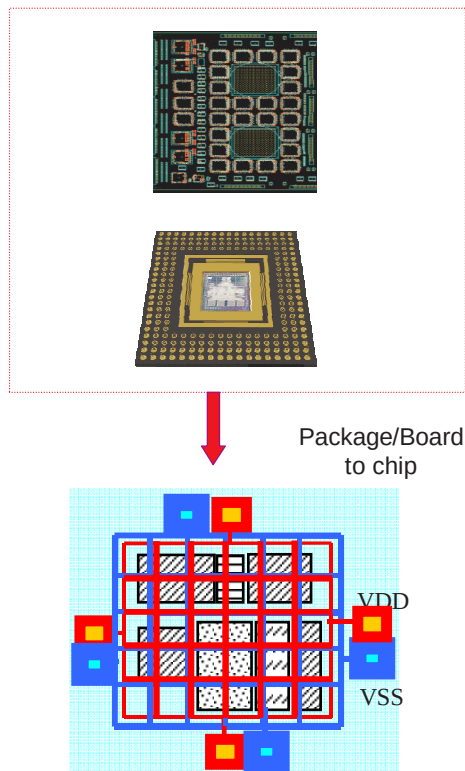


Figure 3 Package/Board awareness for chip power analysis

III. Co-design methodologies in power delivery system designs

Since a power delivery system in general is the entire power supply path from voltage source to active devices (chips) through passive interconnects (packages and PCBs), it would be difficult to design such a network across the three domains of silicon, package, and board. Considering the physical scales of PCBs, packages, and ICs, and the frequency ranges each of these components operates, the best approach to designing a power delivery system is through chip-package co-design and package board co-design.

1. Package-aware IC power analysis

When selecting a package to facilitate chip designs, IC designers need to be aware of the static and dynamic IR-Drop both on package and board before the voltage supply gets to the power grid on chip, as Figure 3 illustrates.

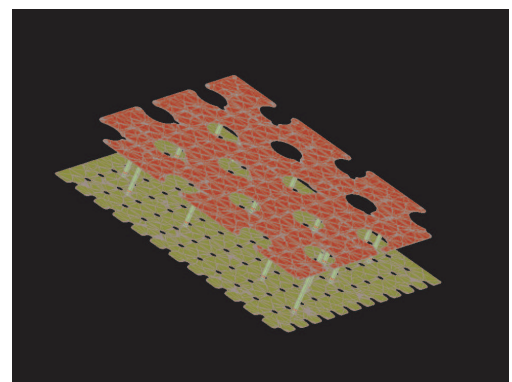
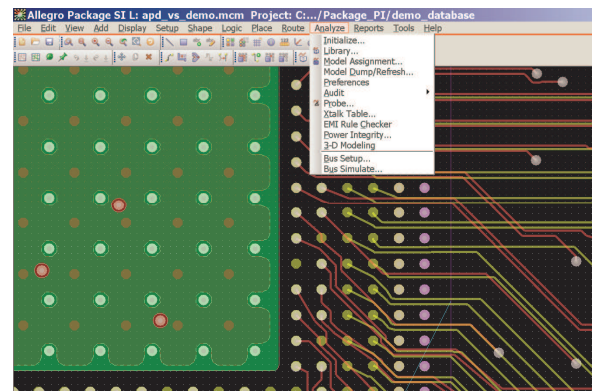
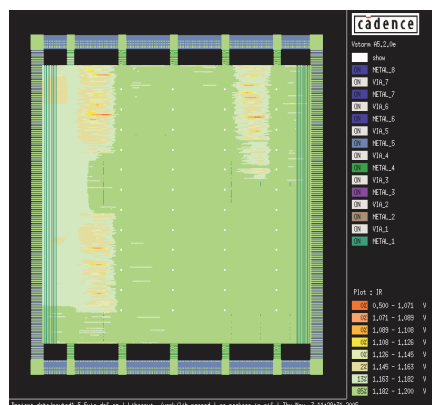


Figure 4 Sample package design and 3D modeling of power delivery path on the package

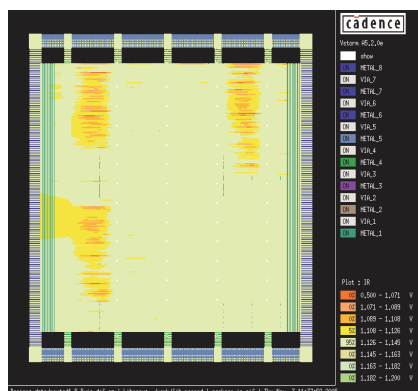
If the power delivery path on board is designed properly, meaning that target impedance is achieved within the desired frequency range, (i.e. from DC to cut-off frequency), it is logical to assume that an ideal voltage source is attached to the power pins at the BGA side on package. Then, the power delivery path in Figure 3 can be simplified to include only the package.

Based on the above assumption, a co-simulation flow to have on-chip power analysis include package effects is introduced and implemented.

In this flow, power and ground nets on an existing package are first modeled using power integrity functions with 3D field solver technology, as shown in Figure 4. The models are then passed on to an on-chip IR-Drop analysis tool, together with terminal mapping information between the package and IC databases.



(a) Without package effects: worst-case IR drop : 147.5mV



(b) With package effects: worst-case IR drop: 179.3mV

Figure 5 IR-Drop simulation results from IC power analysis tool

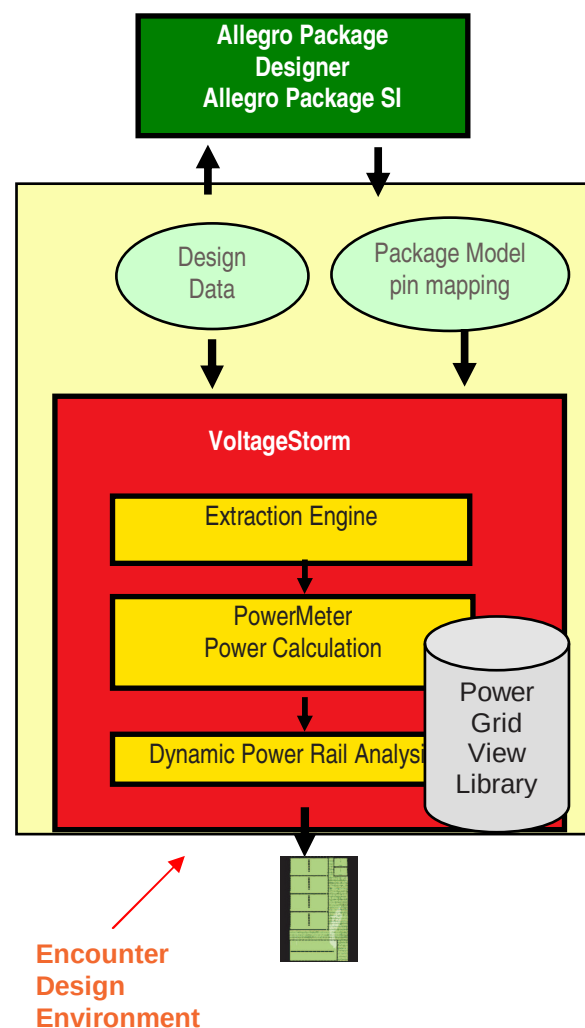


Figure 6 Cadence environment to analyze voltage drop on chip with package effects included

The IR-Drop analysis tool then builds the circuit that includes chip power grid and package power net models, performs IR-Drop analysis, and reports voltage changes on the grid during required time period.

Figure 5 gives the worst-case dynamic IR-Drop on chip with and without package effects included. It is evident that packages can introduce significantly additional IR-Drop to ICs. Ignoring this effect could result in chip malfunction, especially in low-power systems.

The complete chip-package integration in the Cadence design environment is described in Figure 6 and summarized as following:

- a. Chip is designed in Encounter

- b. Allegro Package Designer (APD) uses DEF information from Encounter to help design the package power delivery path
- c. Allegro Package SI creates and outputs sub-circuit models of power and ground nets on package, and a pin mapping file to VoltageStorm
- d. VoltageStorm combines the DEF design data from Encounter with the sub-circuit models from the package to account for package loading during the dynamic power rail analysis

2. Chip-aware package power analysis

When designing the package power delivery path, package designers need to be aware of the loading condition on chip that would affect the impedance profile on package. A natural way to include such loading effects, of course, would be to connect the chip circuitry with package and to perform analysis. However, considering the chip complexity, it is impossible to have such a circuit extracted and simulated in a package simulation environment. The most practical approach is to represent the chip power grid behavior with an equivalent sub-circuit which can be consumed by package analysis tools, as shown in Figure 7.

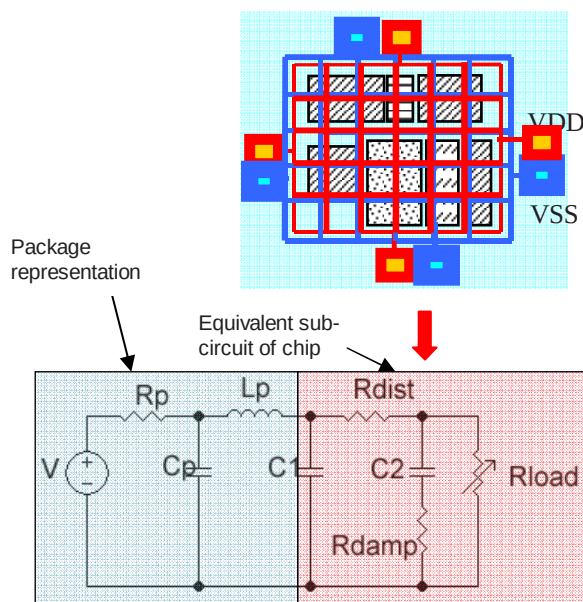


Figure 7 Representing power grid on chip by equivalent sub-circuit

In the Cadence design environment, such equivalent sub-circuit can be generated using VoltageStorm. When the power delivery path on package is configured and routed, the power integrity function in package SI tool is used to

create a coupled power and ground model. The model, which is in Spice sub-circuit format, is then connected to the equivalent sub-circuit of chip to build the entire simulation netlist. Frequency domain analysis is performed to obtain the complete impedance profile of power delivery path on package with chip loading condition accounted for.

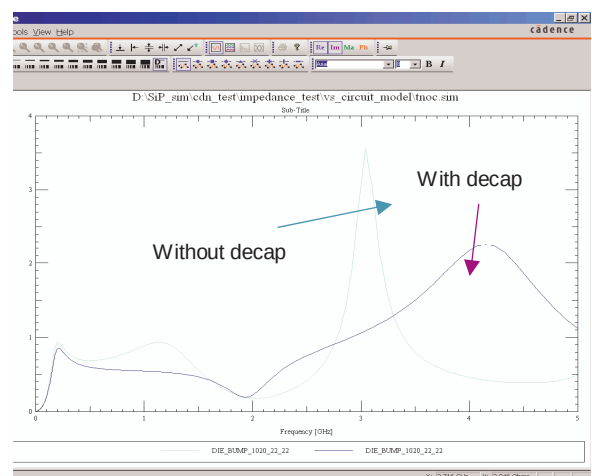
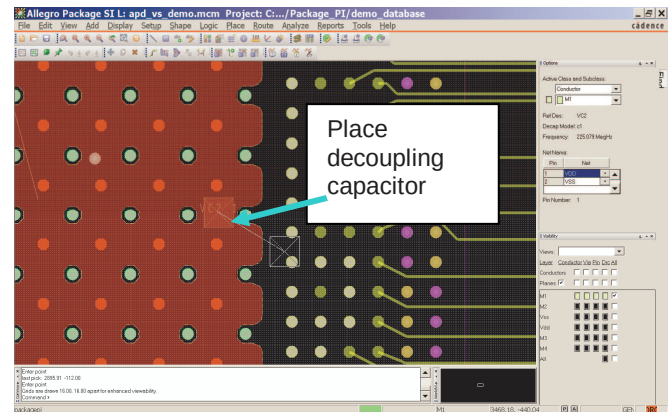


Figure 8 Impedance profile of power delivery path on package and decoupling study using chip equivalent sub-circuit

Using the impedance profile, one can study decoupling strategies, as shown in Figure 8, and exercise decoupling schemes by placing decoupling capacitors at different locations on package, or modifying the power delivery path configuration and routing. This will result in an optimized power delivery path design on package that meets target impedance requirements.

Combining the methodologies demonstrated above, a complete co-design flow for chip-package power delivery system design and simulation can be obtained, as Figure 9 shows.

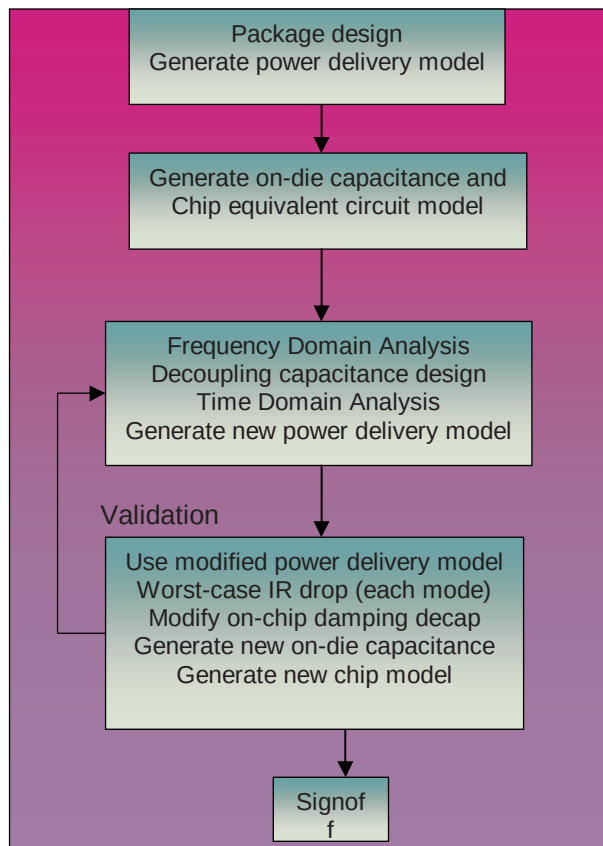


Figure 9 A complete co-design flow of chip-package power delivery system design and simulation

4. IC-Package-aware PCB power analysis

PCB designers use maximum switching current on chip to determine the target impedance of the power delivery path on board, based on equation (1). This may result in pessimistic impedance requirements. In addition, the usually large inductance of package can add up with board inductance at high frequency range and resonate with on-die capacitance. Therefore, PCB designers need to obtain more accurate IC and package information to design effective and efficient power delivery path on board. Figure 10 illustrates this scenario. As shown in Figure 11, such information includes switching current profiles of ICs, on-die capacitance, and package inductance. An example is given in Figure 12 to show how impedance profiles and voltage ripples of a power rail on board change due to the impacts of on-die capacitance and package inductance.

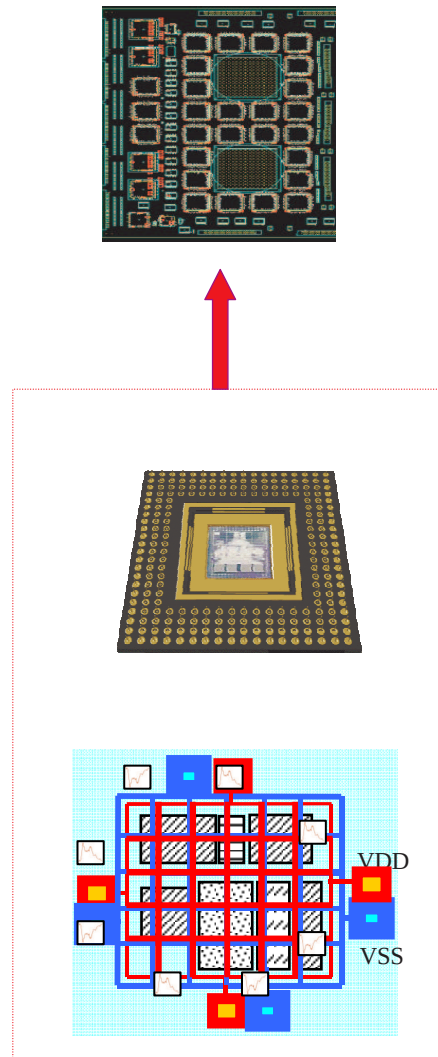


Figure 10 Using chip-package information to guide PCB power delivery design

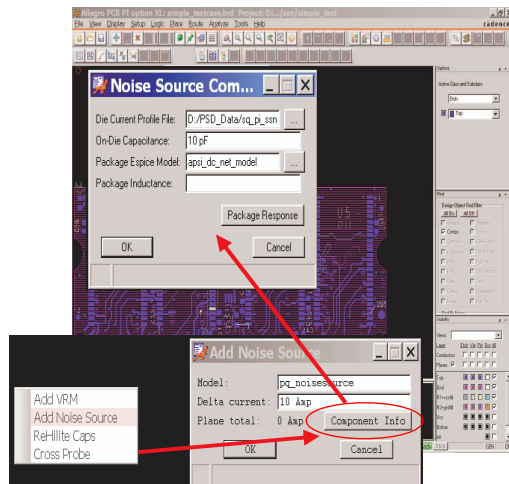


Figure 11 Input IC and package information available to Power Integrity tool on board

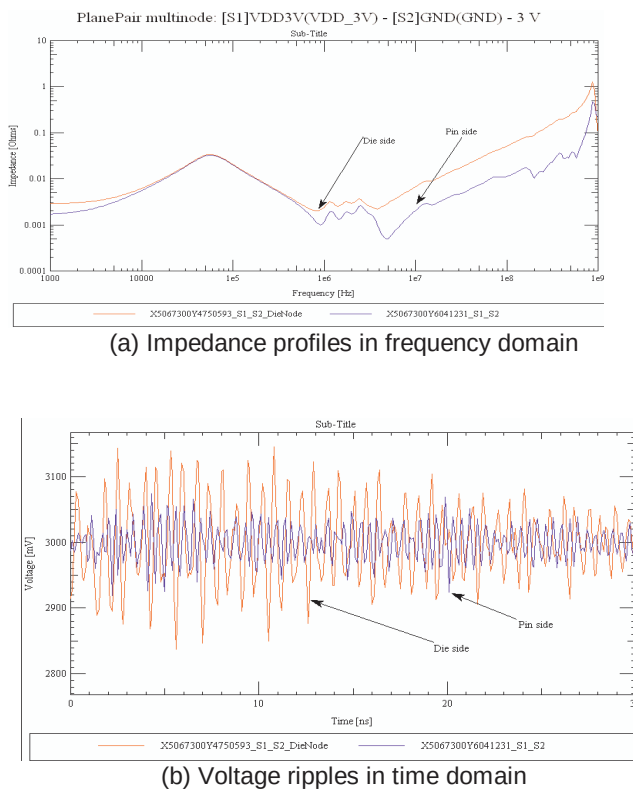


Figure 12 Effects of IC current, on-die capacitance, and package inductance included in power delivery path design on board

IV. Verification of power delivery system design

Power delivery system design will not be complete if there is no verification analysis applied to the system. The verification includes IR-Drop (to examine sufficiency and efficiency) and SSN (to examine stability) simulation using detailed models of the power delivery path and signals contributing coupling and switching noises to power delivery system. Here we use a sample design, a PCI-Express design as shown in Figure 13, to demonstrate the verification procedure using Cadence tools. At the final design stage, transistor based buffer models are created and assigned to active devices; signals and power delivery path are extracted and modeled using the power integrity function in Cadence's package analysis tool; and the board is represented by long differential traces. Figure 14 gives the complete circuit representation. Simulation results with signal and power variations in time domain are displayed in Figure 15.

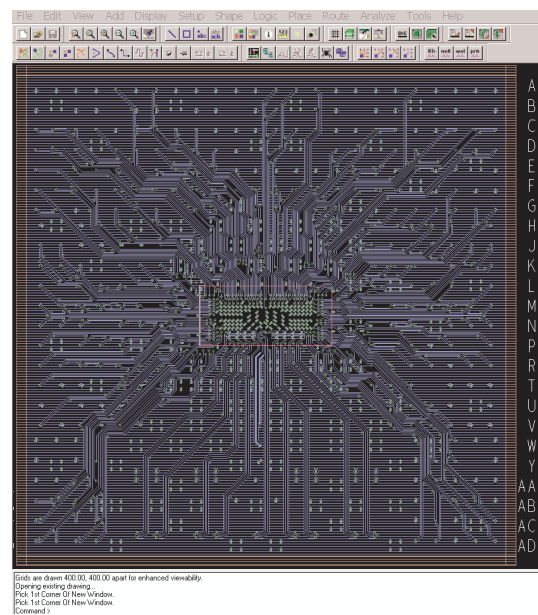


Figure 13 A sample design: PCI Express design

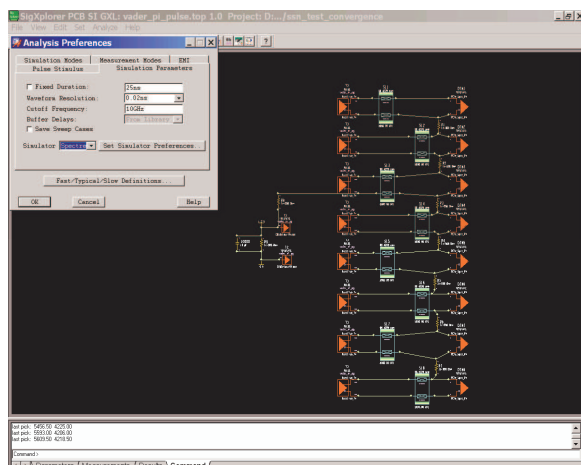


Figure 14 Simulation topology for SSN analysis

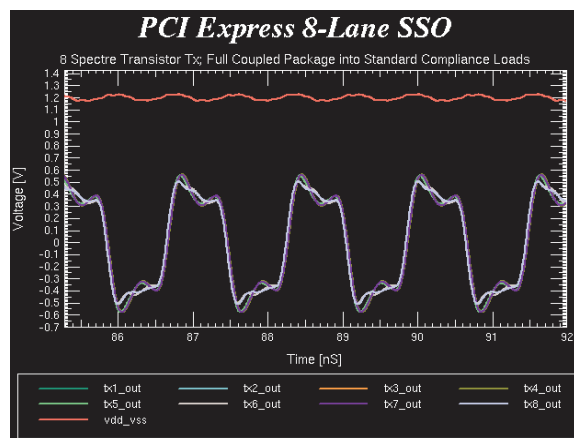


Figure 15 Simulation results to verify a power delivery system design

V. Conclusions

A successful design of power delivery system is measured by three important factors: sufficiency, efficiency, and stability. This paper presents how a power delivery system can be designed, implemented, and verified to satisfy the three requirements using co-design and co-simulation methodologies of chip-package and package-board. Examples are also given to show the integration of the methodologies within Cadence design environment.

VI. References

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