

Optimization of Redistributed Layers between Heterogeneous Devices for Wafer-Level Integration

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Abstract

Pseudo-SOC (System on Chip) technology is integration technology consisting of the chips embedded in epoxy resin and redistributed (thin-film metal) layer formed with semiconductor process, realizing the complementary advantages of SOC and SIP (System in Package) technology. In this technology, high-density integration is achieved by integrating heterogeneous chips with very narrow gap in the resin and without interposer substrate. In this paper, the authors focused on the improvement in the pitch of the redistributed layer by improving the planarization and the adhesivity of the underlying layer. By improving the transfer process of the chips and the printing process of the resin, the resin was formed between the chips set with narrow gap of 100 μm with good filling ratio. Furthermore, by controlling the formation condition of the planar layer, redistributed layer with a fine pitch of 15 μm /15 μm in line and space was achieved. Thus, the redistributed layer with a pitch 3 times finer than that of the device previously developed was realized, leading to the miniaturization of pseudo-SOC.

Keywords: SIP, SOC, pseudo-SOC, chip redistribution, planarization

1. Introduction

High-density integration technology is one of the most promising driving forces in electronics-related technologies as it enhances the performance of electron device systems. The main stream of system integration technology is SOC (System on Chip) and SIP (System in Package). SOC technology realizes monolithic integrated chips. However, it is difficult to integrate heterogeneous chips to one chip. On the other hand, SIP technology reduces the cost by integrating ready-made heterogeneous chips. However, the integration density of SIP is rather low. Thus, integration technology capable of solving the problems of SOC and SIP is required.

The authors have proposed pseudo-SOC technology that is set up with heterogeneous chips embedded with epoxy resin, planar layer and redistributed layer [1-3]. Figure 1 shows the schematic view of pseudo-SOC. The pseudo-SOC is set up with heterogeneous chips, such as MEMS, driver, CPU and memory, formed by means of the corresponding fabrication technologies, with epoxy resin, planar layer and redistributed (thin-film metal) layer. The heterogeneous chips are separated and selected as KGD (Known Good Die) chips before being redistributed and integrated to a chip-redistributed wafer. Thus heterogeneous devices are integrated in one chip at a reduced cost, same as SIP. By forming redistributed layer (global layer) with the most advanced semiconductor process, redistributed layer with fine pitch can be

achieved. Thus, integration with high density can be also achieved, same as SOC.

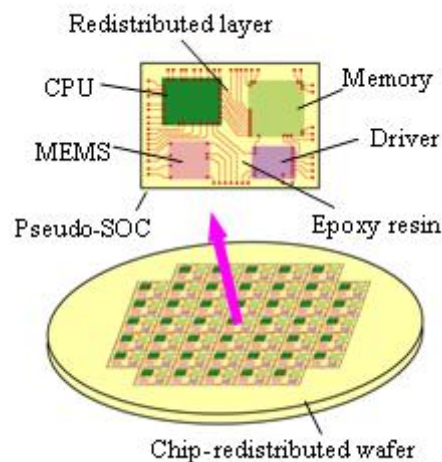


Figure1: Concept of pseudo-SOC

In previous studies, analysis of the residual stress in pseudo-SOC was carried out in order to optimize the mechanical stability by using FEM simulation and stress measurements with TEG chips with stress gauges. By optimizing filler content in the resin, the stress was suppressed. Also pseudo-SOC devices such as RF receiver module were developed where thin-film redistributed layers of 50 μm /50 μm in line and space were formed. However, the pitch of the redistributed layer was the same as that of SIP, much larger than that of SOC, which is the target of pseudo-SOC [1-3]. In

order to realize pseudo-SOC with redistributed layer, several problems such as surface planarization and adhesion of the redistributed layer need to be solved. Several studies were reported on the redistributed layer for heterogeneous chips encapsulated with resin, realizing redistributed layer with $20\mu\text{m}/20\mu\text{m}$ in line and space for the finest pitch [4-7]. However, detailed study on the planarization such as the relation between the condition of encapsulation and transfer process and the planarity was not reported.

In this study, by improving the chip redistribution process and planar layer process, the planarity of the chip-redistributed wafer was improved with the step of less than $3\mu\text{m}$. Redistributed layer was formed on plasma-treated planar layer to improve the adhesivity. As a result, redistributed layer with fine pitch of $15\mu\text{m}/15\mu\text{m}$ in line/space was achieved. Thus, the redistributed layer with a pitch 3 times finer than that of the device previously developed was realized, leading to the miniaturization of the device.

II. Pseudo-SOC process

Figure 2 shows a fabrication process of pseudo-SOC. The process consists of three main processes: chip redistribution process, redistributed layer process and pseudo-SOC grinding process. In the chip redistribution process, heterogeneous KGD chips were picked up with a pick-up layer using adhesive or vacuum contact. The picked-up chips were redistributed on an adhesive layer on a supporting substrate. The resin was cured using curing oven in order to cure it temporarily on the adhesive layer. After that, the cured resin with chips or the chip-redistributed wafer was peeled from the adhesive layer, and then cured to harden it completely. In the redistributed layer process, an insulator was formed on the wafer as a planar layer to the step height between the resin and the chips. After that, thin-film metal layer was formed and then patterned with semiconductor process to achieve the redistributed layer with fine pitch. In the pseudo-SOC wafer grinding process, the wafer was ground in the post-process in order to achieve ultra-thin pseudo-SOC.

Figure 3 shows the formation process of the resin using the vacuum printing technique. A sample where chips to be integrated were mounted on the adhesive layer was introduced into a vacuum chamber, and the pressure was reduced to a certain pressure by pumping. Next the pressure was controlled to a primary pressure P1 and the resin was spread by a squeegee A. Next, the pressure was changed several times between the primary pressure P1 and a secondary pressure P2 in order to reduce air bubbles mixed in the resin. Then, the resin was planarized by a squeegee B in the pressure P2. In the vacuum printing method, the quantity of the bubbles in the resin can be reduced greatly by

printing the resin in the diminished pressure atmosphere. Furthermore, good filling to the narrow gap region between the chips can be achieved by controlling the pressures P1 and P2.

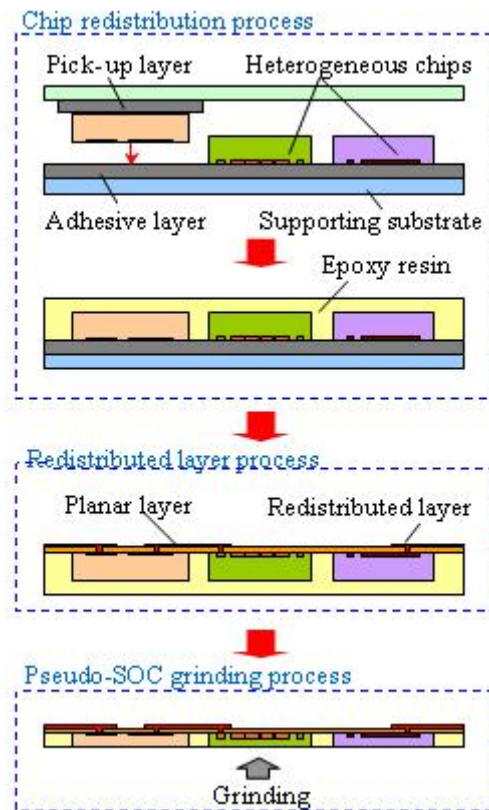


Figure 2: Pseudo-SOC fabrication process

III. Problems for Fine Pitch and Models toward the Target

There are several problems to be solved in order to realize redistributed layer with fine pitch on chip-redistributed wafer. On the chip-redistributed wafer, there is a step between the chips and the resin. The surface roughness is also high as the resin is filled with silica fillers of several tens of microns in size, partly exposed on the surface. Thus, the step and the roughness may be induced even on the planar layer of the wafer. So, the redistributed layer could be cracked or broken at the step if the coverage of the planar layer is insufficient. Furthermore, as the step and the roughness increase, the resolution of the photoresist pattern may deteriorate owing to the difference of the exposure gap under the mask at the UV exposure process. Thus, planarization of the wafer needs to be realized. As the planarity of the wafer is due to several factors, such as the transfer process of the chips, encapsulation process and planarization process, these factors need to be resolved.

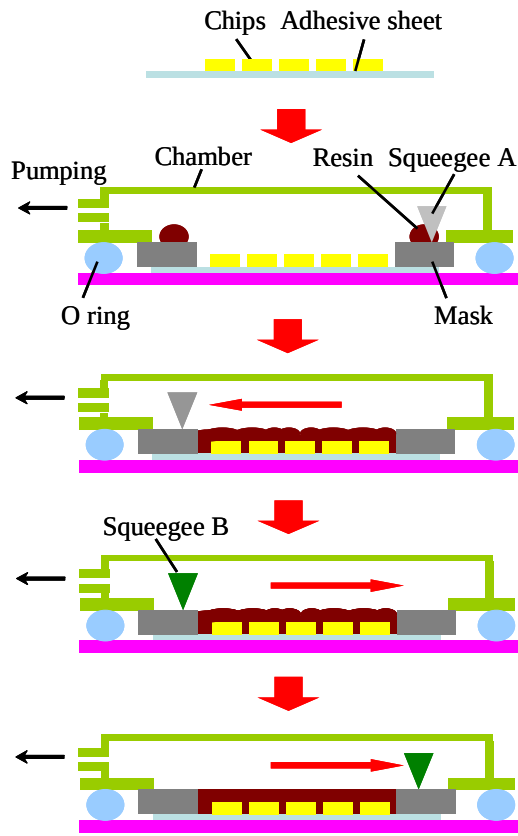


Figure 3: Vacuum printing process

Figure 3: Vacuum printing process

The adhesivity of the redistributed layer on the planar layer is also a serious problem. In order to realize redistributed layer with fine pitch, that is, the square of the thin-film metal line is very small, the adhesion strength between them also becomes small. As a result, the metal can be peeled off when being etched with wet solution. Furthermore, as the planar layer is to be formed on the epoxy resin, the curing temperature cannot be elevated above the decomposition temperature of the resin. Thus, the material as well as the formation condition for the planar layer is limited. Therefore, it is necessary to ensure enough adhesion to endure the etching process for very fine line pattern on a PI film in a limited condition.

Figure 4 shows a model of pseudo-SOC with planar and redistributed layers. As shown in this figure, the step, shown as s_1 , may be induced between the chips and the resin, which may induce the step, indicated as s_2 , on the planar layer with the thickness of t . Thus, two ways of decreasing the step s_2 are considered. One is to reduce the step s_1 by controlling the chip redistribution process, and the other is to increase the thickness t by controlling the formation process of planar layer. Thus, in this study, the planarization on the pseudo-SOC was considered in order to realize a

redistributed layer with a fine pitch.

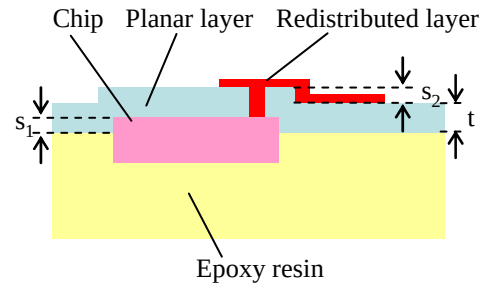


Figure 4: Model of pseudo-SOC with planar and redistributed layers

Figure 5 shows three models for formation of the step between the chip and the resin at the encapsulation process. For model A, the adhesive is deformed at the mounting process of the chips, which may induce the step in the resin printing process. To confirm the validity of this model, it is effective to study the mounting force dependence of the step s_2 , since the step s_2 may be increased if the deformation of the adhesive A is essential to the step s_2 . For the model B, a part of the resin is peeled off and then transferred to the surface of the adhesive. To confirm the validity of this model, it is effective to investigate if there is some residue on the adhesive A. For the model C, the resin cannot reach the adhesive surface at the printing process because of the narrow gap between the chips and the lack of the pushing pressure in the chamber of the printing machine. As mentioned above, the resin is formed on the chips as well as on the adhesive with the vacuum printing method before being cured with an oven. Thus, to confirm this model, it is effective to investigate the relation between the pressures P_1 , P_2 and the step s_2 . By assuming these models, the step on the wafer was evaluated in this study.

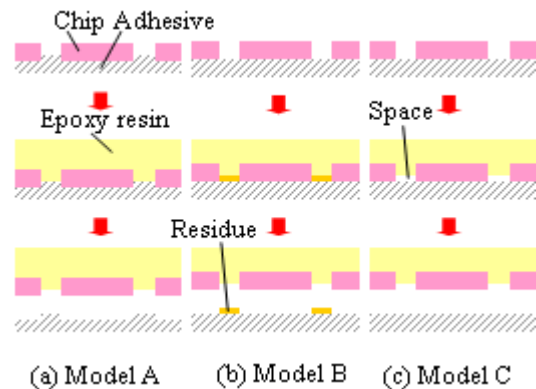


Figure 5: Models for the induction of the step on the chip redistributed wafer

IV. Experiment

A Mounting and peeling process

Figure 6 shows a schematic image of the measurement on the step of the chip-redistributed

wafer by controlling the mounting condition of the chips. TEG chips (Phase 8; Hitachi Ultra-LSI Co. Ltd.), whose size was $3.5\text{mm} \times 3.5\text{mm} \times 200\mu\text{m}$, were mounted with flip-chip bonder on adhesive sheet on a glass substrate. The adhesive sheet consisted of three layers: adhesive A, base film (PET) and adhesive B. The mounting force F was varied from 1N to 100N in order to study the effect of the deformation of the adhesive layer at the mounting process. The thickness of the adhesive A, indicated as d , was also varied from 4 to $50\mu\text{m}$, as it is thought to be effective for reducing the deformation, while the thickness of the base film and the adhesive B was fixed to $100\mu\text{m}$ and $15\mu\text{m}$, respectively. Resin was printed under the condition that the primary pressure P_1 of 0.2kPa and the secondary pressure P_2 of 20kPa. By curing and then peeling off the sample of the chips encapsulated with the resin from the adhesive, a chip-redistributed wafer was formed. Finally the step s_1 was measured using surface profile measurement machine P10 (KLA Tencor Inc.)

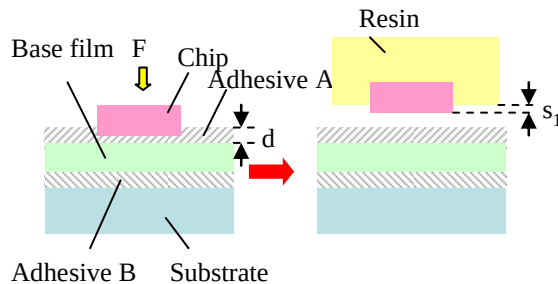


Figure 6: Schematic view of mounting condition dependence on the step of the chip redistributed wafer

IR spectrum measurement was also conducted in order to find out if some resin was transferred onto the adhesive surface at the chip-redistribution process. Figure 7 shows the schematic view of the measurement. A silicon wafer was mounted on the adhesive before being encapsulated with epoxy resin. The surface of the adhesive to the epoxy surface peeled off from it (Z) was measured and the spectrum was compared with those of the epoxy (X) and the adhesive before the fabrication process of pseudo-SOC (Y).

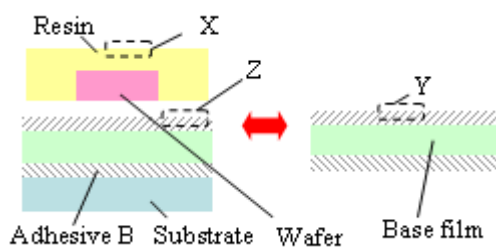


Figure 7: Schematic view of measured points for IR measurement

B. Printing process

Figure 8 shows a schematic view of the

measurement on the step of the chip-redistributed wafer by controlling the printing condition of the chips. A bare silicon wafer of the thickness of $400\mu\text{m}$ was laminated with an adhesive using hand roller, before being encapsulated with the resin using the vacuum printing process. For the adhesive A', the thickness was $4\mu\text{m}$, while the thickness of the base film and the adhesive B was fixed to $100\mu\text{m}$ and $15\mu\text{m}$, respectively. The primary P_1 and the secondary pressure P_2 were varied to study the effect of the pressure in the printing process. The primary pressure P_1 was varied from 0.2 to 80kPa where the P_2 was set to 80kPa. The pressure P_2 was also varied in the region between 0.2 and 2kPa where the P_1 was set to 0.2kPa. The gap g was set to $110\mu\text{m}$. The step between the gap s_1 was measured using laser microscope.

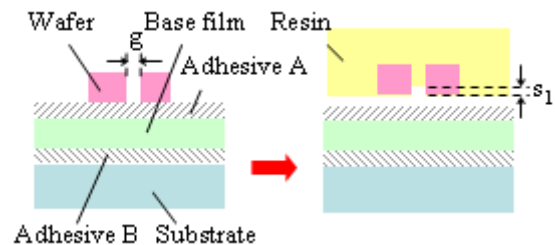


Figure 8: Schematic view of mounting condition dependence on the step of the chip redistributed wafer

C Redistributed layer process

In order to realize the redistributed layer with fine pitch, formation condition of planar layer and redistributed layer on the chip-redistributed wafer was studied. Figure 9 shows a schematic view of the measurement on the step of the chip-redistributed wafer by controlling the formation condition of the planar layer. The step s_1 was varied by varying the condition of the adhesive as well as the epoxy resin material. On this wafer, PI film was coated using spin coater and then cured in an oven. The thickness t was set to $7\mu\text{m}$. The step s_2 was measured using the surface profile measurement machine P10. In order to evaluate the relation between the planar layer thickness t and the step s_2 , planar layers with the thickness t varied were also formed on the silicon wafer with the step of $10\mu\text{m}$ in depth.



Figure 9: Schematic view of mounting condition dependence on the step of the chip redistributed wafer

Next, formation condition of the redistributed layer on the planar layer was studied. A plasma treatment was conducted with chemical dry etching machine CDE650 (Shibaura Eletec Co., Ltd.)

Figure 10 shows the plasma treatment apparatus used in this study. The mixture of CF₄ and O₂ was plasma activated by the microwave power supply (2.45GHz) and then sprayed through the nozzles to the sample set on the rotating stage (450mmφ). Table 1 shows the plasma treatment condition. Gas flow ratio of CF₄/O₂ was varied in order to confirm the adhesivity between the planar layer and the thin-film metal layer. Thin-film metal of Al/Ti was formed with the sputtering method. After photolithography process, the thin-film metal was etched with acidic solution.

Table 1: Plasma treatment conditions

Gas flow (CF ₄ /O ₂) (sccm)	40/400	290/150
Power (W)	600	600
Pressure (Pa)	30	30
Time (sec)	15	15

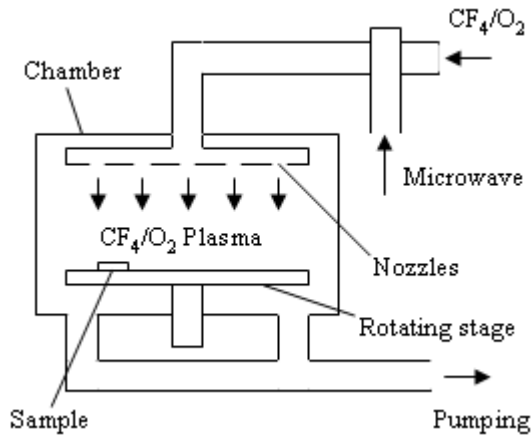
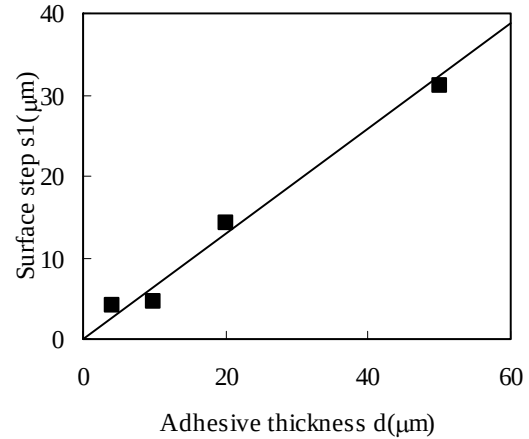


Figure 10: Plasma treatment apparatus

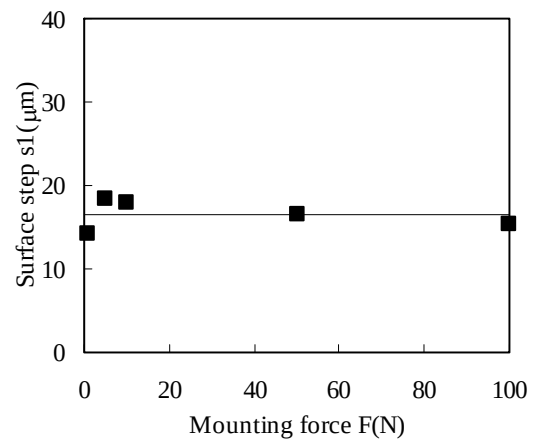
V. Results and discussions

A Mounting and peeling process

Figure 11 shows the measurement results for the adhesive thickness dependence of the surface step on the chip-redistributed wafer for the mounting force F of 1N. As shown in these figures, the step s_1 depends on the thickness of the adhesive A , and by decreasing the thickness, the step can be reduced. By using an adhesive A of 4 μm in thickness, the step s_2 was reduced to 4 μm . Figure 11 also shows the mounting force dependence of the step for the adhesive with the thickness d of 20 μm . The step was almost the same even if the force F was varied from 1 to 100N. If the step s_1 was induced by the deformation of the adhesive A at the mounting process of the chips, the step must be larger as the mounting force was larger. In this case, the deformation of the adhesive induced by the mounting force F was thought to be reduced to less than 4 μm at least. Thus, it was confirmed that the step s_1 was not induced only by the deformation of the adhesive A when the chips were mounted on it.



(a) Adhesive thickness dependence



(b) Mounting force dependence

Figure 11: Mounting condition dependence of the surface step

Figure 12 shows the measured IR spectrum. There were found to be some peaks (p_1) at 1630, 1600, 1584, and 1511 cm^{-1} in the case of the adhesive peeled off from the epoxy (Z), also observed in the case of the epoxy resin (X) but not in the case of the adhesive before the fabrication process of pseudo-SOC (Y). Those peaks are due to the framework vibration of the benzene ring in the epoxy material. Thus, some epoxy residue is transferred from the epoxy resin onto the adhesive surface. Furthermore, there were found to be some peaks (p_2) at 1780 and 1860 cm^{-1} due to cyclic acid anhydride only in the case of the adhesive peeled off from the epoxy (Z), which is thought to be formed as a result of reaction between the epoxy resin and the adhesive. From the results, it was estimated that some residue formed with the reaction between the resin and the adhesive was transferred to the adhesive and the surface step of the chip-redistributed wafer was induced.

B. Printing process

Figure 13 shows printing pressure dependence of the surface step of the chip-redistributed wafer. It

was revealed that as the primary pressure P_1 decreases from 80kPa to 2kPa, the step between the chips and the resin at the gap region decreases to about 70%. With regard to the secondary pressure P_2 , by increasing it from 0.2kPa to 2kPa, the step decreases to about 70%. As the resin is spread by the squeegee A into the gap in the primary pressure P_1 , the resin can be filled into the gap without air bubbles between the adhesive and the resin by decreasing the pressure of the atmosphere. On the other hand, because the resin can be pushed when being planarized with the squeegee B, the secondary pressure P_2 may push the resin. Thus, it would be preferable to control the secondary pressure P_2 to be more than the primary pressure P_1 in order to fill the resin into the narrow gap and to planarize the surface of the chip-redistributed wafer.

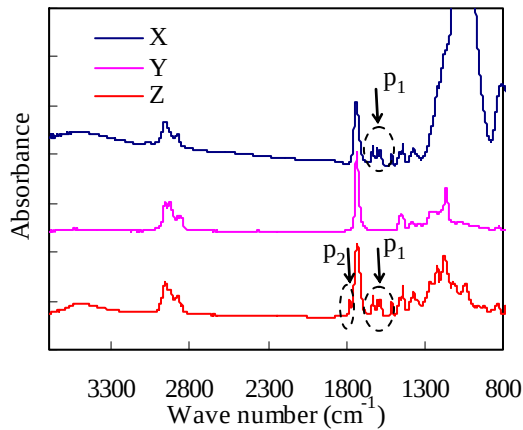
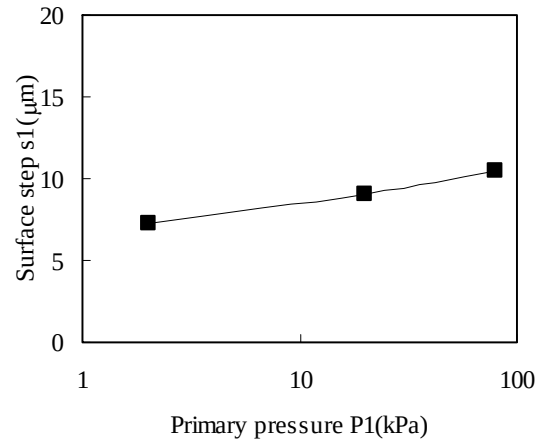


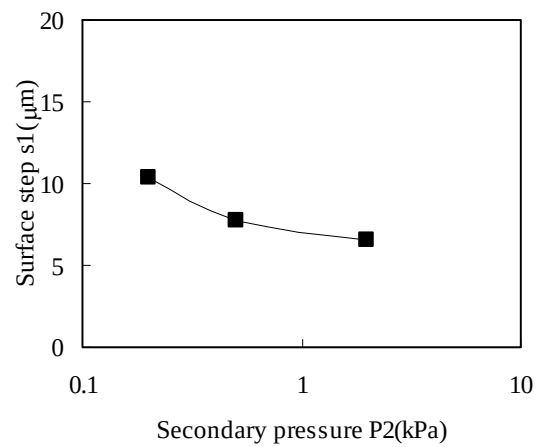
Figure 12: IR spectrum measurement results

C Redistributed layer process

Figure 14 shows the relation between the thickness of the planar layer t/s_1 and the surface step of the planar layer s_2/s_1 on the Si wafer. It was confirmed that by forming the planar layer and by thickening the layer, the surface step s_2/s_1 can be decreased. The step can be decreased to 80% by forming the PI planar layer with the thickness 2 times greater than the underlying step s_1 . Figure 14 shows the relation between the surface step on the planar layer and the surface step on the underlying chip-redistributed wafer. Thus, it was confirmed that by decreasing the step of the underlying layer, the surface step on the planar layer can be decreased. By forming the step of the chip-redistributed wafer s_1 to 4 μm , the step of the planar layer s_2 was decreased to 3 μm .



(a) Primary pressure dependence



(b) Secondary pressure dependence

Figure 13: Printing pressure dependence of the surface step

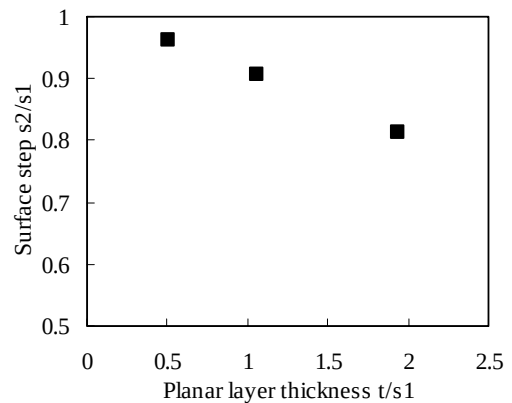


Figure 14: Relation between the normalized surface step s_2/s_1 and the planar layer thickness

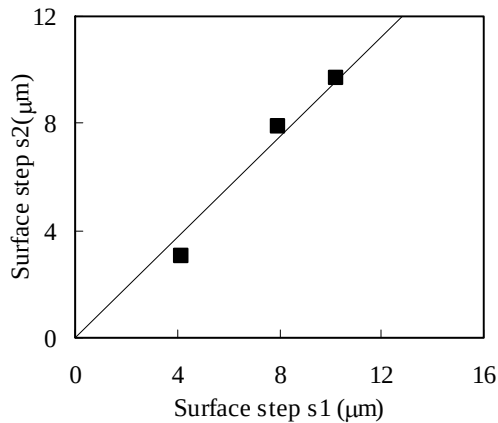


Figure 15: Relation between surface step of the planar layer and the surface step of the underlying layer

Figure 16 shows the image after the etching of Al/Ti thin-film metal on a PI planar layer on a SiO₂/Si substrate. The etching condition, such as the etching time and etching temperature, was the same to compare the results. As shown in this figure, the metal layer was peeled off between the Ti layer and the underlying PI layer after the etching of Ti layer for the gas flow ratio of CF₄ and O₂ of 290sccm and 150sccm, resulting in no metal line patterns in the image, whereas no peeling off occurred for the gas flow ratio of CF₄ and O₂ of 40sccm and 400sccm.

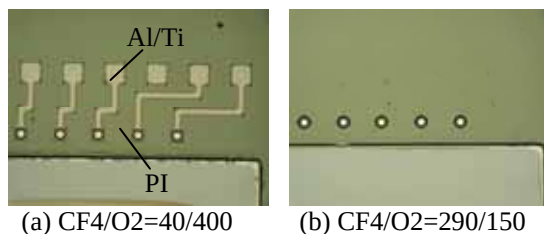


Figure 16: Metal lines on planar layer

Figure 17 shows thin-film Al/Ti lines formed on planar layer of PI on a SiO₂/Si wafer and on SiO₂ as reference. The thickness of the metal was 0.2 μm for Al layer and 0.02 μm for Ti layer. It was confirmed that the thin-film metal was successfully patterned with the line and space of 5 μm /5 μm at the finest on the SiO₂ surface as well as on the PI surface on Si wafer. Figure 18 shows thin-film Al/Ti lines formed on the planar layer of the pseudo-SOC composed of TEG chips integrated with a narrow gap of about 100 μm and epoxy resin encapsulating them. The thickness of the metal was 1 μm for Al layer and 0.1 μm for Ti layer, and the line width was about 10 μm . For the sample A with larger step with the surface step s_2 of about 8 μm , some cracks were observed at the edge of the chip even on the planar layer, whereas for the sample B with very flat surface with the surface step s_2 of

less than 1 μm , no crack was observed.



Figure 17: Redistributed layer on planar layer

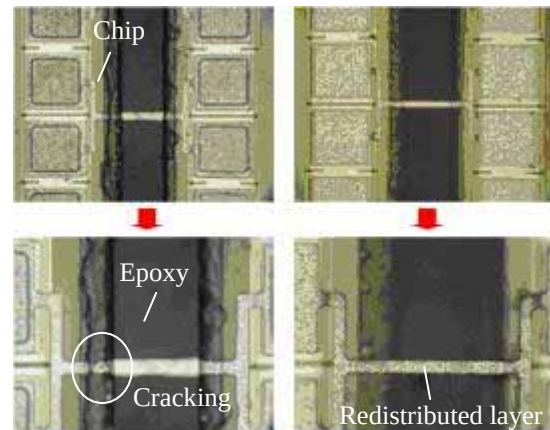


Figure 18: Redistributed layer on pseudo-SOC

VI. Conclusion

The authors have proposed a pseudo-SOC technology realizing the integration of heterogeneous chips, a novel integration technology realizing a thinned package structure with fine redistributed layer unattainable with the previous SOC technology, and integration of heterogeneous devices unattainable with the previous SIP technology. In this study, by improving the chip redistribution process and planar layer process, the planarity of the chip-redistributed wafer was improved with the step of less than 3 μm . Redistributed layer was formed on plasma-treated planar layer to improve the adhesivity. As a result, redistributed layer with fine pitch of 15 μm /15 μm in line/space was achieved. Thus, the redistributed layer with a pitch 3 times finer than that of the device previously developed was realized, leading to the miniaturization of the device.

Acknowledgments

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