Alternative Processing Methods for Copper Through Silicon Vias

Gayathri Devi Jampana[1], Leonard W. Schaper, Isi Abhulimen[2], Yang Liu
University of Arkansas, [1]Brewer Science, [2]Intel Corporation
University of Arkansas, Fayetteville, AR 72701
gjampana@uark.edu

Abstract

Over the past decade, there has been significant development of 3D packaging due to its reduced interconnect length and associated parasitics. Through Silicon Via technology (TSV) enables short and dense interconnects with increased speed and reduced noise. Via-first and Via-last are the two standard ways of fabricating TSVs based on the order of forming vias, either before or after fabricating active devices. In the project discussed here, TSVs are formed in a wafer that will function as a multichip substrate in a 3-D stack, and will not itself contain active devices.

At the University of Arkansas, most of the research projects have been based on the Via-last approach of fabricating TSVs. The method reported here is a novel approach of bottom-up filling of through vias using copper DC plating. Blind vias of aspect ratio 6:1 are first etched with Bosch scallops in a high resistance process wafer. Then the method involves two carrier wafers. The first carrier is bonded to the process wafer with a double-sided thermal release tape, which provides mechanical support during thinning. The process wafer is thinned down to 200 μm by grinding and blanket etch in RIE, until the backside of the vias are exposed. The process wafer is then debonded. The second carrier has a Ti/Cu/Ti seed layer to initiate copper plating and is bonded to the process wafer so that the bonding agent can be removed at the base of the vias to expose metal on the carrier for plating. Copper is plated using DC current on titanium for shearing of plated vias from the carrier wafer. Scallops inside the vias provide mechanical support to the plated copper. Wafers have been debonded and examined for plating uniformity and the presence of voids. This paper reports on the development of this novel process.

Keywords: Through Silicon Vias, Wafer thinning, Via Filling, Wafer bonding and debonding.

Introduction

Through Silicon Via (TSV) technology has gained importance over other 3D integration methods due to its advantages. TSVs reduce the length of global interconnects in 2D integration to a short Z axis conducting via through silicon, thus reducing the associated parasitics and increasing speed. TSV technology is rapidly advancing from R&D to commercialization. Some of the challenges of TSV commercialization are via formation, wafer handling, bonding and via filling. Several packaging, equipment, and material companies have formed an Equipment and Materials Consortium EMC^{3D} to solve these challenges, in order to move toward cost effective manufacturing [1].

Via filling is one of the challenges faced in the fabrication of through silicon vias. Blind-via filling before wafer thinning and through-via filling after wafer thinning are the two approaches in use today. In blind via filling, blind vias are etched in a silicon wafer; insulation, barrier and seed layers are deposited; vias are filled by reverse pulse plating; and then the wafer is thinned. In through-via filling, the silicon wafer is thinned; through vias are etched; the seed layer is deposited on the back side; vias are plated by bottom-up via filling; and the seed is removed. Blind via filling is the most prominent method used in industry and many other research groups. Through-via filling after wafer thinning has been reported by Nanyang Technological University [2]. Through vias were fabricated and insulated. A carrier wafer with Cr/Au seed layer was attached to the process wafer with photo resist. Copper plating with AC pulse filled up the high aspect ratio vias from the bottom. They failed to debond the plated vias from the carrier due to the strong inter-metallic bonding between the gold seed layer and the electroplated copper.

The approach reported here by the University of Arkansas is through-via filling after wafer thinning. Through vias were formed by blind via formation, wafer bonding, and process wafer thinning. Via filling was achieved by bottom up filling from the Ti/Cu/Ti seed layer on the carrier wafer with DC copper plating. The wafer, along with its copper TSVs, could be debonded from the seed layer on the carrier wafer. This process is designed to achieve stacked modules with embedded integrated circuits and through silicon vias. That is, the silicon module substrate itself only contains TSVs; the active devices are on ICs contained in cavities in the silicon module. Thus an alternative processing method of DC plating of TSVs with seed layer on a carrier wafer is a novel method replacing the conventional way of plating up blind vias with the seed layer on the process wafer, and could be particularly useful for forming TSVs in a wafer that does not itself have active devices. This research was conducted at the High Density Electronics Center (HiDEC) at the University of Arkansas, Fayetteville [3].

Proposed Process Flow

The goal was to fabricate void free interconnects with DC copper plating of straight side walled and scalloped Through Silicon Vias (TSV) in a high resistivity substrate. The process wafers were 400 µm thick, 125 mm in diameter, P (111) type with 998 Ω-cm resistivity. The photo mask, originally designed for 100 mm wafers, contained 7 groups of vias each 30 µm diameter on 100 µm pitch with an array of 12 X 40 TSVs in each group. The process wafers were patterned with a 16 µm thick layer of photoresist to form a masking layer on the polished front side. 200 µm deep straight, scalloped blind vias were fabricated by the DRIE Bosch process. Figure 1 shows 6:1 aspect ratio blind vias with Bosch scallops.

The 625 µm thick silicon carrier wafer provides both mechanical support and seed layer functionality for the thinned process wafer. EXP06017B thermoset high temperature adhesive from Brewer Science Inc. was used to bond the process wafer to the carrier wafer. The adhesive should be able to withstand high temperatures in RIE. A first layer of 4.5µm thick thermoset was spun on the carrier wafer to separate the process wafer during debonding. Ti-Cu-Ti metal layers were sputtered on the first layer of hard baked thermoset. These metal layers provide the seed layer during copper plating. A second layer of thermoset was spun on the sputtered metal to attach the process wafer to the carrier wafer.

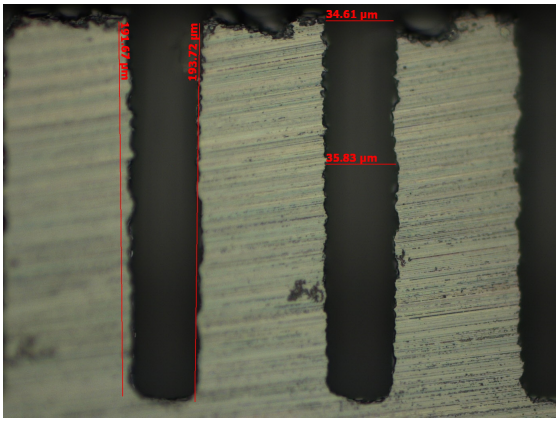

Figure 1. Blind vias with Bosch scallops

The front side of the process wafer was bonded to the carrier wafer at 180°C for 2 minutes under vacuum and 1psi pressure. The backside of the process wafer was thinned by grinding and silicon blanket etching to expose the backside of blind vias. 150 µm of silicon was removed by grinding the process wafer in 15 µm particle sized alumina slurry. The backside of the vias was exposed by etching the remaining 50 µm of silicon in RIE. The second layer of thermoset in the bottom of the vias was etched in RIE to expose the metal for plating. Titanium was removed by Ti etchant to expose the copper seed layer for plating. DC plating of copper with constant current was used for bottom up filling of the TSVs. Thermal decomposition of the thermoset adhesive at 400°C for 40 minutes releases the process wafer with copper filled through silicon vias from the carrier wafer.

Modified Process Flow

Some of the challenges faced during processing using the proposed process flow are addressed in this section. The solutions for the problems and modified process flow to achieve the goal are discussed in detail. Preliminary testing of the adhesive for its compatibility with the process flow revealed that two layers of thermoset with metallization in between fuse during thermal decomposition and make debonding impractical. So, Ti-Cu-Ti metals were sputtered on the polished surface of the carrier wafer and a single layer of thermoset was spun on to bond the process wafer.

Since the back grinding was uneven by ±6 µm, the vias in the outer perimeter were exposed initially from the backside during silicon blanket etching, followed by the vias in the center. Due to the

prolonged time in RIE to expose the backside of all the features, the adhesive and metallization at the bottom of the vias that were exposed initially was etched away by physically active ions. In some vias, there was no metallization in the bottom for copper plating. For successful plating throughout the wafer, a two carrier method was therefore introduced. The first carrier, a bare silicon wafer with a layer of thermoset, mechanically supports the process wafer during grinding and silicon etching. The secondary carrier contains sputtered metal layers and spun on thermoset for plating copper.

Bonding and debonding thermoset twice during the processing was time consuming, ineffective, and messy. So based on previous experimental results [4], Revalpha thermal release tape from Nitto Denko was adopted to bond the primary carrier wafer to the process wafer for grinding. The tape is double sided with a thermal release adhesive for easy release of the process wafer, and a normal adhesive for the carrier wafer. Revalpha tape can be applied at room temperature and released by heating to 120°C for 4 minutes. After grinding, the process wafer was released from the primary carrier and placed in the RIE for silicon blanket etching. The process wafer with through silicon vias was then attached to the secondary carrier with thermoset. Brewer Science ceased production of the thermoset adhesive and commercialized another high temperature adhesive, Wafer Bond™ HT-250. Further experimentation was carried out using Revalpha tape and thermoplastic Wafer Bond™ HT-250.

The 200 µm thin process wafer and the secondary carrier were bonded with HT-250 at 160°C for 5 minutes under vacuum and 1 psi pressure. The adhesive in the bottom of the vias was etched by RIE with oxygen. Oxygen gas alone formed a fiber-like residue in the bottom of the vias, but adding 10% of CF_4 gas to the reactive gas mixture increased the etch rate and also removed the residue in the bottom of the vias. Titanium was wet etched and copper was plated in the vias. After plating, wafers could be debonded at 250°C for 2 minutes and a shear force for 2 minutes. The fixture for applying shear force is shown in Figure 2. Debonding the wafers was difficult due to voided bonding and burnt adhesive in these voids during adhesive etching. Also, applying shear force on the thin process wafer fragmented the wafer. An alternative bonding method which avoids the high temperature etching of the adhesive was simply to develop exposed photoresist at the bottom of the vias. A negative tone photoresist was spun on the secondary wafer following metallization. The process wafer was attached and the resist was baked allowing the solvent to escape though the vias. When exposed, the process wafer acts as a mask for the resist and the exposed resist in the bottom of the vias is developed. Copper plating results are discussed in the following section.

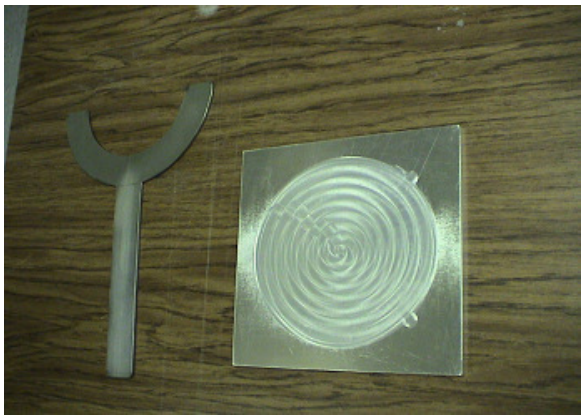

Figure 2. Fixture for debonding wafers

Results and Discussion

The CUBATH® SC copper electroplating process was developed by Enthone, and a simple plating system is in use at HiDEC. The copper plating solution consists of CUBATH SC MAKE UP with CUBATH SC MD and CUBATH SC LO 70/30 as additives. Additives were measured on the basis of used ampere hours and were added to the bath before plating the samples to have uniform copper coverage. Before plating the copper, the Ti layer in the bottom of the vias was etched with Ti etchant and ultrasonic agitation. The bottom of the vias was inspected for a clean copper seed layer. After plating for 4 hours at a current density of 20 mA/cm^2, the vias were partially filled. When the wafers are debonded, the plated copper in the through silicon vias should slide off the carrier wafer along with the process wafer. But the process wafer chipped off during debonding and the plated copper remained on the carrier wafer like copper posts grown from the seed layer due to the strong inter-metallic bonding between the plated copper and the copper seed layer. Thus, we developed an alternative of plating on titanium, which has weak inter-metallic bonding with plated copper compared to a Cu-Cu bond.

The photo mask described in the proposed process flow had a plating area of 0.1 cm^2, which was virtually negligible. Therefore, another photo mask

with 8 different sized vias and text in each section, as shown in Figure 3, was used. The vias with 100 µm, 75 µm, and 70 µm diameters etched deeper than the other vias and were exposed initially from the backside. The text and these vias gave a cumulative area of 6 cm^2.

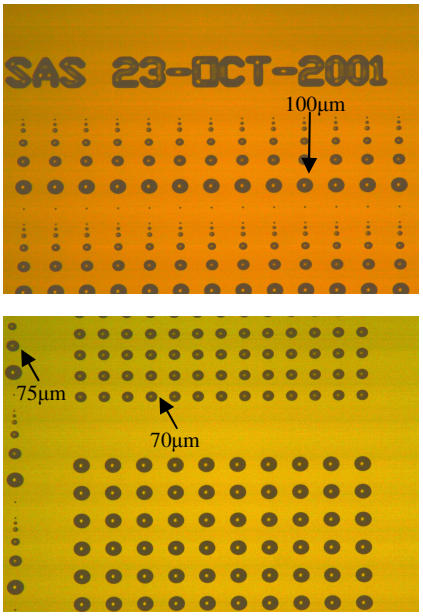

Figure 3. A) Text and 100µm, B) 75µm and 70µm diameter vias

Figure 4 shows 24 µm of plating in a 70 µm diameter via plated on titanium after 4 hours of copper plating at a current density of 20 mA/cm^2.

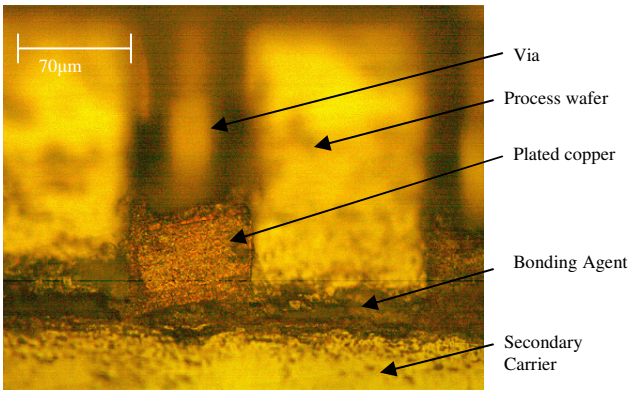

Figure 4. Plating in the vias after 4 hours

When plated for 6 hours with the same current density of 20 mA/cm^2, the copper was plated on the process wafer with very little plating inside the vias and the text was over plated. Figure 5 clearly shows that plating initiated on the carrier wafer and when the copper came in contact with the process wafer, even the high resistivity silicon started conducting and plating. Hence, a 2 µm silicon oxide insulation layer was deposited on both sides of the process wafer before bonding, forming a layer of insulation.

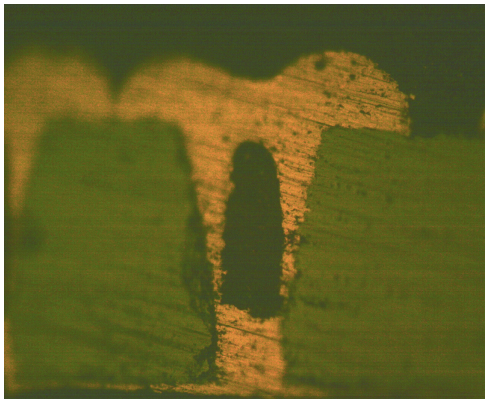

Figure 5. Void due to conducting silicon

After plating for 10 hours with 20 mA/cm^2 current density for the 6 cm^2 plating area, the vias at the edges of the pattern were plated through without voids as shown in Figure 6, and the vias in the center of the process wafer were partially filled as shown in Figure 7. The text was still over plated, thieving the copper from the vias, due to the expanded area and current concentration near the over plated copper. For future work, optimization of the plating parameters with a uniform feature sized mask is advised.

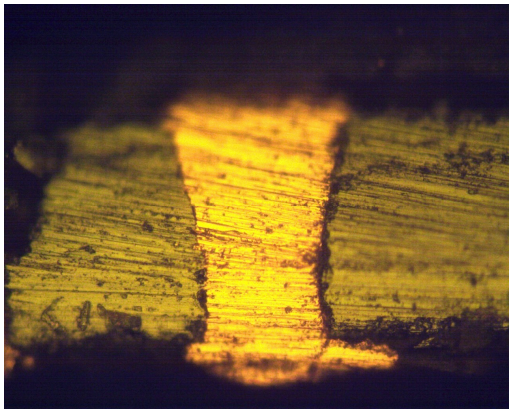

Figure 6. Copper plated TSV

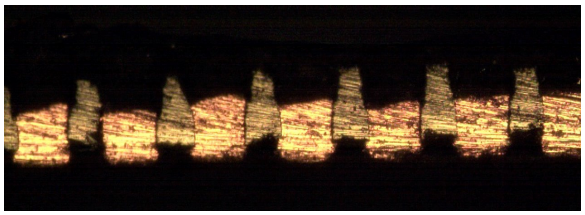

Figure 7. Partially filled vias

Final Process Flow

After modifying virtually step of the proposed process, we achieved a process for electroplating TSVs in silicon module substrate wafers using a seed layer on a separate carrier wafer.

The process wafer was a 125 mm diameter, high resistivity, P<111> type, 400 µm thin silicon wafer. It was patterned using photolithography to etch 200 µm deep, scalloped, straight side walled vias. A representative photo mask that provides a plating area of 6 cm^2 was used for process development. A single carrier process flow was replaced by a two carrier process flow; a primary carrier for wafer thinning and a secondary carrier for copper plating. Revalpha double sided thermal release tape bonded the primary carrier to the process wafer. Grinding the wafer with 15 µm alumina slurry for 45 minutes thinned down the process wafer to 250 µm. The process wafer was diced on one end to leave room for contacts for plating when bonded to the secondary carrier. Wafers were debonded by heating at 120ºC for 4 minutes. Silicon blanket etch in RIE etched away the remaining silicon and exposed the backside of the vias. A 2 µm thick SiO_2 layer was deposited on both sides of the process wafer for insulation. HMDS was applied to improve adhesion with photoresist during bonding. Ti (500Å)-Cu (3000Å)-Ti(500Å) thick metal layers were sputtered on the secondary carrier which was attached to the process/device wafer by photoresist. The resist in the bottom of the vias was exposed with UV light and developed under ultrasonic agitation. Bottom up via filling was achieved by DC plating for 10 hours at 20 mA/cm^2 current density on the top titanium of the seed layer, for better release of the plated copper. Wafers were debonded by ultrasonic agitation in an acetone bath.

Conclusions

We have shown that copper plated TSVs can be produced in thin silicon wafers using a plating seed layer on a secondary carrier wafer. This process avoids blanket plating and subsequent removal of undesired copper, and may be useful in certain TSV implementations.

Acknowledgements

This work was supported by Irvine Sensors Corporation under contract FA8650-04-C-7120 from the Defense Advanced Projects Research Agency (DARPA).

References

[1] Semiconductor International website- White Paper “EMC-3D Consortium Targets Cost-Effective TSV Interconnects”

[2] Pradeep Dixit and Jianmin Miao, “Fabrication of High Aspect Ratio 35µm Pitch Interconnects for Next Generation 3D Wafer Level Packaging by Through-wafer Copper Electroplating,” Electronic Components and Technology Conference, 2006, pp. 388-393.

[3] Gayathri Devi Jampana, “Alternative Processing Methods for Copper Through Silicon Vias for 3D Packaging” The University of Arkansas, MS Thesis - 2008.

[4] Ziaur Rahman, “Ultra thin Wafer Processing for Through Silicon Via in 3D VLSI Z-axis Interconnect Technology”, The University of Arkansas, MS Thesis-2002.