

Reliability Improvement of Resin Stress Buffer Layer Type Wafer Level Chip Size Package for Automotive Applications

Shunpei OGAYA, Shuichi TANAKA, Haruki ITO, Hirokazu ITO, Nobuaki HASHIMOTO
Advanced Technology Development Center, Production Engineering & Development Division
SEIKO EPSON Corporation
Fujimi 1010, Fujimi-machi, Suwa-gun, Nagano, 399-0295, Japan
Phone: +81-266-62-6721, Fax: +81-266-62-4415
ogaya.shunpei@exc.epson.co.jp

Abstract

With expanding applications of portable electronic devices such as mobile phones, packaging technologies that enable make it small, slim and high density have been evolved at rapid speed. In these technologies W-CSP (Wafer level Chip Size Package) is developed as an ultimate package that enables a real chip size package, and its usage in such fields has been increasing during last years. Recently, in accordance with increasing the requests of small package on car electronic devices, the adoption of W-CSP has been increasing at the car electronics field. Thermal cycle reliability at a board level test is important all the more. Compared with interposer type CSP, W-CSP is simple structure that is formed on IC chip. In other words, it is difficult to make complex structure on W-CSP. Therefore structure design to decrease thermal mechanical stress caused by differences in thermal expansion between the IC chip and the substrate is very important to obtain enough thermal cycle reliability for board level test. In addition, it is important to figure out influence of the dimension, material properties, and so on. In this paper, we describe the development of a W-CSP structure that includes a resin stress buffer layer to improve thermal cycle reliability on a board level test using finite element method. Applying finite element method results, the modified W-CSP reliability has improved more than double compared with an ordinary W-CSP reliability at a thermal cycle board level test.

Keywords: Wafer Level Package, Reliability, Simulation, BLT, Viscoelasticity

1. Introduction

With expanding applications of portable electronic devices such as mobile phones, packaging technology that enable make it small and high density have been evolved at rapid speed. In these technologies W-CSP (Wafer level Chip Size Package) had been developed as an ultimate package that enables a real chip size package and its usage in such fields has been increasing during last years.

Recently the demand of small package has been increasing in automotive electronics fields. In this fields environment and thought of reliability are different from other consumer products. Higher reliability is required than other consumer products.

In this paper we report board level reliability improvement results of stress buffer type wafer level chip size package structure that we developed ^[1] by numerical stress analysis.

2. W-CSP structure

The stress buffer type W-CSP structure had been developed. Cross sectional schematic illustration of the W-CSP structure is shown in Figure 1. The structure has a quite simple structure that consisting of stress buffer layer, copper redistribution layer, solder resist layer and solder balls. The stress buffer layer is formed with polyimide. Compared with conventional interposer type CSP structures, W-CSP has to be relax the stress that caused by the difference of the thermal

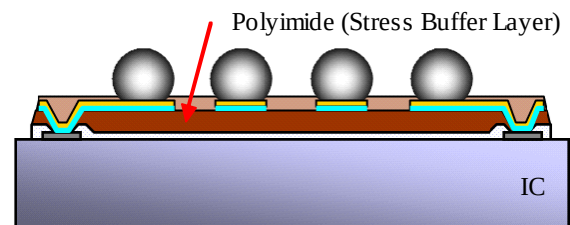


Fig.1: Cross sectional schematic illustration of the resin stress buffer type W-CSP

expansion between the chip and the substrate only with the structure that formed on the chip surface. In other words, optimizing and obtain reliable structure is more challenging than when in the conventional CSP. Therefore understanding the impact of the parameter of the structure on reliability is important to improve board level reliability. Especially, in the stress buffer type W-CSP, understanding the impact of the resin property of stress buffer layer is important, and these properties have to be optimized to improve board level reliability.

3. Evaluation the effectiveness of the resin property of the stress buffer layer

3.1 Material Property Measurement

First, the polyimide resin property was measured by dynamic mechanical analysis. Two polyimide resin; PI-A and PI-B was measured. The dynamic mechanical analysis was evaluated by SHIMAZU TRITEC 2000 dynamic mechanical analyzer. Specimens were prepared as 15 μ m thickness rectangle film. Specimen size was 10mm x 3mm. Measurement was performed in tensile mode. Measurement temperature varied from -40°C to 300°C continuously. And measurement was performed for frequency of 0.1, 1.0, and 10.0Hz.

Figure 2 shows measurement results of temperature versus storage modulus (E'), loss modulus (E''), and loss tangent ($\tan\delta$). PI-A could not be measured by 300°C due to large deformation over 260°C. Both polyimide resins showed that storage modulus was larger than loss modulus. This result indicates that these polyimide resins were elasticity

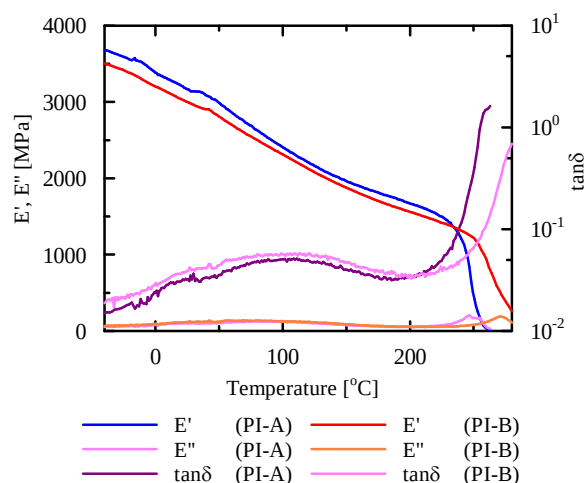


Fig.2: Measurement results of the polyimide films by dynamic mechanical analysis

dominant materials. Storage modulus was decreasing in accordance with temperature rise. There were about twice the storage modulus difference when that at 125°C compared with that at -40°C. This result indicates that these polyimide resins have high temperature dependencies. The storage modulus of PI-B was lower than that of PI-A while from -40°C to 125°C, which is the temperature range of the thermal cycle test. The peak of $\tan\delta$ existed between 270°C and 280°C in PI-B while the peak of $\tan\delta$ existed between 240°C and 250°C in PI-A. It is understood that the glass transition temperature of PI-B was about 30°C higher than that of PI-A. Highest temperature of the thermal cycle reliability test was 125°C, thus the difference of the glass transition temperature might not be had a influence on thermal cycle test result, but there was a possibility that this difference might have a influence on the residue stress after assemble when thinking of the melting point of solder to be about 220°C.

The master curve was calculated from the three different frequencies measurement results. A master curve shows the relationship between relaxation time and elastic modulus at the reference temperature. The master curve was calculated with the third order power series assuming that these materials had thermorheological simplicity^[2]. Figure 3 shows master curves at 125°C. PI-B storage modulus was also lower than PI-A when comparing it in master curve. Over more it was possible that the relaxation character was differ because relaxation curves were not parallel. From these results, PI-B might have a better stress relaxation character and might show higher reliability than PI-A.

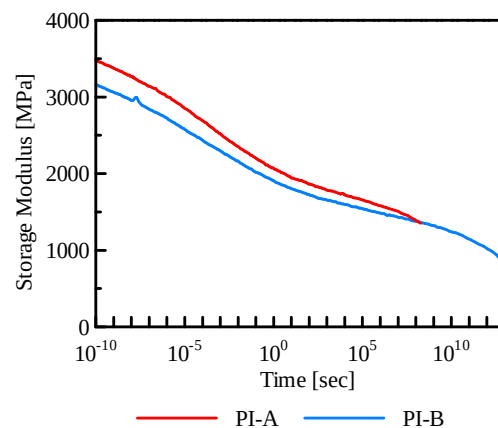


Fig.3: Master curves of two polyimide film calculated using power series

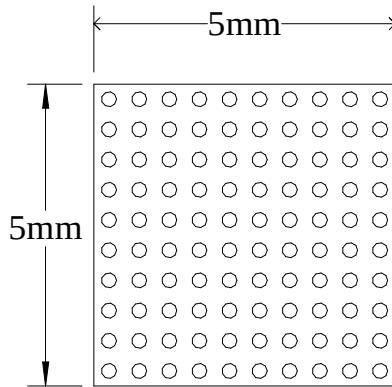


Fig 4: Schematic illustration of test vehicle

3.2 Thermal Stress Analysis considering resin material properties

To evaluate the difference of material properties between PI-A and PI-B, thermal stress analyses of W-CSP assembled on the board substrate were performed. The stress analysis model was based on actual device with die size of 5mm x 5mm. The solder ball pitch was 0.5mm. The number of solder joints was 81. Figure 4 shows the schematic illustration of the test vehicle. The solder ball diameter was 0.3mm. The solder alloy configuration considered was Sn-3.0Ag-0.5Cu. The analysis model was modeled on the FR-4 printed circuit board (PCB).

Thermal stress analysis was performed using MSC Marc 2007. 3D solid elements (8 nodes Hex) and global to local zooming technique were used. Figure 5 shows the global model and the cross sectional illustration of the structure of the local model around the solder joint. Octant symmetry technique was used in the global model to reduce the size of model. The local model of the package was consisted of Si, SiN, Polyimide, Thin Film Cu, Solder Resist, and the board was consisted of substrate and Cu electrode. Material property of the solder was assumed as a thermal plastic-elastic creep material. The plastic-elastic property was assumed as isotropic hardening rule material calculated by poly-linear approximation, and creep property was used the Norton creep law. Both plastic-elastic and creep property were considered that it had thermal dependencies. Table 1 and 2 show the material properties of solder that was used in this study. The resin were assumed as a viscoelastic material that was approximated with 10 term prony series using master curve data obtained in the previous section.

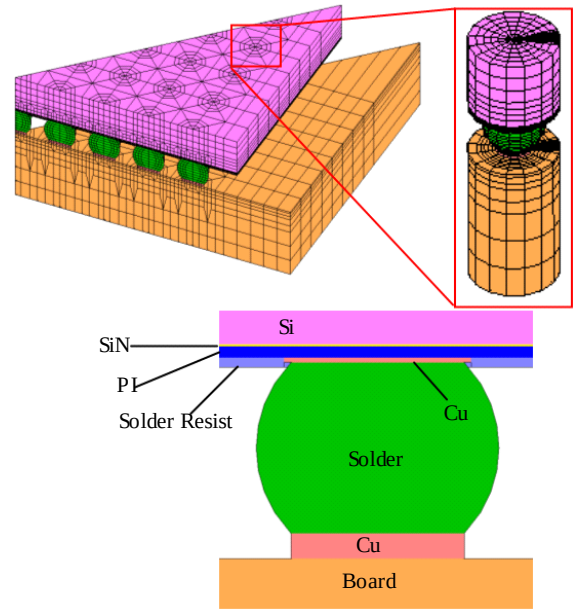


Fig.5: Simulation model and cross sectional illustration of the structure of local model around the solder joint.

Table 1: Plastic property of solder

Temperature [°C]	-40	75	125
Plastic Strain	Stress [MPa]		
0	45.79	31.75	20.03
0.0016	57.54	34.22	24.73
0.0048	67.45	36.13	26.72
0.0084	73.13	37.07	27.22
0.0214	81.09	38.28	27.77

Table 2: Creep property of solder

A (Creep Constant) [MPa/s]	n (Creep Exponent)
$0.00021 \cdot \exp(-11360/T)$	$-0.0363 \cdot T + 21.77$

T: Temperature (K)

Table 3: Other material properties

	Young's Modulus [GPa]	Poisson's Ratio	CTE [ppm/K]
Si	170	0.25	3
SiN	290	0.27	3.4
PI	Fig.3	0.3	55
Cu	131	0.35	17
Solder Resist	2.2	0.3	56
Solder	38.5	0.38	22
Board	23	0.28	15

The other materials properties used were assumed as elastic materials and these values were shown in Table 3. Symmetry boundary conditions were imposed on symmetry planes and the bottom side of the substrate was fixed at the center on the vertical direction. Cyclic thermal load was applied as shown in Figure 6. Dwell time at -40°C and 125°C was 25min, and the ramp time between -40°C and 125°C was 5min. Analysis was calculated two cycles. Analysis results were evaluated with averaged inelastic strain range of solder; within $40\mu\text{m}$ from solder edge, at the package corner, and in second cycle^[3].

Figure 7 shows calculated results of total equivalent inelastic strain range of the package side and board side. The difference of the viscoelastic properties between PI-A and PI-B obtained from thermal mechanical analysis has no significant influence on the inelastic strain range. This result indicated that the difference of the stress relaxation character between PI-A and PI-B might have no significant influence on the board level reliability.

3.3 Board Level Reliability Evaluation

In order to confirm numerical stress analysis results, the board level reliability test was evaluated with actual test vehicle. The test vehicle design was same as stress analysis model; 5mm x 5mm chip size, 0.5mm solder ball pitch, and 81pin. Reliability was tested by the thermal cycle test. Test conditions were also same as stress analysis. Interconnects state was measured by the resistance of a daisy chain trace. The failure criteria were defined when the total daisy chain trace resistance increase tenfold.

Figure 8 shows the weibull plot of the thermal cycle test result. Compared in the characteristic fatigue life (63.2% cumulative failure), PI-A showed 650 cycles and PI-B showed 800 cycles. PI-B resulted over 100 cycles higher than PI-A.

This result came from the difference of the material properties that obtained by viscoelastic measurement; the modulus of PI-B was lower than that of PI-A, because only polyimide material changed. But any significant difference obtained by previous thermal stress analyses. It indicated that there are other important material parameters that have to take into analysis models.

In addition, this result indicated that lower modulus has high stress relaxation character. The stress concentration on the solder might be decreased when the stress relaxation character of the stress buffer layer was increased, but the stress might be concentrating on the redistribution layer. Thus it is

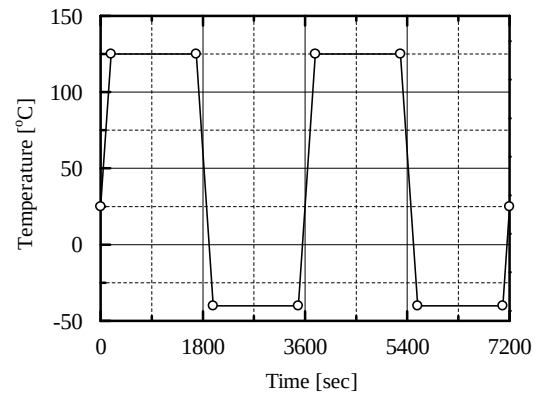


Fig. 6: Temperature profile of thermal cycle test

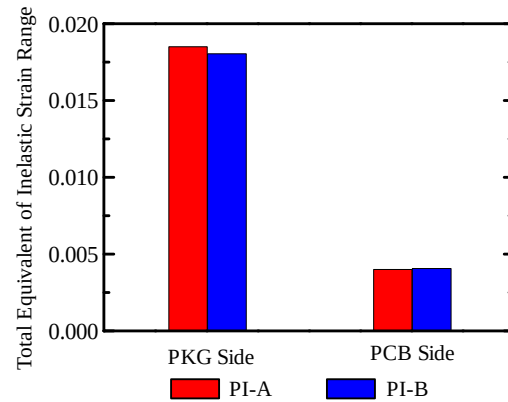


Fig. 7: Numerical analysis results of total equivalent inelastic strain range comparing two polyimide

important that the stress relaxation character was to be maintained that failure occurred by solder crack.

In addition, β (slope from the weibull plot) of the PI-A was smaller than that of PI-B. It indicates that PI-A had a wider range distribution in the fatigue life. This result might be caused by the material properties of the resins such as the difference of the glass transition point and the difference of the master curve that shown in figure 3.

Figure 9 shows cross sectional images of the solder joint which failure occurred after the board level reliability test. The failure occurred by the crack propagation at the W-CSP side along inter metallic compound interface, and there was no crack propagation observed on the board side. This result showed that the stress was highly concentrated on the package side. Thus reliability could be improved by optimizing load balance by changing the land designs, especially the ratio of the package and the board side land diameter.

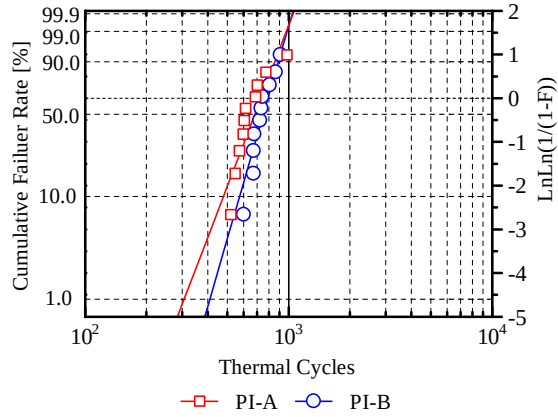


Fig. 8: Weibull plot of thermal cycle test result comparing polyimide

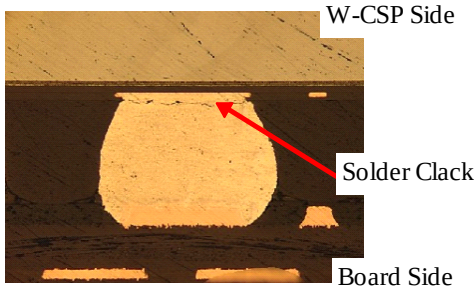


Fig. 9: Cross sectional view of electrical defected joint

4. Structure Optimization of Stress buffer type W-CSP

From the result of reliability test, the structure with PI-B was optimized. The influence of the substrate land diameters and the thickness of the stress buffer layer on the reliability were evaluated with thermal stress analysis.

4.1 Effect of the package and substrate land design

Thermal stress analysis was performed with model that the land diameter of the package (D_{PKG}) was fixed as 250 μm , the land diameter of substrate side (D_{PCB}) were changed to 250 μm , 200 μm , and 150 μm . Every condition except land diameter of substrate was as same as that of in the section 3. Results of the total equivalent inelastic strain range of the solder were shown in Figure 10. The total equivalent inelastic strain range of the package side (ϵ_{PKG}) showed larger than that of the substrate side

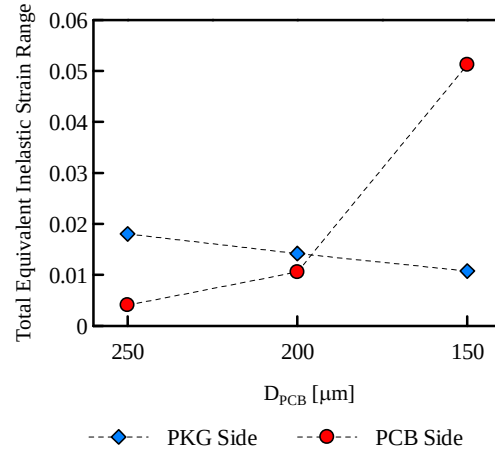


Fig. 10: Numerical analysis result of total equivalent inelastic strain range comparing substrate land diameter.

(ϵ_{PCB}) when the D_{PCB} was 250 μm . As decreasing D_{PCB} , ϵ_{PKG} was decreased almost linearly. On the other hand, ϵ_{PCB} was increased like exponentially. Especially, ϵ_{PKG} was larger than ϵ_{PCB} when the D_{PCB} was 150 μm .

Over more, the sum of the total equivalent inelastic strain range at package side and PCB side can be reduced when the balance of the stress in a solder ball was optimized by changing the substrate land diameter. It predicted that the board level reliability might be improved.

4.2 Effect of the thickness of the stress buffer layer

The effect of the thickness of the stress buffer layer to the board level reliability was evaluated. Thickness of the stress buffer layer was varied 15 μm and 20 μm . Figure 11 shows the results of ϵ_{PKG} and ϵ_{PCB} . The results showed that ϵ_{PKG} of 20 μm was lower than that of 15 μm in every land diameter. On the other hand, ϵ_{PCB} of 20 μm was almost same as that of 15 μm when D_{PCB} was 250 μm , but decreased when D_{PCB} was 150 μm . This result indicated that the balance of ϵ_{PKG} and ϵ_{PCB} depended on the stress relaxation character of the stress buffer layer that was determined by such as thickness and modulus. Thus the optimal land diameter might not be constant, might depend on the structure.

In this case, the optimal land design of both package and substrate might be 250 μm and 200 μm , respectively.

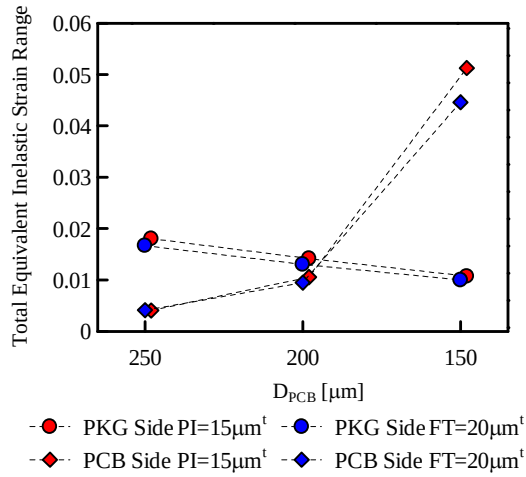


Fig. 11: Numerical analysis result of total equivalent inelastic strain range comparing substrate land diameter and stress buffer layer thickness.

4.3 Evaluation with Reliability Test

The thermal stress analysis result of the influence of land diameter and polyimide thickness was confirmed by reliability test. Test vehicle design was as same as section 3. PI-B was applied to stress buffer layer.

Figure 12 shows the result of the board level reliability test result. The characteristic fatigue life was 1500 cycles when the D_{PCB} was 200μm, improved about twice compared with D_{PCB} was 250μm. In addition the characteristic fatigue life was decreased down to 400 cycles when D_{PCB} was 150μm. Reliability of 20μm thickness was almost same when D_{PCB} was 250μm, and gradually improved in accordance with D_{PCB} decreasing. The influence of the land diameter was greater than that of the stress buffer layer thickness.

Figure 13 shows the cross sectional images of the solder bump where the failure occurred. As the result of thermal stress analysis, the crack was propagated at the board side when D_{PCB} was 150μm and at the package side when D_{PCB} was 200μm.

These results showed good correlation with numerical stress analysis.

5. Conclusion

The effectiveness of the stress buffer layer type W-CSP structure was evaluated. Board level reliability was optimized by modifying the structural properties such as material properties, film thickness, and land diameter. Thermal stress analysis considering resin properties was effective to optimize

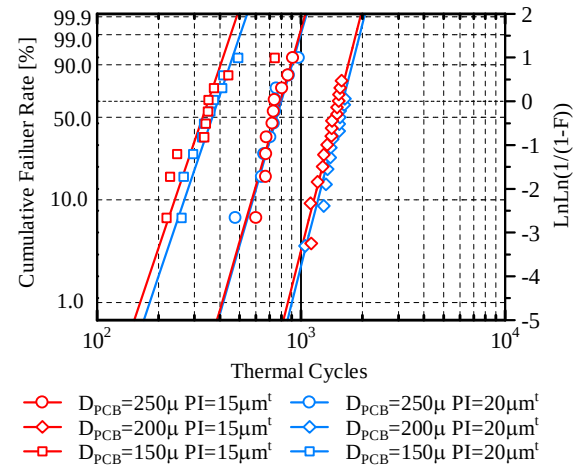


Fig. 12: Weibull plot of thermal cycle test result comparing substrate diameter and stress buffer thickness

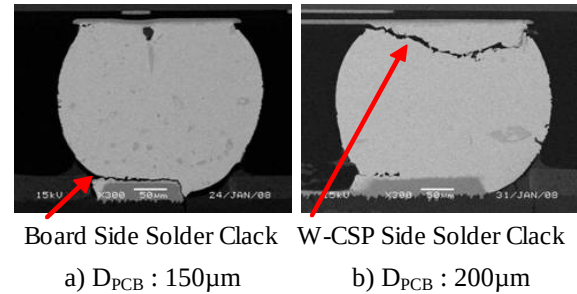


Fig. 13: Cross sectional view of electrical defected joint

the structure. As the result, we improved the board level reliability twice higher than the original structure. This reliability was applicable to the automobile applications. Furthermore, there was a possibility that obtain enhanced reliability by modifying the material and structure.

Even there are some unknown factors that have influence on reliability. We will improve the analysis model to obtain higher reliable package structure.

6. References

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