

Challenges in Cavity-Down Thermally Enhanced Packages Containing Low-k Dies

Chu-Chung (Stephen) Lee¹, TuAnh Tran¹ and Yuan Yuan²

Freescall Semiconductor Inc.

1: 6501 William Cannon Drive West, MD: TX30-OE21: Austin, TX 78735

Stephen.chuchung.lee@freescall.com, TuAnh.Tran@freescall.com

2: 7700 West Parmer Lane, MD: TX32-PL49, Austin, TX 78729

Yuan.yuan@freescall.com

The cavity-down thermally enhanced package such as Tape Ball Grid Array (TBGA) has the best thermal performance among the wire bonded packages because the silicon is attached directly onto a thick internal heat spreader. However, the TBGA package structure generates challenges in passing industrial-level package qualification requirement, especially for temperature cycling test under JEDEC condition C (-65/150C) for packages containing low-k silicon. Low-k interlayer dielectric (ILD) material usually has the dielectric constant k of less than 3. 3D finite element model simulations were performed to analyze the stress distribution in the low-k die area when the structural parameters in the cavity-down package structure were modulated. The simulation result explained as to why the TBGA package is more susceptible to failures in temperature cycling tests. Additionally, mechanical analyses were performed to identify the weakest adhesion interface within the stack of the back-end-of-line (BEOL) in the low-k die. The theoretical explanation was validated with experimental data. Corrective actions on how to handle low-k silicon in the TBGA package will be discussed.

Key words: TBGA, Thermally enhanced packages, Mechanical simulation, Low-k, Cu wafers

Introduction

Traditional wafer process integration using fine lines of aluminum alloy metallization and fine spaces of SiO₂ dielectric material can no longer provide the electrical resistance and parasitic capacitance performance to meet the demand of high speed IC's today. High electrical resistance and capacitance will result in high RC delay, increased crosstalk between adjacent metal lines and increased voltage drop. New fab process integration uses copper metallization and low-k dielectric material to resolve the performance limitation of aluminum interconnect technology. The electrical resistivity of aluminum is 3.3 $\mu\Omega\text{-cm}$ whereas the electrical resistivity of copper is 1.68 $\mu\Omega\text{-cm}$. Replacing aluminum with copper interconnect will significantly reduce the power loss due to resistivity and improve the heat dissipation. The dielectric constant of SiO₂ is 4.1, whereas the dielectric constant of low-k dielectric material is less than 3.0. Replacing SiO₂ with low-k dielectric material will reduce the parasitic capacitance between the fine metal lines.

However, the low-k dielectric material used as part of copper wafer process integration has intrinsically weaker mechanical properties as compared to SiO₂ dielectric material. Furthermore, the low-k dielectric material has substantially weaker adhesion strength to neighboring barrier films as compared to SiO₂ dielectric material to its neighboring barrier films. Table 1 summarizes the comparison of key mechanical properties of SiO₂ and low-k dielectric materials. The two major weakness of the low-k material, which are the inherently weaker bulk mechanical and fracture-strength properties, and lower interfacial adhesion strength in the silicon stack-up, pose significant challenges to downstream wafer testing and packaging process and material selection [1, 2, 3, 4 and 5].

Table 1: Mechanical Properties of Dielectric Materials

Material	CTE (PPM/°C)	Flexural Modulus (GPa) at 25°C	Hardness (GPa)	Adhesion to Barrier Films (J/m ²)
SiO ₂	0.55	80	9	15

($4 < k < 3$)				
Low-k ($3 < k < 2.5$))	15	8	2	5 - 6

Figure 1 illustrates the cross-section of cavity down Tape Ball Grid Array package (TBGA using polyimide tape-based substrate). TBGA substrate is based on a one-metal layer or multiple-metal layers laminated on a polyimide tape which is attached to an internal heat spreader. The silicon is attached directly onto the internal heat spreader, thus providing an excellent thermal performance in terms of low thermal resistance between silicon junction and package case (i.e. Theta-jc). The package encapsulation is generally accomplished by using the glob top process instead of the over-molding process. Other thermally enhanced package designs for wire-bond parts are usually cavity up and the heat cannot be transferred as sufficiently as TBGA packages. However, TBGA package seems to challenge the electronic packaging industry in general in its capability to pass temperature cycling (TC) tests when the silicon contains low k ILD [1]. When non-low k dies is used, TBGA can pass Temperature cycling tests as well as cavity up thermally enhanced packages. In using low-k die in TBGA, the failure mode has primarily been cracks generated at low k ILD layers near the metal 1 and metal 2 regions of the back-end-of-line structure of the silicon.

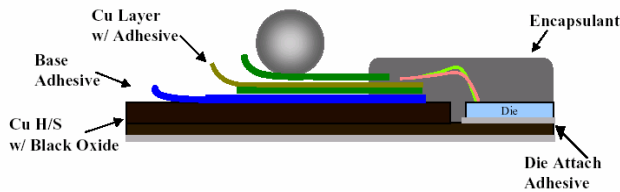


Figure 1: Tape Ball Grid Array (TBGA) Package Components

We believed that the unique cavity-down configuration created a higher stress generated at the top portion of the die where the low-k layers are located. This mechanical stress exceeds the low fracture strength of the low-k structures, resulting in cohesive or adhesive failures. These failures are manifested as crack lines initiating from the die edge propagating into the dielectric layers or delamination along the interfaces. This paper intends to explain the reason as to why TBGA package can present a very unique stress distribution along the die edge. A

detailed discussion on the delaminated interface will also be provided.

Experimental Approach

Finite element model simulation was performed to obtain the stress distribution at the silicon region inside the TBGA package in order to understand the reason why TBGA can fail low k dies more often than other cavity up thermal enhanced packages. Full functional devices fabricated in 90 nm MOSFET (metal-oxide-semiconductor field-effect transistor) technology were packaged into the TBGA package to collect temperature cycling reliability data and to further validate the simulation results.

A FIB (Focused Ion Beam) technique was performed at the damaged low k ILD region at the edge of the die after failing temperature cycles, and SEM (Scanning Electron Microscopy) was then used to inspect the damaged area. Moreover, TEM (transmission electronic microscope) was used to further inspect the actual delaminated interface at the damaged region.

Results and Discussions:

I. Finite Element Model Simulation:

3-D quarter symmetric Finite Element Models (FEM's) were created to emulate the major package structural features. A typical model is shown in Figure 2 and Figure 3.

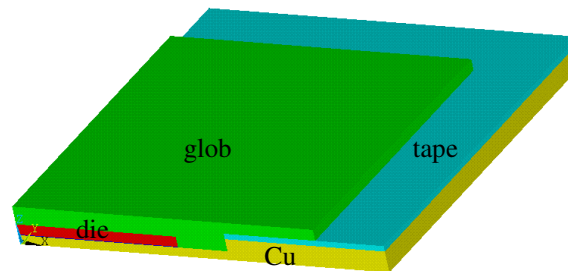


Figure 2: Quarter Symmetric 3-D Package Model

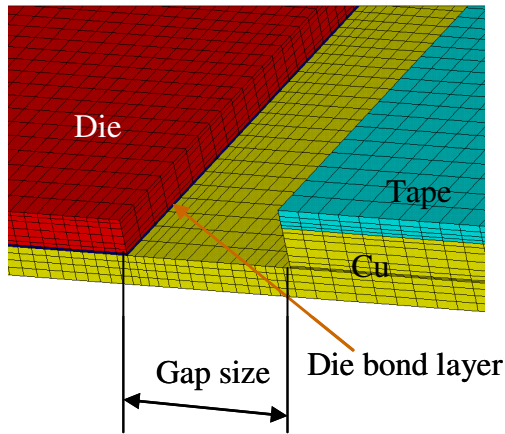


Figure 3: Package Local View and FEM Mesh (viewed without glob)

Note: The gap size is the distance between the die and the edge of substrate cavity. The gap size is denoted as “D” in the mechanical simulation discussion.

The typical package geometries are:

- Package size = 40 mm x 40 mm
- Cavity size = 15.3 mm x 15.3 mm
- Die size = 13.8 mm x 13.8mm
- Die thickness = 0.28mm (11 mil)
- Glob height (above the die) = 0.35 mm
- Glob area = 22 mm x 22 mm
- Tape thickness (including Cu routing layer and solder mask) = 0.2 mm

In the FEM model, the tape layer includes the polyimide tape, its associated adhesive layers, routing layer and solder mask layer. The layers are smeared together as one layer with material properties averaged from all the associated layers.

The simulation analysis result indicated that during temperature cycling tests the existing TBGA package created an off-plane “tensile stress (S_z) on top of the die where ILD stacks are located. The stress at the die corners and edges is especially notable. A typical off-plane stress distribution is shown in Figure 4.

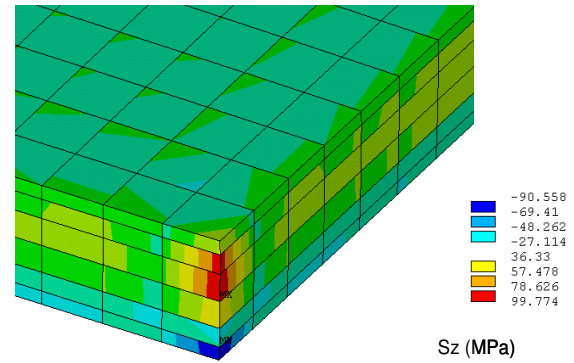


Figure 4: Typical off-plane Stress S_z Near Die Corner

Effect of Gap Distance between Die and Cavity:

The next set of simulation was to understand the impact of the gap distance between the die and the cavity wall (shown in the Figure 5) to the stress at the die top corners and die top edges. A series of simulations were performed for squared die with side of 14.2 mm, 13.6 mm, 13.0 mm, 12.4 mm and 11.8 mm. The corresponding gap distance is 0.55 mm, 0.85 mm, 1.15 mm 1.45 mm and 1.75 mm, respectively.

Particular attention was focused on the stress component S_z (off-plane stress) and the maximum principal stress S_1 because these stresses are most likely linked to the observed failure mode. The maximum off-plane stress S_z and the maximum principal stress S_1 for the element at the top of the die corner are shown in Figure 5.

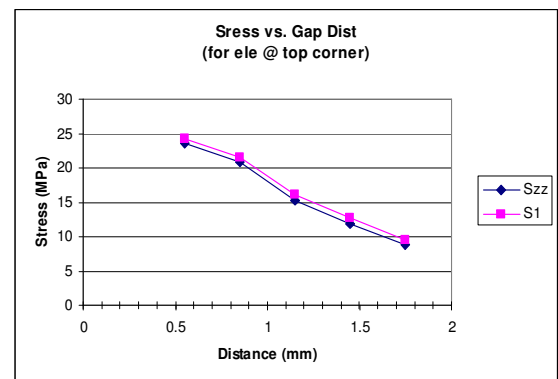


Figure 5 : Effect of Gap Distance to S_z and S_1 Stresses

Both S_z and S_1 decrease as the gap distance increases. Therefore, increasing the distance between the die and the cavity is expected to reduce the failure rate in temperature cycling. It is worth

mentioning that our purpose is NOT to reduce the stress to zero. Increasing the gap distance will also increase the wire length, which in turn will have adverse effect on wire sweep performance and electrical performance due to long wires. For practical application, the stresses only need to be reduced below the threshold of S_z and S_1 . The experiments described in the subsequent section are to determine the threshold gap distance necessary to reduce the failure rate to zero.

II. Validating Finite Element Simulation Results

The simulation model result highlighted two important factors affecting the temperature cycling performance of low-k dies in TBGA package. One factor is the tensile stress applied at the die edge and die top corner; and the other is the die-to-cavity distance affecting the magnitude of this tensile stress. The tensile stress applied to the die edge and die top corner is very unique to the TBGA package since similar FEM simulation for cavity-up BGA has predicted a compressive stress applied to the die edge and die top corner. Since the tensile stress is applied at the die edge, a “low stress” glob top material for TBGA packages is required in order to reduce the possibility of delamination between layers at the die edge.

The test wafer was made with Freescale’s CMOS (Complementary Metal Oxide Semiconductor) 90-nm technology. The test die has a die size around 36 mm², and its structure has 6 copper metal layers with one thick copper layer as the final copper metal layer. The ILD material has a k value around 2.9. Four TBGA substrates with different cavity sizes were designed and fabricated in order to validate the effect of the die-to-cavity-edge distance on the die-edge-tensile stress. Four die-to-cavity distance D values were evaluated, 1x, 1.8x, 2x and 6.5x, respectively. The D value marked as 1x is the current production’s minimum clearance specification for the die-to-cavity-edge distance. The 1.8x of D value means the evaluated die-to-cavity distance is 1.8 times the current production’s minimum clearance specification.

The TBGA packages were processed through the normal TBGA assembly production flow, which includes wafer singulation, die attaching and die attach curing, wire bonding, dam and glob top encapsulation and glob top curing, solder ball attachment and package singulation. Parts were subjected to MSL3/260 degrees C preconditioning followed by air-to-air temperature cycling condition C (-65 to 150 degrees C). Ultrasonic scanning test was performed on all parts at temperature cycling read points of 100, 200, 500, 750 and 1000 cycles.

The failure was defined as an occurrence of delamination in the die region detected in C-mode acoustic microscopy (CSAM). Failure analysis cross sectioning and/or focused ion beam (FIB) was performed to further identify the specific delaminated interface.

(A) Validating the Effect of Gap Distance between Die and Cavity:

Four TBGA substrates with different cavity sizes were designed and fabricated in order to validate the effect of the die-to-cavity-edge distance on the die-edge-tensile stress.

The glob top material used in this study was the material whose mechanical properties have been used in the mechanical simulation model. This particular glob top material, denoted as glob top A in the discussion, is the current production material used for non-low-k die and is considered as a high stress glob top material. The CSAM results after various temperature cycling read-points are summarized in Table 2.

Table 2: CSAM Results after Temperature Cycling from Four Die-to-Cavity-Distance.

Result is listed as the number of failed units out of the total quantity of tested units.

D	To	MSL3/ 260	TC 100	TC 200	TC 500	TC 750	TC 1000
1x	0/20	8/20	n/a	n/a	n/a	n/a	n/a
1.8x	0/20	0/20	0/20	0/20	0/20	0/20	0/20
2x	0/20	0/20	0/20	0/20	0/20	0/20	0/20
6.5x	0/20	0/20	0/20	0/20	0/20	0/20	0/20

From Table 2, eight out of 20 units using the current die-to-cavity distance specification (i.e. 1x) and the current glob top material has low-k ILD delamination after MSL3/260 preconditioning based on the CSAM inspection. An example of CSAM image showing the low-k ILD delamination is shown in Figure 6. The dark region in the sonic scan spectrum indicates a phase shift of the ultrasonic frequency when the ultrasonic wave penetrates the package from the glob top side to the bottom of the copper heat sink. A special mathematical algorithm in the sonic scan system will automatically change the grey scale color when a phase shift is encountered as indicative of the delaminated region. The exact delaminated interface cannot be determined by ultrasonic technique and can only be identified by subsequent cross section.

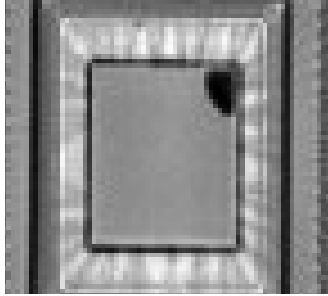


Figure 6: CSAM Example of TBGA Failed Part due to low-k ILD Delamination

Figure 7 indicates that the delaminated interface is located in the corner of the die. This finding agrees with the mechanical simulation prediction in that a “tensile” stress is exerting on the die corner, making the die corner more vulnerable to the delamination damage than other regions of the die during temperature cycling test.

When the die-to-cavity distance D value increases to 1.8 times the existing distance specification, all units were capable of passing MSL3/260 and 1000 cycles of temperature cycling even though the existing production glob top material which is considered to be a high stress material was used. However, the D distance cannot be increased freely because of the increase in the wire length. As a result, both the resistivity and self inductance for each wire increase leading to poor electrical performance of the whole package system. Additionally, longer wire length can cause wire sweep during molding process, thus reducing the assembly yield. In short, increasing the die-to-cavity distance in TBGA package in order to pass temperature cycling test should be considered in conjunction with assembly and electrical impacts.

(B) Validating the delaminated interface

In order to determine the specific delaminated interface that failed after temperature cycling, ion mill cross-sectioning was performed on failed samples. As shown in Figure 7, the delaminated interface was identified to be the separation between Metal 1 (M1) and Via 1 (V1) layers.

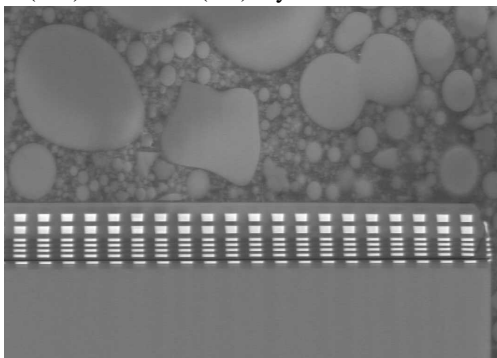


Figure 7: FIB Cross Section Showing low-k ILD Delamination due to Package Stress

It is worth noting that mechanical cross-sectioning could introduce additional damage to the low-k region within the die. An example of mechanical cross-sectioning process damaging low-k dies by is illustrated at Figure 8.

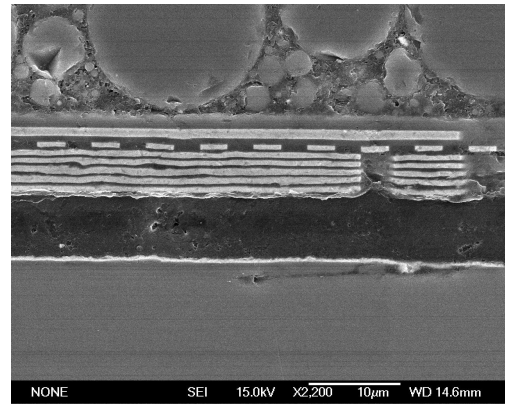


Figure 8: Mechanical Cross Section Showing low-k ILD Delamination due to Mechanical Cross Sectioning Technique

This particular part was not submitted to any temperature testing and did not show any sign of delamination through CSAM. The mechanical cross-sectioning had generated a gap as wide as 8 μm in the low-k region. Therefore, care needs to be taken while performing failure analysis on packages containing low-k dies. It was found that the best result can be achieved by thinning down the package and leaving a thin layer of encapsulation material above the die before performing FIB (focused ion beam) and/or ion milling at the delaminated area.

(C) Mechanical stress analysis for actual delaminated interface

The actual delaminated interface cannot be clearly identified based on SEM photos due to the limitation of maximum magnification of SEM technique as shown in Figure 8. Therefore, TEM was performed to further isolate the delaminated interface, as shown in Figure 9.

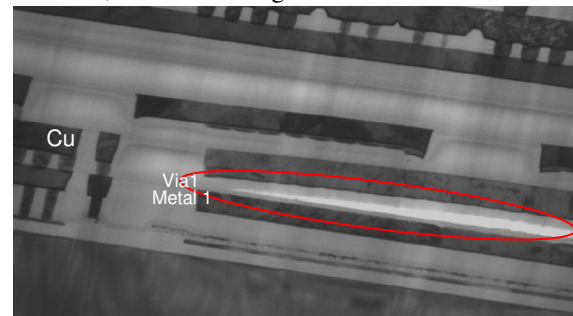


Figure 9 (a): TEM picture showing the delaminated interface as circled in red. The

delaminated interface is located between Via1 and Metal 1 region.

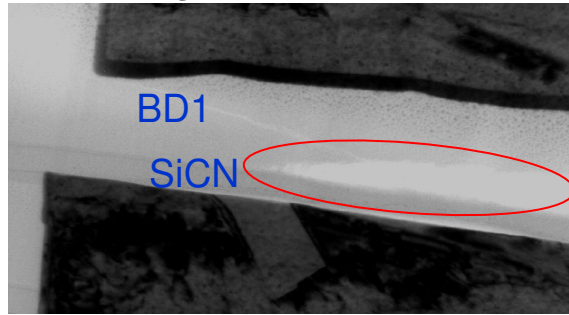


Figure 9 (b): Close up TEM picture at the delaminated interface showing the actual delaminated interface between SiCN and BD1 (Black Diamond 1) at the Via 1 layer.

The delaminated interface is between Via1 and Metal 1 layers and has been clearly shown in Figure 9(a), where the red circle is marked. The actual delaminated interface is indeed located at Via1 layer region, and is between black diamond ILD layer (BD1) and glue layer of SiCN as shown in Figure 9 (b). The stacking sequence for Freescale C90 structure is schematically shown in Figure 10 [2]. The largest CTE mismatch interface can be found in two areas, which are (a) the interface between LM-2 ILD (one layer below the last ILD layer as marked at Figure 10) and LM-3 ILD layers (the last low k ILD layer counting from the bottom of ILD layer), and (b) the interface between M1 ILD (metal 1 ILD layer which is located at the bottom of the BD1 layer) and Contact ILD layer. The last thick layers generally use SiO₂ as ILD material, while contact layer uses doped SiO₂ as ILD material. The stress applied at interface of LM-2 and LM-3 is not as large as compared to that of M1 and contact ILD layer because the thickness of LM-3 ILD layer is greater than LM-1 ILD layer. For example, for the same amount of displacement, the thicker ILD layer can experience a smaller amount of strain which is defined as displacement divided by ILD thickness. Therefore, it is likely to have higher stress at the Metal 1 ILD interface. However, the adhesion strength between Metal 1 ILD and contact ILD layer is much stronger than Via1 ILD and M1 ILD layers. Therefore, the delaminated interface is found more frequently at Via1 ILD layer between SiCN and BD1 layers.

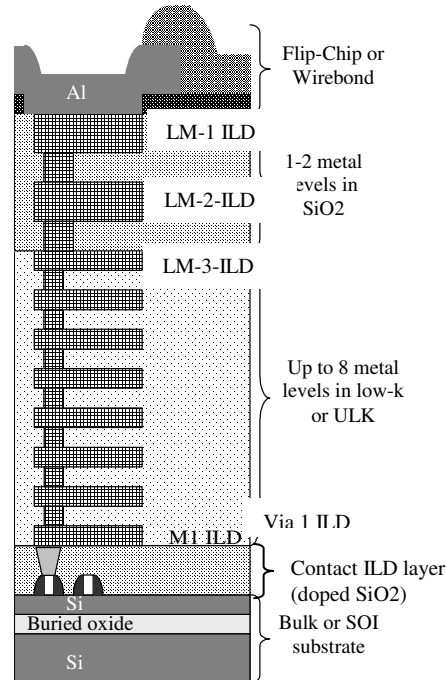


Figure 10 [2]: Schematic drawing of cross section of die using C90 or C65 technology

Conclusions and Future Works

The unique package construction of the cavity-down TBGA poses significant challenges in packaging low-k silicon that has lower fracture strength. The main learning from the TBGA development is the followings:

- (1) Because of the tensile stress applied to the die corner where low-k BEOL stacking is located, the TBGA package is more susceptible to failures in temperature cycling tests than other types of BGA packages. The die-to-cavity distance has an important impact on the level of tensile stress onto low-k die. The greater the die-to-cavity distance is, the lower the tensile stress is observed on the die edge. Both mechanical simulation model and experimental data have proven this hypothesis.
- (2) The increase in die-to-cavity distance will increase the wire length resulting in both wire sweep yield loss and poor package-level electrical performance. Therefore, increasing the distance between die to cavity edge must take manufacturability into account.
- (3) The weakest interface of low k dies using 90nm technology when being submitted to temperature cycling stress tests is located at Metal 1 and Via 1 ILD layers. Indeed, it is highly likely to be found between glue layer and BD1 layers at Via 1

ILD region where the CTE mismatch is largest among the C90 BEOL stack.

(4) Methods of qualifying TBGA with dies using C90/ C65 technologies have been found in previous works [5] by using new reformulated low stress glob top materials.

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