

## Overcoming Challenges in Thermally Enhanced BGA Packaging with Low-k Silicon

Tu Anh Tran<sup>1</sup>, David Dorinski<sup>2</sup>, Simon Gonzales<sup>2</sup>, Phong Vu<sup>2</sup>, Ron Weberg<sup>2</sup>  
 Freescale Semiconductor, Inc.

1: 6501 William Cannon Drive, Austin TX 78735

[Tu.Anh.Tran@freescale.com](mailto:Tu.Anh.Tran@freescale.com)

2: 1300 North Alma School Road, Chandler, Arizona 85224

[David.Dorinski@freescale.com](mailto:David.Dorinski@freescale.com), [Simon.Gonzales@freescale.com](mailto:Simon.Gonzales@freescale.com),

[Phong.Vu@freescale.com](mailto:Phong.Vu@freescale.com), [Ron.Weberg@freescale.com](mailto:Ron.Weberg@freescale.com)

### Abstract

All market segments continue to put cost pressure on semiconductor and packaging suppliers in order to stay competitive. Reducing silicon area while providing more silicon functionalities increases potential die count per wafer and lowers the die cost. Staying in wire bond packaging instead of migrating to flip chip packaging further provides a cost competitive advantage. Wire bond packaging for silicon devices has been the backbone of the semiconductor industry to serve communications and networking customers for many years. Innovative interconnect routing and IC design and fine pitch wire bonding capability enable silicon to have 900 bonding pads in an area of 60mm<sup>2</sup>. The high wire count and wire density is unprecedented in thermally enhanced plastic ball grid array (PBGA) packages with an internal heat spreader, which is commonly denoted as TE-PBGA-II. With the further shrink of the silicon dimension, the Low-k inter-layer dielectric (ILD) material has been widely used to replace the traditional SiO<sub>2</sub> ILD in order to reduce the interconnect delay. Low-k dielectric by definition has a dielectric value of less than 3. The introduction of Low-k ILD material into the silicon process imposes new challenges for high wire density packaging. In particular, the inherently weak adhesion in the Low-k interconnect makes the silicon more susceptible to a failure mode called ILD crack or delamination that causes electrical failure during temperature cycling stress testing. This paper will discuss the challenges and resolution during the packaging development for Low-k products with high wire density in large 31x31 and 35x35mm TE-PBGA-II packages. Challenges range from wafer dicing through difficult test structures in the scribe streets, die attach fillet height control, wire bonding on Low-k bond pads, and molding Low-k silicon in a large package. Alternative methods including Finite Element Modeling and extended package reliability testing were used to demonstrate the robustness of the Low-k packaging solution.

Key words: Low-k dielectric, TE-PBGA, ILD delamination, dicing, die attach fillet height, mold compound filler

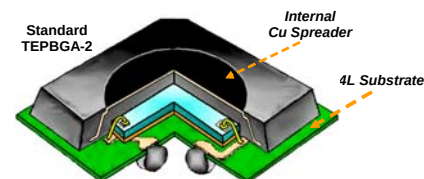
### Introduction

This paper presents a collection of process improvements related to the assembly of a 90nm CMOS device in a Thermally Enhanced Plastic Ball Grid Array with an internal heat spreader, which is commonly denoted as TE-PBGA-II (Figure 1). For this given technology introduction, TE-PBGA-II package with wire bonding was chosen based on the die size, thermal dissipation, and cost value. TE-PBGA-II package was used as an alternate over a flip-chip package with a larger die size as a cost competitive advantage for assembly and integration [1 and 2]. In addition to the above, an internal heat spreader was included in TE-PBGA package which offers thermal transfer from the die to the external environment for added heat transfer performance. TE-PBGA-II package can be 200% to 300% less costly than the flip chip equivalent package. This package type is typically used in applications that require high I/O counts, mid level cost structure, and mid level thermal performance. Customer end use applications are varied. The end use of the packages within this paper include a 600+ ball count TE-PBGA-II with an external heat sink mounted to the embedded heat spreader combined with 200 linear feet per minute (LFM) airflow that is designed to dissipate 5+ watts. A second application is a 400 plus ball

count TE-PBGA-II package without external heat-sink and zero LFM airflow that is designed to dissipate 3+ watts.

The challenge of TE-PBGA-II packaging is the intrinsic material properties including silicon, die attach, mold compound, heat spreader, and the integration of such materials. This includes property effects from thermal and mechanical stresses, and material mismatch that contributes to the integration of these materials into a final package configuration. Subsequently, when TE-PBGA-II package operates under normal thermal cycling conditions or during reliability stress, such material components can lead to delamination, cracking, or other attributes that result in electrical failures [3].

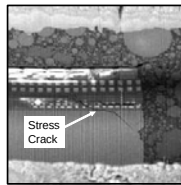
**Figure 1:**  
**Standard**  
**TE-**  
**PBGA-II**  
**Cross**  
**Section**



Within the regime of TE-PBGA-II packaging is the consideration of a Low-k inter-layer dielectric (ILD) used in the back-end-of-line (BEOL) manufacturing process of the

silicon. The Low-k material adds a porous structure with high coefficient of thermal expansion (CTE), and low mechanical strength relative to SiO<sub>2</sub> interlayer dielectrics. The Low-k material interface is therefore vulnerable to the thermal and mechanical stresses during assembly. Such stresses during Moisture Sensitivity Level (MSL) preconditioning and temperature cycling have been determined to induce die corner delamination [3].

As defined by other packaging studies, the use of temperature cycling data can validate the silicon, packaging material, and packaging components for determining the reliability of the integration [4]. In this study, the failure mechanisms associated with TE-PBGA-II packaging were observed during the thermal cycling associated with reliability stressing. The failure modes included die cracking at the opposite corner of the injection point for the mold compound as shown in Figure 2. Furthermore, the increase of the die size in the package drives additional cracking forces with Low-k delamination [5].



**Figure 2:**  
**Die Cracking**  
**Cross Section**

An additional challenge with the 90nm die integration with TE-PBGA-II package was the high wire count associated with the circuit layout. The 90nm device has approximately 900 wires including multiple wire looping heights associated with the wire bond operation. The high wire count coupled with a die size of 7.5x7.5mm translates into a wire density approaching 30 wires/mm. In other words, for every millimeter of the silicon periphery, 30 wires were wire bonded. The high wire count presented several issues including, wire looping control, crossing of wires (electrical short potential) and a mechanical screen restricting the flow of the mold compound during assembly. Such restriction or screening of the mold compound affected the uniformity of the distribution of the filler material in the mold compound across the package. The reduced filler content in the mold compound increases the thermal mechanical stress on the die resulting in a cracking event during temperature cycling.

Within the paper the challenges of integrating Low-k dielectric with Cu interconnect device in TE-PBGA-II package include several process improvements at dicing, die attaching, wire bonding, and molding. The result of this study was an increase in reliability of 10X over the initial baseline performance. The associated process improvements are detailed in this paper to further support a successful integration of a 90nm die technology in an advanced TE-PBGA-II package.

### Dicing Challenges and Resolution

#### (a) Optimizing Dicing Process Parameters

The 90nm wafers were background to 200um before dicing. The first set of evaluations was to develop a dicing process that can help minimize dicing defects. It is known that dicing through 90nm Low-k wafers has produced more silicon damage, specifically BEOL Cu chipping and dielectric peeling, than was observed with previous silicon technologies. During package temperature cycling, these dicing defects can travel laterally through the die seal ring, damage the device's interconnecting circuits and cause the device to fail. Extensive

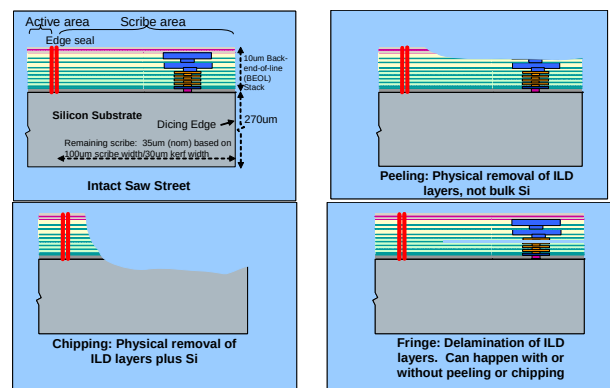
dicing technical details and Low-k dicing evaluations were covered in a previous publication [6]. Key dicing process parameters affecting the dicing quality are dicing blade type, table speed and cut depth of the Z1 blade. Table 1 summarizes the dicing design of experiment.

**Table 1: Dicing Design of Experiment**

| Cutting Mode | Blade Combination                                         | Table Speed (mm/sec) | Z1 Cut Depth (um) |
|--------------|-----------------------------------------------------------|----------------------|-------------------|
| Step Cut     | Current Z1/Z2<br>(Z1: Standard Grit /<br>Standard Width)  | 23                   | 60                |
|              |                                                           | 23                   | 80                |
|              |                                                           | 40                   | 60                |
|              |                                                           | 40                   | 80                |
| Step Cut     | New Z1/Z2<br>(Z1: Fine Grit /<br>Standard Width)          | 40                   | 60                |
|              |                                                           | 40                   | 80                |
| Single Cut   | New Single Blade<br>Z2: Standard Grit /<br>Thinner Width) | 50                   | -                 |

The dicing machine offers two cutting modes, single cut and step cut. The single cut mode uses one dicing blade to cut through the wafer and a part of the dicing tape. Single cut mode often times cannot satisfy minimal top-side chipping and back-side chipping simultaneously. Step cut mode employs two dicing blades, the first blade (Z1) cutting through a certain depth of the silicon to remove all BEOL layers and some bulk silicon, and the second blade (Z2) cutting through the remaining bulk silicon and a part of the dicing tape. As such, Z1 and Z2 blades can be designed independently in order to achieve best dicing quality for the top and bottom sides of the wafers. In this experiment, both step-cut and single-cut modes were examined. For the step-cut mode, two Z1 blade types were evaluated while the Z2 blade type was held constant. The current Low-k Z1 blade was a Ni bond diamond blade with a standard grit size and a standard blade width. The new Low-k Z1 blade was designed with a finer grit size and a standard blade width. In the single-cut mode, a single blade was designed with a standard grit size but with a thinner blade width. The process window of the table speed is listed in Table 1. The Z1 cut depth is the amount of silicon depth being diced through by the Z1 blade.

The dicing results included optically inspecting and counting the instances of top side peeling and/or chipping of 2 die reticles on a wafer, and taking Scanning Electron Microscopy (SEM) micrographs of specific die corners with the most severe chipping. For the 90nm device being diced, there were 12 die per reticle on the 300mm wafer. The two reticles randomly selected for inspection were one reticle located on the center of the wafer and the other reticle close to the edge of the wafer. Therefore, the sampling size of the optical inspection for top die peeling/chipping is 24. Figure 3 provides the definition of Low-k top-side peeling and chipping observed during dicing.

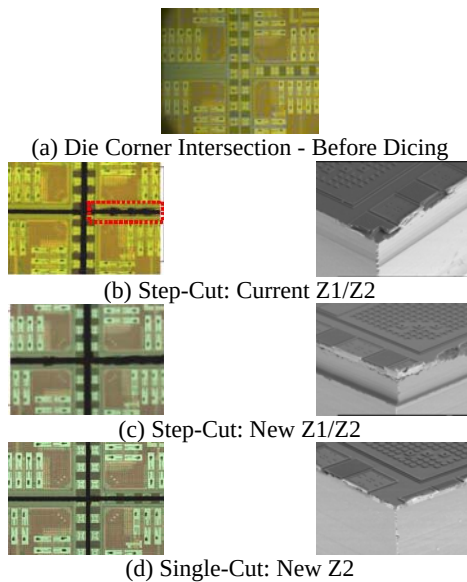


**Figure 3: Low-k Top-Side Dicing Defect Description**

Table 2 tabulates the dicing inspection results. In the column “Top Side Peeling”, the higher ratio indicated the worse dicing quality was obtained. The dicing quality was further assessed by close-up SEM inspection of the die corners. Representative optical images and SEM images of top-side peeling are shown in Figure 4. Figure 4(a) shows a die corner known for difficult dicing; Figures 4(b), 4(c) and 4(d) are examples of dicing results of this particular die corner from different blades.

**Table 2: Dicing Inspection Results**

| Cutting Mode | Blade Combination                                  | Table Speed (mm/sec) | Z1 Cut Depth (um) | Top Side Peeling | Temp Cycling (-55C/ 125C) |
|--------------|----------------------------------------------------|----------------------|-------------------|------------------|---------------------------|
| Step Out     | Current Z1/Z2 (Z1: Standard Grit / Standard Width) | 23                   | 60                | 14 / 24 (59%)    | Not Pursued               |
|              |                                                    | 23                   | 80                | 20 / 24 (83%)    | Pursue                    |
|              |                                                    | 40                   | 60                | 7 / 24 (29%)     | Not Pursued               |
|              |                                                    | 40                   | 80                | 9 / 24 (38%)     | Not Pursued               |
| Step Out     | New Z1/Z2 (Z1: Fine Grit / Standard Width)         | 40                   | 60                | 7 / 24 (29%)     | Not Pursued               |
|              |                                                    | 40                   | 80                | 5 / 24 (21%)     | Not Pursued               |
| Single Out   | New Single Blade Z2: Standard Grit / Thinner Width | 50                   | -                 | 2 / 24 (8%)      | Pursue                    |



**Figure 4: Optical and SEM Images per Dicing Blade Combination**

The current Z1 blade (standard grit size / standard width) produced the worst top side peeling/chipping. SEM inspection of the dicing quality revealed an inconsistent die edge chipping and peeling produced by the current Z1 blade. The best dicing quality was obtained by the new single-cut blade (standard grit size / thinner width). The thinner blade showed marked improvement over the current Z1 blade in terms of top side peeling, edge peeling and die edge chipping. Samples from the worst and best dicing cells were subsequently processed with the standard 90nm assembly process and materials and subjected to package-level temperature cycling.

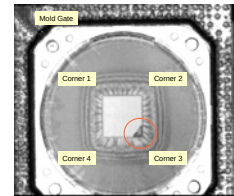
The package reliability test began with Moisture Sensitivity Level 3 (MSL3) preconditioning (bake at 125°C/24 hours, moisture soak at 30°C, 60%RH for 192 hours, and 3 cycles of forced air convection reflow at 225°C). After MSL3 preconditioning, parts were subjected to Air-to-Air Temperature Cycling (-55°C to 125°C) for 200 and 500 cycles.

After 200 cycles of temperature cycling, two groups experienced a high level of electrical opens and shorts failures, reaching a 25,000 PPM level. Mapping of the failed pins

indicated that the failed pins were located in the corners of the die. C-mode Scanning Acoustic Microscopy (CSAM) of the failed packages showed a large delamination in the failed die corners. Furthermore, 80% of the failures exhibited electrical failures and CSAM delamination in the die corner opposite to the mold injection gate.

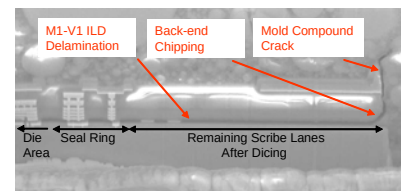
The CSAM image of a failed package is shown in Figure 5. In Figure 5, the mold injection gate is on the top left. The corner corresponding to the mold injection gate is designated as Corner 1. The corner diagonally opposite to the mold gate corner is Corner 3. Figure 5 represents a CSAM image of a package with a large delamination detected in Die Corner 3.

**Figure 5: Die Corner 3 Delamination Detected by CSAM**

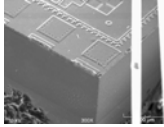


Several failed packages were submitted to failure analysis to determine the nature of the delamination and the linkage between the delamination and the electrical failing signature. The best failure analysis method for interfacial delamination in Low-k devices is to thin down the package's mold compound, leave a thin layer of mold compound above the die and perform Focused Ion Beam (FIB) cross sectioning or ion milling at the delaminated area [7]. Figure 6 shows the FIB cross-section diagonal across Corner 3 of a failed device. The delamination detected by CSAM method was found to be an interfacial delamination between Metal 1 (M1) and Via 1 (V1) layers of the BEOL stack of the device. This delamination started at the die edge, propagated laterally across the remaining scribe lane, broke through the die seal ring designed to protect the die, broke through the vias as parts of the active interconnection, and consequently rendered the signal pin non-functional. A back-end chipping was also found at the die edge where the M1\_V1 delamination initiated. Two additional delaminated areas were found, a vertical interfacial delamination between the mold compound and the die side, and a 45-degree angle crack in the mold compound.

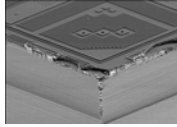
**Figure 6: M1-V1 Delamination Propagating from Die Corner into Active Die Area**



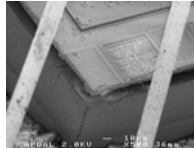
Several packages were de-processed and inspected for dicing-related defects such as top side peeling and chipping. Figure 7 shows SEM examples of passing die corners 3 devices (Figures 7(a) and 7(b)) and failed die corners 3 devices (Figures 7(c) and 7(d)). The gap between BEOL and bulk Silicon in the SEM images in Figures 7(c) and 7(d) is an exaggeration of the M1-V1 delamination (similar to Figure 6) resulted from the failed packages being subjected to the de-processing chemicals. The amount of top side peeling was similar among the passing and failed corners. There were failed devices that did not exhibit any top side peeling/chipping or had minimal dicing defects. This observation entailed that the high level of die corner failures was not due solely to top-side peeling or chipping.

**PASSING DEVICES**

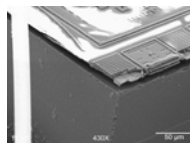
(a) No Dicing Defect



(b) Slight Top Side Peeling on Test Structure

**FAILING DEVICES**

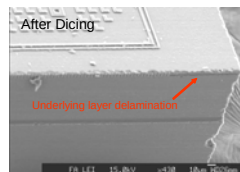
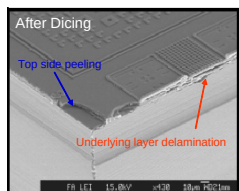
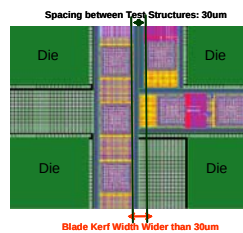
(c) No Dicing Defect



(d) Slight Top Side Peeling on Test Structure

**Figure 7: Dicing Quality in Passing Die Corners and Failed Die Corners****(b) Changing Dicing Alignment on Scribe Lane**

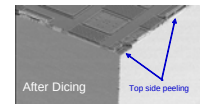
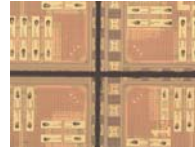
Further investigation revealed that the 90nm device used for the assembly development had a single-scribe lane in the horizontal direction and a double-scribe lane in the vertical direction. In Figure 8, there were two vertical banks of Scribe Grid Production Control (SGPC) bond pads in the double-scribe lane at this intersection. SGPC pads are used during the wafer fabrication to monitor the wafer-level process control. The SGPC bank is generally over 4mm long and consists of more than 20 pads. The SGPC pads are designed with bond pads at each BEOL metal layer connected with series of vias. The SGPC bank is therefore high in copper density, approaching 80% at each metal layer. When the dicing is aligned on the center of the single-scribe lane, the dicing blade cuts across the high copper density SGPC pads. When the dicing is aligned centered on the double-scribe lane, the dicing blade cuts between two columns of SGPC pads. The low copper density spacing between two high copper density columns of SGPC pads was designed at 30um, which is narrower than the combination of the kerf width and positional tolerance of any dicing blades under evaluation.

**Figure 8: Narrow Spacing for Dicing on a Double Wide Scribe Lane with SGPC Structures****Figure 9: Underlying Layer Delamination Observed When Dicing between SGPC Banks**

Dicing in the narrow spacing between SGPC banks produced a drastic change in the copper loading at the center of the blade and on the edges of the blade. A more thorough inspection of the dicing quality at this scribe intersection revealed delamination (or fringe) at the underlying Low-k

layer without top-side peeling as shown in Figure 9. It was speculated that dicing narrowly between SGPC banks had peeled up the underlying Low-k layers and the Low-k layer delamination was most likely the crack initiation point for the ILD delamination and failure observed in temperature cycling.

The next evaluation was to perform a dicing alignment experiment. The single-cut blade (standard grit / thinner width) was selected for its least top side dicing defects. Wafers were diced offset to the left or to the right of the double-scribe lane so that the dicing blade always cut on top of the SGPC banks. The process window of the table speed was also evaluated. Figure 10 presents optical and SEM images of the left offset dicing, and Table 3 summarizes the temperature cycling results.

**Figure 10: Dicing Quality After Dicing on SGPC Pads (Left Offset Dicing)****Table 3: Temperature Cycling Results for Offset Dicing**

| Cutting Mode | Blade Combination                                      | Offset | Table Speed (mm/sec) | Temp Cycling (-55C / 125C) |
|--------------|--------------------------------------------------------|--------|----------------------|----------------------------|
| Single Cut   | New Single Blade<br>Z2: Standard Grit / Thinner Width) | Left   | 50                   | 0 / 100, 1000 cyc          |
|              |                                                        | Left   | 30                   | 0 / 100, 1000 cyc          |
|              |                                                        | Right  | 50                   | 6 / 100, 200 cyc *         |
|              |                                                        | Right  | 30                   | 3 / 83, 200 cyc *          |

\*: Not dicing-related failures.

Both left and right offset dicing yielded minimal top side peeling but no underlying Low-k delamination. Two splits with left offset dicing and two table speeds passed 1000 cycles of temperature cycling. However, the two splits with right offset dicing failed 200 cycles of temperature cycling. Failure analysis on the failed devices indicated that the failure was not due to dicing defects, but due to die attach defect. These failures will be described further in section "Die Attach Challenge and Resolution".

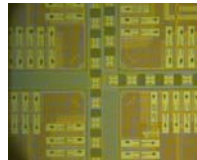
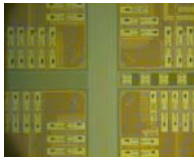
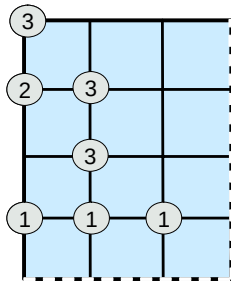
From the dicing inspection and temperature cycling results, it was evident that the Low-k layer delamination induced by dicing narrowly between SGPC banks was the initiation point for weakening the silicon, causing the ILD delamination to propagate into the active die area and failing devices prematurely at 200 cycles of temperature cycling.

**(c) Changing SGPC Placement in Scribe Street**

During the initial temperature cycling assessment using center dicing alignment on the double-scribe lanes, a high level of electrical failures was experienced as previously described. Fifteen failed packages were de-processed to identify the die location on the die reticle of the wafer and to assess if there was any commonality among the test structures in the failed die corners. The die corners contained unique test structures such that the devices can be mapped back to its specific location on the die reticle. The 90nm device used for the evaluation was printed in a 3x4 reticle on the wafer. Figure 11 illustrates the findings of the mapping. The number in the circle represents the instances that particular die corner failed. The ILD delamination failures were found more frequently on the scribe columns 1 and 2 with high test structure content. A comparison between low and high test structure content in the scribe intersections is shown in Figure 12. The scribe lane with high test structure content could be the lane with two parallel SGPC banks intersecting one

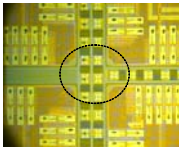
horizontal SGPC bank at the die corner. Having dicing damage at the die corner which is the high stress concentration point had led to the ILD delamination and device failure in the temperature cycling test.

**Figure 11:  
Mapping Failures  
on 3x4 Die Reticle**

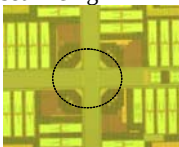
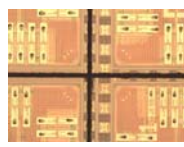


**Figure 12: Scribe with Low (on the left) and High Test Structure Content (on the right)**

The dicing issue related to the double-wide scribe lane and high test structure content was discussed with the wafer fab. A request was made to re-design the scribe street's test structure placement in order to reduce the risk of dicing-induced damage and reliability failures. A new device revision was made with significantly improved scribe design. As seen in Figure 13(b), the device revision 2 implemented a single scribe lane on both x- and y-directions. The SGPC bank's test structures were re-designed to have less metal density. The SGPC banks were placed away from the scribe intersection, and consequently, the scribe corner intersection was free of test structures. Center alignment of the dicing blade was executed, and the devices passed 1000 cycles of temperature cycling.



(a) Device Revision 1 with Vertical Double-wide Scribe and Offset Dicing



(b) Device Revision 2 with Vertical Single-wide Scribe and Center Dicing

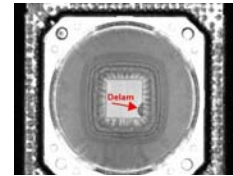
**Figure 13: Changing Scribe Test Structure Placement to Improve Dicing Quality**

#### Die Attaching Challenge and Resolution

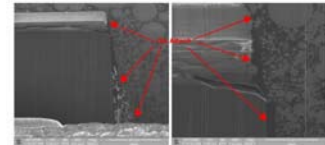
As shown in Table 3, the initial temperature cycle data observed functional failures at 200 cycles. Subsequent Product Analysis of a 200 temperature cycle failure showed delamination on the die side which was confirmed by CSAM imaging (Figure 14). Delamination on a die side was not typical of the failures observed during the packaging development. A typical failure was Die Corner 3 delamination presented earlier in the Dicing section.

As shown in Figure 15, cross-sectional analysis indicated the die attach extending to the top of the die which caused abnormal vertical stress on the die during temperature cycling which led to die cracking, BEOL delamination and device failure.

**Figure 14:  
Die Side Delamination  
Detected by CSAM**



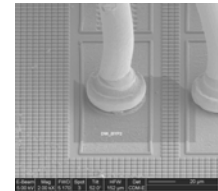
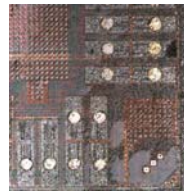
**Figure 15:  
Tall Die Attach  
Fillet Height  
Causing BEOL  
Failure**



An interim solution to correct this failure mode was to control the die attach fillet height. The standard assembly process allowed the die attach fillet height to be less than or equal to 90% of the die thickness. To reduce the vertical stress caused by the die attach material, the fillet height needed to be limited to no more than 2/3 the die thickness. The existing die attach process using a 200um die thickness proved not to have sufficient margin to control the fillet height to the 2/3 die thickness requirement. A DOE was run to evaluate the effect of increasing the die thickness to achieve the desired fillet height, to evaluate dispensing patterns for the die attach material, and to evaluate the volume of die attach material per usage. The results of the DOE indicated that changes be made to the dispensing pattern and to increase the die thickness from 200um to 275um for process robustness and optimization.

#### Wire Bonding Challenge and Resolution

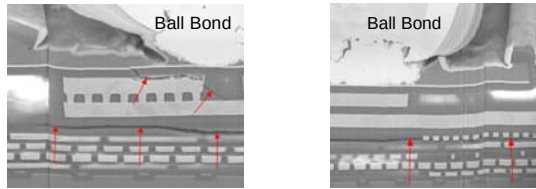
The die pads for the 90nm device were designed with a rectangular shape to allow for wafer probe "touch down" on a portion of the pad saving the remainder of the pad for the actual wire bonding. Initial product builds assumed the entire area of the die pad as useable area resulting in the ball bond being placed in the middle of the pad as shown in Figure 16.



**Figure 16: Initial Wire Bonding in Middle of Bond Pad**

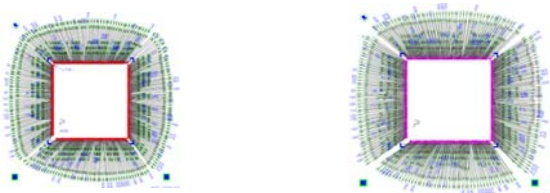
Packages were submitted to temperature cycling test and failed for Scan Chain and JTAG test after 500 cycles. Failed packages were examined with CSAM but no delamination was detected. Extensive Failure Analysis was conducted. The failure was not caused by dicing defects or by tall fillet of the die attach. The failed ball bond and underlying circuitry of the pad were FIB cross-sectioned and inspected. BEOL layer delamination was observed under the failed ball bond. In Figure 17, the initial crack started in the top metal layer where the ball bond was made, and propagated downwards into other BEOL layers. It was also noted that the ILD delamination was localized underneath the affected ball bond and did not extend beyond the ball bond region. Further analysis revealed that the initial wire bonding location was outside the designated Bond

Over Active (BOA) region, which was designed to provide robust mechanical support for low-k wire bonding. This failure mode was corrected by wire bonding on the BOA region which is located on the opposite side of the pad away from the probe region.



(a) Left Side of Ball Bond (a) Right Side of Ball Bond  
**Figure 17: Localized ILD Delamination Underneath Ball Bond**

An additional action was taken to enhance the bondability by updating the bonding diagram to eliminate crossing wires (Figure 18). The original version of the bonding diagram allowed wires with shorter lengths and lower loop heights to cross under the longer wires with taller loops. The new bonding diagram eliminated the wire crossing and opened up the corner gaps. This change also allowed for a more efficient mold flow during the injection molding process.



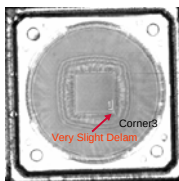
(a) Original Bonding Diagram with Crossed Wires (b) Enhanced Bonding Diagram without Crossed Wires

**Figure 18: Improving Wire Bondability and Moldability by Changing Bonding Diagram**

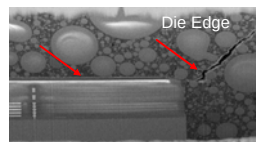
#### Molding Challenge and Resolution

##### (a) Inconsistent Result after 500 Temperature Cycling

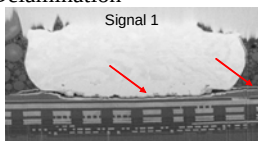
After dicing, die attaching, wire bonding processes and die thickness were fully optimized, packages were submitted to temperature cycling test for confirmation. Opens/shorts failures still persisted after 600 cycles of temperature cycling at 30,000PPM level. All failures were associated with pins in die corner 3.



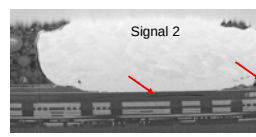
(a) Corner 3 Slight Delamination



(b) Die Edge at Corner 3



(c) Delamination Cracking Underneath Ball Bond



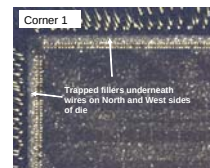
(d) Delamination Cracking BEOL Layers Underneath Ball Bond

**Figure 19: Interfacial Delamination between Die Top and Mold Compound Causing Crack in Ball Bond**

In Figure 19(a), the CSAM image of a failed device is shown. The very slight delamination in die corner 3 detected here was not the same as the large delamination in die corner 3 resulted from poor dicing or the large delamination on the die side resulted from tall fillet height of the die attach. FIB cross-sectioning was performed at die corner 3 of several failed devices. As shown in Figure 19(b), a 45-degree crack in the mold compound and an interfacial delamination between the mold compound and the die surface were found. The interfacial delamination continued to propagate across the die surface and pulled the ball bond off the bond pad (Figure 19(c)) and cracked the BEOL layers underneath the ball bond (Figure 19(d)), thus causing the devices to fail.

Flat-sectioning on failed devices was also performed to thin down the mold compound above the die and to inspect the quality of the mold compound around the die. A non-uniform distribution of the mold compound fillers was noticed as shown in Figure 20. In die corner 1 where the mold injection gate is located, fillers were trapped underneath the wires on the North and West sides flanking die corner 1. In die corners 2 and 4, fillers were visible only on the sides closer to the mold injection gate whereas fillers were substantially less on the sides around the corner and away from the mold injection gate. In die corner 3, loss of fillers was seen on both sides flanking the die corner.

Since the Silica fillers provide the thermal mechanical strength to the mold compound formulation, it is speculated that the loss of fillers in die corner 3 weakened the mold compound. This caused the mold compound to crack during temperature cycling, and caused the delamination to propagate and fail the device.



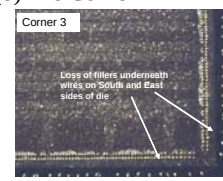
(a) Die Corner 1



(b) Die Corner 2



(c) Die Corner 4



(d) Die Corner 3

**Figure 20: Non-uniform Filler Distribution at Different Die Corners**

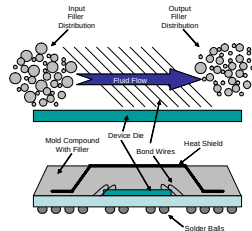
##### (b) Fluid Flow Dynamics of Mold Compound

There are multiple factors that influence the flow of mold compound during the molding process (Figure 21). These components ultimately influence the integrity of the electrical functionality of the device. Factors that impact fluid flow include:

- Wire density/spacing
- Die thickness
- Clearance between die surface and heat spreader
- Center vs. corner gate injection of mold compound
- Mold compound's filler particle distribution
- Mold compound fluid viscosity
- Molding pressure
- Molding temperature

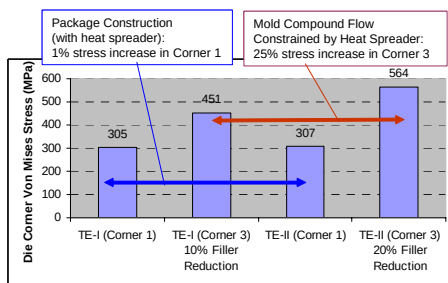
Within the integration of the package, several variables would remain fixed due to the device and package requirements and existing tooling capability. This included device's die size, wire count, and corner gate injection. The final die thickness will determine the clearance between the die and the heat spreader. Two experiments were conducted to understand the effect of the addition of the heat spreader and the die thickness to the distribution of the mold compound fillers and temperature cycling performance.

**Figure 21:  
Package  
and Flow  
Dynamics**



A package cross-sectioning and flat sectioning technique combined with digital imaging processing was developed to analyze and calculate the filler distribution at various die corners. Detailed discussion on the inspection method of the mold compound fillers is presented in a separate publication [8]. It was found that the filler content was about 10% less in corner 3 than in corner 1 in a TE-PBGA-I without a heat spreader. The filler content was about 20% less in corner 3 than in corner 1 in a TE-PBGA-II with a heat spreader attached. The data in TE-PBGA-I without the heat spreader confirms that filler particle loss in the die corner diagonally opposite to the mold injection gate cannot be avoided in a corner gate injection molding process. Furthermore, the heat spreader had obstructed the mold compound flow in TE-PBGA-II, thus resulting in a greater filler loss in corner 3 in TE-PBGA-II.

A finite element model (FEM) was established to investigate the stress increase at the die corner due to the reduction of the mold compound filler [8]. The Von Mises stress in corners 1 and 3 of TE-PBGA-I and TE-PBGA-II is shown in Figure 22. Several observations were made. The 10% filler reduction in corner 3 of TE-PBGA-I translates to almost 50% increase in stress in corner 3 as compared to corner 1 of TE-PBGA-I. Similarly, the 20% filler reduction in corner 3 of TE-PBGA-II yields an 84% increase in stress in corner 3 as compared to corner 1 of TE-PBGA-II. Comparing between package configurations, the stress in corner 1 of TE-PBGA-II is 1% higher than that of TE-PBGA-I. The stress profile in corner 3 is however completely different between these packages. The higher filler loss in corner 3 in TE-PBGA-II translated into a 25% increase in stress as compared to corner 3 of TE-PBGA-I.



**Figure 22: Die Corner Stress Simulation for TE-PBGA-I and TE-PBGA-II**

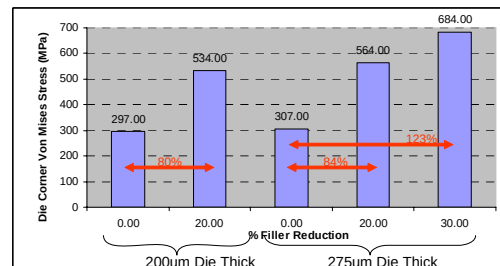
Table 4 summarizes the temperature cycling results of a device with high wire density packaged in TE-PBGA-I and TE-PBGA-II. While TE-PBGA-I passed electrical testing past 2000 cycles, TE-PBGA-II failed at 500 and 800 cycles for pins in corner 3. The empirical data had supported the FEM simulation. This suggests that a 10% filler reduction in corner 3 was an acceptable level to achieve passing at least 1000 cycles of temperature cycling.

**Table 4: Temperature Cycling Results of TE-PBGA-I and TE-PBGA-II (Same Device)**

| Package Type                    | MSL3 / 250C | Temp Cycling (-55C / 125C)          |
|---------------------------------|-------------|-------------------------------------|
| TE-PBGA-I (No Heat Spreader)    | No          | First Fail: > 2000 cycles           |
| TE-PBGA-II (With Heat Spreader) | No          | First Fail: > 500 cycles (Corner 3) |
|                                 | Yes         | First Fail: > 800 cycles (Corner 3) |

Sample Size: 80 units / split

Figure 23 tabulates the die corner stress simulation for two die thickness of 200 and 275um in TE-PBGA-II packages. The effect of the die thickness to the die corner stress was minimal when the filler content reduction was held constant. The most significant factor affecting the die corner stress is still the filler content reduction in corner 3.



**Figure 23: Die Corner Stress Simulation for Different Die Thickness in TE-PBGA-II**

Two devices with different wire density were assembled in TE-PBGA-II packages with different die thickness. Their temperature cycling results are presented in Table 5. All failures accounted here were related to die corner 3 failures with minimal corner delamination. For device A, thinner die of 200um had the lowest failure rate of 2,000PPM and the failures occurred at the greatest number of cycles of 1000. With 275um die thickness, the failure rate increased to 30,000PPM and the failures occurred earlier at 600 cycles. The impact of the high wire density is very evident in device B. Coupled the high wire density with a thicker die, the higher filler loss in corner 3 resulted in the failure rate of 66,000PPM and the first failure occurred the earliest at 500 cycles.

**Table 5: Temperature Cycling Results of TE-PBGA-II with Different Die Thickness**

| Device/<br>Wire Density | Die Thickness<br>(um) | Cum.<br>Failures | Sample<br>Size | % Failure<br>after TC | First Fail<br>TC |
|-------------------------|-----------------------|------------------|----------------|-----------------------|------------------|
| A<br>(26 wires/mm)      | 200                   | 1                | 577            | 0.2%                  | 1000 cyc         |
|                         | 275                   | 51               | 1685           | 3.0%                  | 600 cyc          |
| B<br>(29 wires/mm)      | 200                   | N/A              | N/A            | N/A                   | N/A              |
|                         | 275                   | 81               | 1232           | 6.6%                  | 500 cyc          |

Up to 1000 Cycles

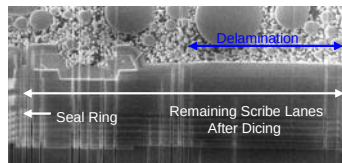
Based on both the FEM simulation and empirical data, the addition of the heat spreader did not add substantial thermal mechanical stress to the package configuration. The most significant factor affecting the corner 3 failure is the resulting loss of the mold compound filler in corner 3 when the heat spreader and the increased die thickness had obstructed the mold compound flow. Although 200um die thickness produced more favorable temperature cycling

results, the difficulty in controlling the fillet height of the die attach prevented the team to select 200 $\mu$ m die thickness as part of the solution. This discovery led to experiments with various mold compound reformulations focusing on smaller filler particle size and distribution improvements in order to minimize the filler content reduction in corner 3.

### (c) Changing to Finer Filler Mold Compound

Modifying the filler particle size and distribution has significant impact on thermal mechanical properties, water absorption, flowability, moldability, package warpage, adhesion, and MSL performance of the mold compound. Moving to smaller filler particle size often times increases the viscosity and therefore wire sweep. Mold compound reformulations needed to adjust the hardener, catalyst system and low viscosity additive in order to compensate for going to smaller filler size and tighter filler distribution and to maintain acceptable thermal mechanical properties. Several iterations of mold compounds from several mold compound suppliers were tried. Two mold compound formulations were finally selected with no electrical failures after 2500 temperature cycles. Filler content loss in corner 3 was measured to be 10-15%. Sampled CSAM showed no sign of delamination in corner 3 at 1500 temperature cycles, and only a slight delamination in corner 3 at 2000 and 2500 temperature cycles. The slight delamination did not cause electrical failures. The minimal delamination between the mold compound and the die top extended only to the die seal ring as shown in Figure 24.

**Figure 24:**  
**Slight Delamination**  
**in Corner 3 After**  
**2500 Cycles When**  
**Using New Mold**  
**Compound**



### Conclusions and Recommendations

This paper examined the root cause for temperature cycle reliability failures using Low-k die in TEPBGA-II package. Failure mode was determined to be ILD delamination predominantly in the package corners, most often in the corner opposite the package mold gate. This location is especially susceptible due to the additional inherent stress forces on the corner of the die and the location being furthest from the mold gate. The most extensive experiments concentrated on wafer dicing parameters and dicing alignment within the scribe grid design and design features within the wafer reticle layout. Additional evaluations were undertaken to enhance the die attach process and molding process. New mold compounds with smaller filler content and tighter distribution further enhanced the package reliability. The first article process and material set resulted in temperature cycle failures at 200 cycle read point. The changes made to the processes and materials have resulted in packages now passing 2500 cycles of temperature cycling (-55°C to 125°C).

An additional recommendation to enhance package reliability would be to encourage more communication between the die physical layout engineering team and the substrate design teams prior to finalizing the die layout. Often the location of the die pads can be modified to increase package reliability by reducing obstructions within the mold compound flow prior to final tape-out. Additionally, reducing the wire density to be less than 20 wires for every millimeter of silicon periphery also enhances mold flow.

### Acknowledgments

The authors would like to thank the following people for their support in their respective areas of expertise: L.C. Tan, Sonder Wang, L.J. Koh, Calvin Lo, C.C. Yong, Ruzaini Ibrahim, W.K. Wong and S.K. Chan from Kuala Lumpur Malaysia (KLM) and Tianjin China (TJN) for their assembly process expertise; Ryan C.L. Loi, K.H. Shum and Menon J from the KLM final test manufacturing center for providing temperature cycling and electrical test support; Linda Pope, Bob Meiers, and Dan Cluff from the Tempe ARAL lab for the CSAM images and volumes of temperature cycle testing; Gaylen Taylor and Lynn Fischer from the DHO electrical test team for supporting the large volume of electrical readouts; John Asquith, Scott McCracken and Tim Cheng from the Silicon Systems Diagnostic Center for performing FIB analysis, die cross sections and Product Analysis reports; Gary Chan and T.C. Chua from KLM Product Analysis and Reliability Laboratory for performing Failure Analysis; and Sharon Furcone from Phoenix Quality Laboratory for package de-processing.

### References

1. Ming-Chun Han, Bei-Yue Yan, J.Z. Yao, Tu Anh Tran, Stephen Lee, Jun Li, "Low K CMOS65 Ball Grid Array 47 $\mu$ m Pitch Wire Bonding Process", IEEE 9th Electronic Packaging Technology Conference, pp. 613-617, 2007.
2. Swaminath Prasad, Flynn Carson, Bret Zahn, T.K. Lee, H.T. Lee, "Thermally Enhanced PBGA Package Characterization, Thermal Performance and Reliability at High Temperatures (Pb-Free)", IMAPS International Symposium on Microelectronics, Vol 4931, pp. 306-312. 2002.
3. Pei-Haw Tsao, Chender Huang, Allan Lin, Mirang-Ji Lii, D.J. Perng, Nun-Sian Tsai, "Cavity Down Thermal Enhanced Package Reliability Evaluation for Low-k Dielectric Cu Interconnect IC", IEEE Electronic Components and Technology Conference pp. 1191-1193, 2004.
4. T.J. Ejim, D.B. Hollesen, A. Holliday, S.A. Gahr, R.J. Coyle, "Assembly and Reliability of Thermally Enhanced High I/O BGA Packages", IEEE CMPT International Electronic Manufacturing Symposium, pp. 25-31. 1997.
5. Guotao Wang, Steven Groothuis, Paul S. Ho, "Packaging Effect on Reliability for Cu/Low-k Structures", IEEE, 42nd Annual International Reliability and Symposium, pp. 557-562, Phoenix, Arizona, 2004.
6. Z. Wang, J.H. Wang, S. Lee, S.Y. Yao, R. Han and Y. Su, "300mm Low-k Wafer Dicing Saw Development", IEEE Transactions on Electronics Packaging Manufacturing, Vol. 30, No. 4, October 2007, pp. 313-319.
7. S. Lee, T. Tran, Y. Yuan, C.T. Siong, T.B. Lau, "Challenges in Temperature Cycling Test for Electronic Packages Containing Low-k/Cu Silicon", Proceedings for 57th 2007 Electronic Components and Technology Conference, Reno, Nevada, pp. 1186-1192.
8. M. Ding, N. Vo, T. Tran, S. Chopin, P. Su, "Filler Dispersion in Epoxy Mold Compound and its Effect on the Reliability of Cu-Low-k Devices in Plastic Ball Grid Array Packages", IMAPS 41<sup>st</sup> International Symposium on Microelectronics, Providence, Rhode Island, November 2008.