

RF MEMS Flip-chip Package Design: Finite Element Modeling and Experimental Verification

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Abstract

RF MEMS device performance can be very sensitive to the die deformation, so appropriate methods need to be considered for the design of the device and package. A numerical approach has been developed to study the die deformation due to the thermal mismatch between die and package substrate as well as the multiple metal-oxide layers associated with the integration of HV RF-CMOS and RF MEMS device layers. The numerical approach consists of two steps: die-level modeling and package-level modeling where the die is flip-chip assembled on a ceramic substrate. The experimental verification is completed by comparison of die-level and package-level models to measurements using Twyman/Green (T/G) interferometry from -40 °C to 210 °C and -40 °C to 200 °C, respectively. The die warpage from modeling is in good agreement with that of T/G interferometry measurement. The warpage of a bare die is approximately 0.4 μm at room temperature and varies non-linearly as temperature changes. The non-linearity is attributed to the plastic deformation of metal in the multiple metal-oxide layers. The validated die-level model is then transferred to package-level model to study the behavior of the assembled die. The warpage of the assembled die is approximately 1.1 μm at room temperature and changes more linearly as a function of temperature. It is concluded that the die/package modeling approach with proper modeling considerations is the key to accurately describe the non-linear characteristics of complex RF MEMS dies and provide more reliable modeling results for package design.

Key words: RF MEMS, Package Design, Finite Element Modeling, T/G Interferometry

Introduction

The significant effect of packaging on Micro-Electro-Mechanical System (MEMS) device performance has been reported in studies [1-3], which reveal that it is important to consider the MEMS devices and package as a coupled design problem due to the heterogeneity nature of the MEMS die and package [4]. As a MEMS die typically consists of multiple layers of metals and dielectric materials that have large difference in the thermomechanical properties, thermally-induced deformation on the bare die will occur prior to the packaging process. The die deformation can potentially remain and interact with the packaging process. Consequently, the error of packaging effect evaluation can be substantial if the

bare die deformation is large but not properly considered. As a result, the deformation of the bare die and sequential assembled die should be carefully investigated in order to evaluate the coupled die/package design with higher accuracy.

In this paper, we report a numerical approach to study the die deformation due to the thermal mismatch between die and package substrate as well as the multiple metal-oxide layers associated with the integration of HV RF-CMOS and RF MEMS device layers on the die. The numerical approach consists of two steps: die-level modeling and subsequent package-level modeling where the die is flip-chip assembled on a ceramic substrate. Since modeling accuracy typically depends on many factors including

model setup (mesh density, simplifications, etc.), process assumptions, and material properties, experimental verification is necessary to ensure that the model predictions are consistent with corresponding experimental measurements before the models can be extensively applied to design and parametric study [5-8]. In this work, die-level and package-level models are verified with Twyman/Green (T/G) interferometry from -40 °C to 210 °C and -40 °C to 200 °C, respectively. And the importance of specific modeling consideration is discussed.

Experimental Characterization

A. Sample Preparation

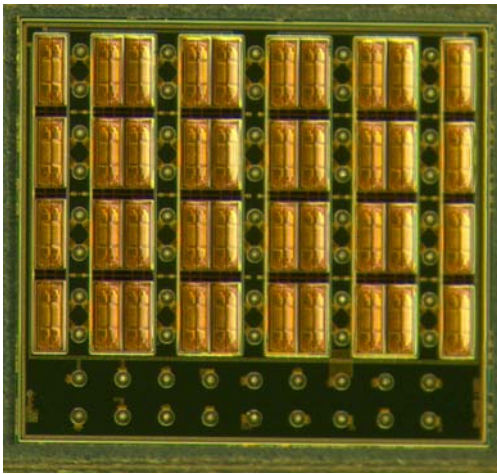


Figure 1. Top view of a RF MEMS die

In this study, the RF MEMS die (3.7 mm × 3.3 mm × 0.2 mm) consisted of a silicon substrate with multiple oxide-metal thin layers that are associated with the integration of HV RF-CMOS and RF MEMS device layers. These multiple layers reside on one side of the silicon die and have a total thickness of approximately 15 μm. The total metal volume ratio in the multiple oxide-metal thin layers is approximately 10%. Each die includes 58 I/Os and 80 RF MEMS devices, which are fixed-fixed beams with a metal-oxide-metal structure. A multilayer, thin film lid is fabricated over the beams to house and protect the beams. A top view of a die is shown in Fig. 1. To package the die, the die is bumped with 95Pb-5Sn solder balls which measure ~Φ140 μm × 90 μm (Fig. 2) and then flip-chip assembled on a Low Temperature Co-fired Ceramic (LTCC) substrate which measures 5.2 mm × 5.2 mm × 0.4 mm. The flip chip assembly is made through a conventional reflow process with a peak reflow temperature ~350 °C.

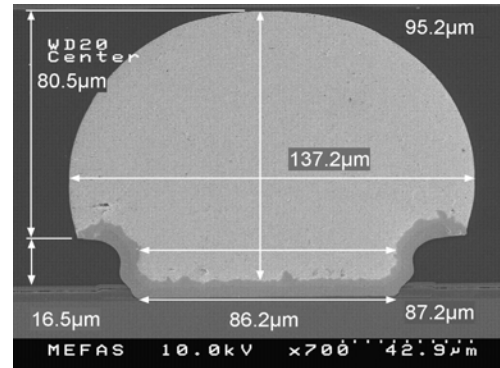


Figure 2. Cross-section of a solder ball

B. Deformation Measurements

T/G interferometry is employed to verify the displacement prediction of the numerical models. Figure 3 shows the optical setup schematically. T/G interferometry can measure the surface contours (out-of-plane displacement) with submicron sensitivity. The surface contour map is constructed in a way that one wavefront from the specimen interferes with the other wavefront from a flat reference mirror. The out-of-plane displacement W can be calculated by:

$$W = \lambda N / 2 \quad (1)$$

where λ is the wavelength of the laser light and N is the fringe order at each point in the fringe pattern [9].

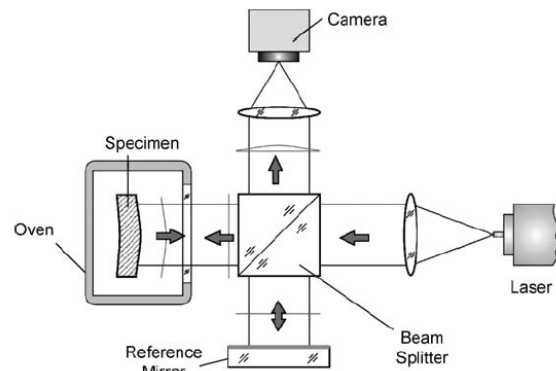


Figure 3. Schematic of T/G interferometry setup [9]

The T/G interferometry measurement is conducted in a specially designed environmental chamber over a temperature range from -40 °C to 210 °C for bare dies and -40 °C to 200 °C for packages to observe the die deformation as a function of temperatures. The detailed principle and procedure of the measurement techniques and experimental setup can be found in many references [9, 10].

Numerical Modeling

The non-linear Finite Element Analysis (FEA), die/package simulations are performed using ABAQUS 6.7. Figure 4 shows a 3-D, half-symmetry model of the RF MEMS die. The model includes approximately 20,600 8-node solid elements (C3D8R) and 2,000 8-node continuum shell elements (SC8R) with a multi-layer composite material definition. The composite shell elements are used to represent the multiple oxide-metal layers on the die due to their very small thicknesses compared to the die dimension. A schematic of the multiple oxide-metal layers is shown in Fig. 5. The averaged material properties of each oxide-metal layer are extracted from “numerical experiments” [11], where a small representative region with fine metal features and field oxide is evaluated to fit average material properties of the layer with a mixture of materials. It is noted that material properties obtained using this approach are close to the calculated results using the rule of mixture, with a discrepancy typically less than 5%, since the fine metal features are reasonably uniformly distributed across a large portion of the die area. The same approach is also applied to derive average material properties of the lid which consists of multiple thin, dielectric layers.

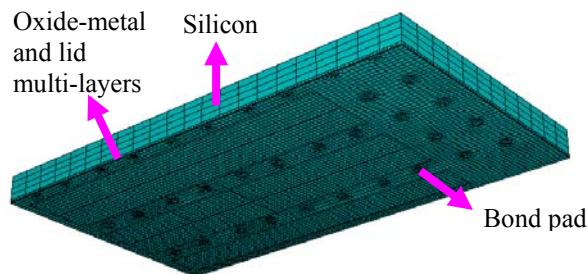


Figure 4. Half-symmetry RF MEMS die model

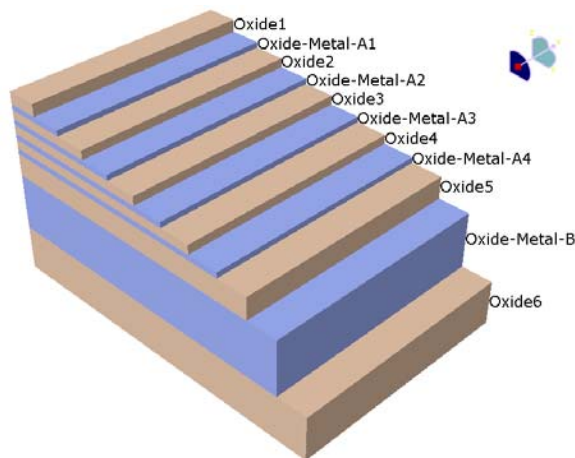


Figure 5. Schematic of multiple thin layers

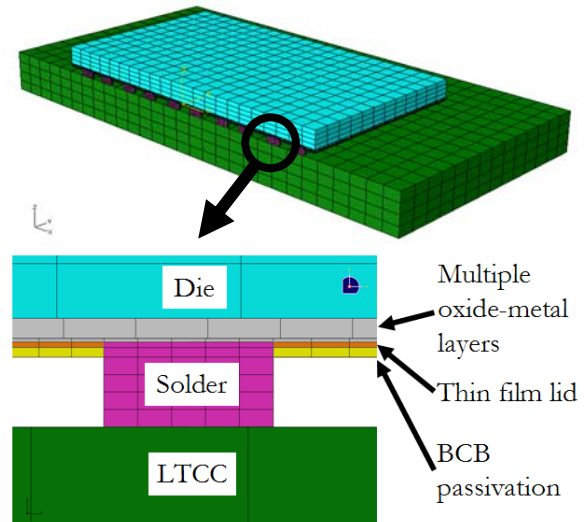


Figure 6. Half-symmetry flip chip package model with enlarged details

Table 1. Material Properties

	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/K)
Si	169	0.28	2.5(25°C) 3.6(250°C) ¹
Oxide-Metal (Type A)	74	0.24	12.0
Oxide-Metal (Type B) ²	71	0.2	6.8
Oxide	70	0.17	0.5
Lid	110	0.2	1.0
BCB ³	2.9	0.34	43
Pb95-Sn5 ⁴	20	0.42	28.7
LTCC	150	0.26	5.0

¹<http://www.matweb.com/search/DataSheet.aspx?MatID=102>

²Yield strength = 125 MPa with work hardening (strength = 300 MPa at plastic strain = 0.006)

³BCB glass transition temperature $T_g > 350^\circ\text{C}$

⁴Yield strength = 35 MPa (nanoindentation)

In the package model, the die is flip-chip assembled on a LTCC substrate as shown in Fig. 6. The package model includes approximately 39,000 8-node solid elements (C3D8R) and 2,000 8-node continuum shell elements (SC8R) representing multiple oxide-metal layers on the die. The reflow temperature of the package is set to be 350°C . The material properties used in the die/package simulations are summarized in Table 1.

In the die/package simulations, we only consider thermal mismatch induced deformation and ignore the potential hygroscopic effect on the die or substrate and inelastic effects of time dependent

creep/relaxation that may be present in the system. The simulation flow consists of the following steps:

1. Die-level modeling: the RF MEMS die cools from thin film deposition temperature to room temperature. The deposition temperature of all the thin films on the die is assumed to be identical. Following that, the die is subject to a few temperature cycles from -40 °C to 210 °C to simulate the characterization process using T/G interferometry;
2. Package-level modeling: the result of the die-level modeling is then transferred to the package-level model. The initial bare die warpage at the reflow temperature is obtained using the die model and is induced by applying a stress gradient in the die thickness direction in the package model. The package substrate is assumed to be flat at the reflow temperature. The whole package cools from the reflow temperature to room temperature and is then subject to a few temperature cycles from -40 °C to 200 °C to simulate the characterization process using T/G interferometry.

Die-Level Modeling and Experimental Verification

Figure 7 shows the fringe images of a RF MEMS die during the temperature cycle from -40 °C to 210 °C. It is apparent that the deformation of the die is asymmetric along the vertical direction corresponding to the non-uniform distribution of the RF MEMS devices shown in Fig. 1. The die deformation is consistent in the first and second temperature cycle.

To compare the experimental results to the modeling results, die warpage is extracted from both the FEA and T/G interferometry measurement over temperatures. The die warpage at die top surface is defined by:

$$\text{Warpage} = dZ (\text{die center}) - dZ (\text{die corner}) \quad (2)$$

where dZ is the out-of-plane displacement. A positive die warpage means that die center is higher than die corner in the Z direction. Figure 8 illustrates the measured (Die A and Die B) and simulated (FEA and FEA-NP) die warpage change during the temperature cycle. As shown in the figure, the die warpage is positive from -40 °C to 210 °C and is approximately 0.4 μm at room temperature. It is evident that the die warpage change is highly non-linear with temperature and forms a hysteresis loop. This non-linearity is attributed to the plastic deformation of metal in the

multiple metal-oxide layers, which can be seen by comparing results of “FEA” and “FEA-NP” in Fig. 8. The characteristic hysteresis loop is predicted by modeling when detailed metal-oxide layer construction and proper material plasticity definition are built in “FEA”. On the contrary, the die behavior can not be accurately described by “FEA-NP” that has no layer construction and plasticity definition. Given the measurement uncertainty of 63 nm, the modeling result with detailed layer construction and proper material definition agrees well with the T/G interferometry measurement over the temperature range from -40 °C to 210 °C, and the verified die model can then be used in the package-level modeling.

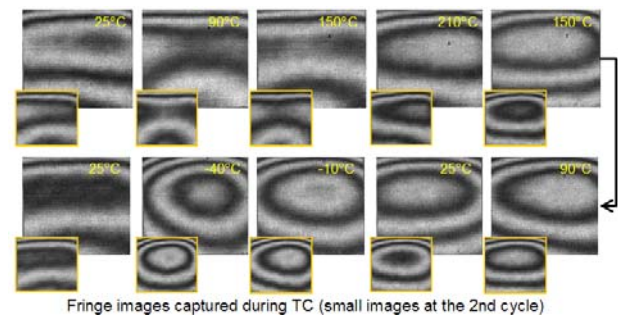


Figure 7. Fringe images of a die during a temperature cycle

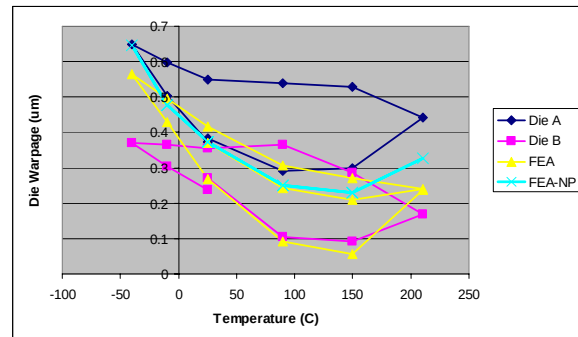


Figure 8. Die warpage change during a temperature cycle

Package-Level Modeling and Experimental Verification

It has been demonstrated that the detailed die construction and proper material definition are the key to capture the characteristics of the die behavior over temperatures. The verified die model is transferred to the package model in this step for higher package modeling accuracy. It is noted that the die warpage increases after 150 °C during heating in Fig. 8. This feature is important for packaging simulation which starts from the solder reflow

temperature. To take into account the initial bare die warpage in the package modeling, the die model is employed first to predict the bare die warpage at the reflow temperature. Following that, the same die warpage is achieved by applying a stress gradient in the die thickness direction. The stress gradient applied on the die is then used as an initial condition in the package model to induce the predicted initial die warpage.

In this modeling step, the LTCC substrate is assumed to be flat at the reflow temperature. This assumption has to be examined. Figure 9 shows the fringe images of the LTCC during temperature cycling. No discernable warpage (<1 fringe order) is observed throughout the temperature cycle from -40°C to 210°C . It is therefore reasonable to assume that the LTCC remains flat at the reflow temperature.

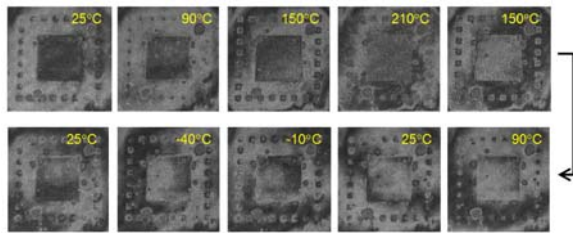


Figure 9. Fringe images of a LTCC substrate during a temperature cycle

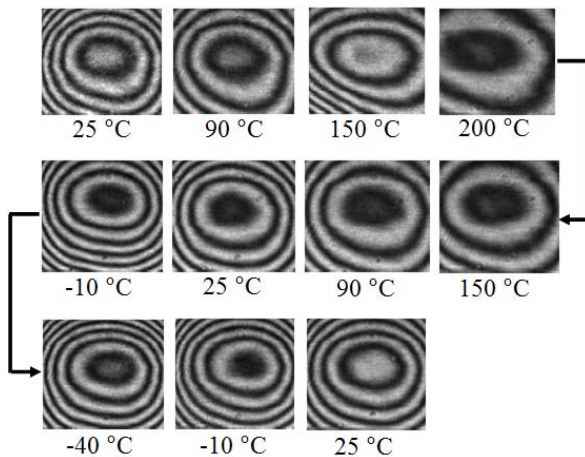


Figure 10. Representative fringe images of a die flip-chip assembled on LTCC during a temperature cycle

Figure 10 illustrates the representative fringe images of a die flip-chip assembled on a LTCC substrate. As can be seen, the fringe pattern is significantly different from that of the bare die. The fringes are more symmetric; concentric circles are formed after packaging process and during the temperature cycle from -40°C to 200°C . Figure 11 shows the measured (samples 1, 2, and 3) and

simulated (FEA and FEA-NI) die warpage change during the temperature cycle. It is clear that the assembled die warpage at room temperature, approximately $1.1\text{ }\mu\text{m}$, is much higher than that of the bare die and warpage changes more linearly as a function of the temperature, which implies the package plays a significant role on die deformation in this case. This packaging effect is also seen in Fig. 7 and Fig. 10 where the bare die deformation is affected by non-uniformly distributed RF MEMS devices whereas assembled die deformation is mainly affected by the CTE mismatch between the die and substrate.

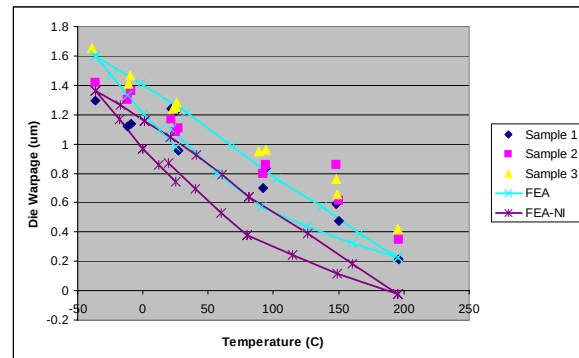


Figure 11. Assembled die warpage change during a temperature cycle

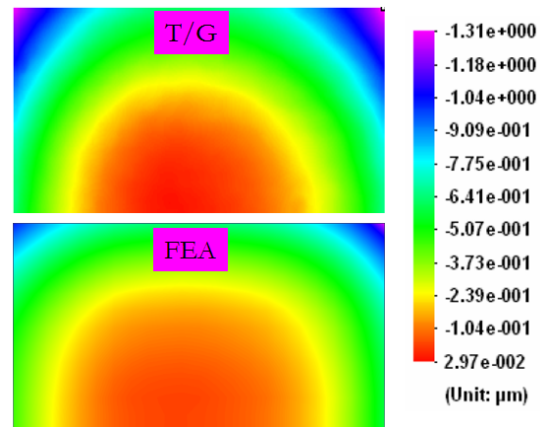


Figure 12. Surface contour of half assembled die at room temperature

The importance of the die initial deformation is shown in Fig. 11. The curve of “FEA” represents the package model with die initial deformation; the curve of “FEA-NI” simply presumes a flat die at the reflow temperature in the package. Compared to “FEA” and measurement results, the simplification causes approximately $0.2\text{ }\mu\text{m}$ deviation in die warpage prediction over temperatures. By using the die/package approach and proper modeling consideration, the package-level modeling results

match the T/G interferometry measurements very well as shown in Fig. 11 and Fig. 12.

Discussions

Considerable MEMS device deformation induced by wafer warpage can occur right after the device wafer is fabricated when complex multiple thin films are deposited on the wafer. The device deformation will be further affected by the following packaging process as the packaging changes die warpage. Thus, it is critical to consider the MEMS devices and package as a coupled design problem especially when the performance of MEMS devices, such as fixed-fixed beams, is sensitive to the warpage-induced mechanical boundary constraints. The optimum design is typically targeted at package-level and/or board-level. However, the error of a single-step package-level evaluation can be substantial as demonstrated in the previous section. The two-step modeling approach with proper modeling considerations not only reveals the characteristics of the die behavior in each processing step, but also is the key to accurately describe the final packaging effect on die by taking into account the die deformation of each processing step. Further, the bare die deformation can play a more important role when the packaging effect is limited by decoupling the die from the substrate in some package designs, for example, package with softer solder materials, less solder joints, smaller solder diameter and/or larger solder standoff height. In such cases, the two-step modeling approach is expected yield much more accurate and reliable results for parametric study and package design optimization.

Conclusions

A two-step numerical approach has been developed to study the RF MEMS die deformation. The numerical models are verified by using T/G interferometry. For the bare dies, T/G interferometry measurements show that the die warpage is approximately 0.4 μm at room temperature and varies non-linearly as temperature changes from -40 °C to 210 °C. This non-linearity is captured by the die-level model with detailed metal-oxide layer construction and proper material plasticity definition. The verified die model is then transferred to the package-level modeling. The warpage of the assembled dies is approximately 1.1 μm at room temperature and changes more linearly as a function of temperature, which implies that package plays a significant role on die deformation. Good agreement is obtained between T/G interferometry measurement and package-level modeling from -40 °C to 200 °C. It is shown that

there is a 0.2 μm deviation in warpage prediction using the model without proper modeling considerations, which can be significant in the cases where MEMS devices are sensitive to the warpage-induced mechanical constraints. It is concluded that the die/package modeling approach can accurately describe the non-linear characteristics of complex RF MEMS dies and provide more reliable modeling results for package design. By using the modeling approach, parametric study of the package design can be conducted with higher confidence to understand the die deformation as a function of part geometry, materials, and process conditions, and to optimize the package design for the RF MEMS devices.

Acknowledgments

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