

Hybrid CSP Package

Challenges and Solutions in Design and Manufacturing

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Abstract

The introduction of CSP hybrid package, where a wire bond die is stacked on a flip chip die, enabled the industry to integrate memory and ASICs in a smaller form and fit package compared to other 3D packages like stacked wire bond package or package-on-package. However, the process of making such a structure using conventional design rules and conventional processes like underfill (UF) and transfer mold limits the application to less complicated circuit interconnection with fewer I/Os, thus making it less appealing to the industry. This paper will discuss the challenges in making a high density Hybrid package and eventually the solution starting from design, such as substrate routing and bump design, to the assembly processes with detailed qualification and reliability test result.

1.0 Introduction

As the portable consumer products move to a higher I/O density and more complicated ASIC design, stacked wire bond package can no longer serve the needs of this complicated design. With the advancement of substrate and RDL technologies, a more complex stacking package, called hybrid package has been developed. At first glance, making a Hybrid CSP package looks simple – mount a flip chip die to a substrate then underfill and cure followed by die attaching a wire bond die on top of the flip chip die, wire bonding, molding, ball attach, and singulation. However, when an actual high density application design was started, the conventional rules of FC, wire bond, bumping, and substrate collided with each other limiting the design rules to a very loose one to accommodate the requirements of the combined processes making the die and package size bigger and expensive. A cross functional team was formed from different areas of expertise – bumping, flip chip, wire bond, bump design, substrate design, and assembly manufacturing – to come up with designs, innovations, technology, process, and materials that will allow the design rules to co-exist with minimum conflict and eventually reducing the die size and package size which reduces cost and real state area on the application boards.

2.0 Design rule limitations

The following discussion outlines the 2 major design rule limitations and the effect of these issues on the overall structure.

2.1 Wire bond design rules vs FC design rules

Figures 1 and 2 shows the package structure of a wirebonded die and a flipchip die. For a wirebonded die, the bondfinger can be closer to the die but for a flipchip die, the bondfinger has to move further away from the die due to a wider underfill keep out area which can result to a bigger package.

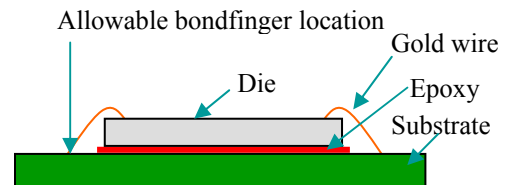


Figure 1. Cross section view of a wire bond part

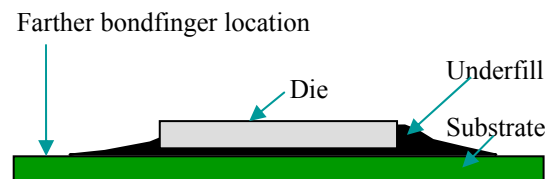


Figure 2. Cross section view of an underfilled FC part.

2.2 Bump pitch design rule vs substrate design rules

Figure 3 shows a portion of bump design using a flipchip substrate and a wirebond substrate. With the use of FC substrate, a finer trace and space design can be used as this is using ABF as dielectric where the semi-additive copper patterning process can be used. For a hybrid package, the use of glass reinforced prepreg as dielectric is needed to have a harder material under the wirebond fingers on the substrate to support the bondfingers during wirebond process. With this prepreg dielectric, the substrate trace and spacing design rule is wider as this uses subtractive process in copper patterning. This limitation means the bump pitch is bigger to accommodate the wider trace and space design rule and can result to a bigger die or reduced bump count.

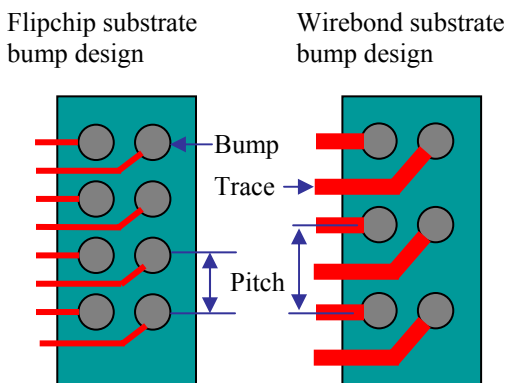


Figure 3. Bump pitch, trace and spacing comparison between flipchip and wirebond substrate

3.0 Solutions, innovations, and evaluation results

The following discussions outlines the solutions for the 2 major challenges previously mentioned. This also includes result of evaluation, work done to improve the process, and final qualification work and result.

3.1 Mold underfill (MUF) solution

The first step is to find a process that will allow the wirebond design rule on bondfinger to die edge distance on this structure. This was done by replacing the underfill with mold underfill material and process. In the development stage, several mold underfill materials were selected. The mold underfill selection process will only be briefly discussed, with more detailed discussion on the test vehicle used and the result.

3.1.1 MUF manufacturing process and reliability challenges

In the selection of MUF material, there were several manufacturing and reliability challenges that were considered. Wiresweep, mold void, compound adhesion to different surfaces, strip warpage after molding, stress to lowK that may lead to lowK crack, moisture absorption that may lead to popcorning, and bump solder joint crack. To address these issues, the material and process evaluation and qualification was done in 2 phases as discussed below.

3.1.2 MUF Phase 1 evaluation details

Phase 1 MUF evaluation is the initial package qualification designed to evaluate MUF process and materials using mechanical daisy chain FC die and wire bond test die on a Hybrid package. This will provide the basis of selecting the baseline process and material in terms of manufacturability and package reliability.

A total of 8 different mold underfill were selected to run the initial evaluation stage at 3 different assembly houses. Each assembly house have their own process and experiences in using mold underfill but limited to a few engineering evaluation. For the purpose of discussion, we will call the different mold underfill as MUF-AMD1 to MUF-AMD8 and the assembly houses as ASSY_1 to ASSY_3.

3.1.2.1 Phase 1 test vehicle description

The test vehicle used in the phase 1 evaluation process was an 8x8 Hybrid TFBGA package that have a daisy chain connection to the flip chip die and a point-to-point connection with the wire bond die for testability.

The flip chip die was a 4mm x 6mm daisy chain die with fine bump pitch and eutectic bump. The top passivation layer of the die is polyimide.

The wire bond die was a 3mm x 4mm daisy chain die. The top passivation layer of the die is polyimide.

The substrate was a BU substrate using prepreg as dielectric. The wire bond finger and ball pad finish was Ni/Au while the C4 pad was with eutectic presolder.

3.1.2.2 Phase 1 evaluation result

The 8 types of mold underfill were distributed at the 3 assembly houses based on AMD selected material and the assembly house preference as shown on table 1 below.

Table 1. Design of experiment table

Assembly house	Mold underfill
ASSY_1	MUF-AMD1 MUF- AMD4 MUF-AMD5
ASSY_2	MUF-AMD2 MUF-AMD3 MUF-AMD4 MUF-AMD5 MUF-AMD6
ASSY_3	MUF-AMD2 MUF-AMD3 MUF-AMD4 MUF-AMD7 MUF-AMD8

A sample size of 2 strips per MUF type were built. The parts were then distributed and subjected to reliability test with the conditions shown in table 2 below.

Table 2. Reliability test condition

Test	Condition
Moisture sensitivity level	JESD22-A113/J-STD-020 LEVEL-4, 255+5/-0C reflow temp
Highly accelerated stress test (Unbiased)	JEDEC 22-A118; 130°C/85%RH33.5PSIG; 100H
Temperature cycling test	JEDEC 22-A104; - 55°C~125°C ; 1000 cycles
High temperature storage	JEDEC 22-A103; 150°C ; 1000H ; no preconditioning
Multiple reflow	255+5/-0C reflow temp, 5X to failure

Out of the 8 mold underfill selected, only 3 mold underfill materials, MUF-AMD1, MUF-AMD2, and MUF-AMD3, have good result in both manufacturability and reliability. These mold underfills were selected to continue to phase 2.

3.1.3 Phase 2 evaluation details

Phase 2 evaluation is the package qualification using the selected processes and materials from phase1 but this time using real lowK FC die. This will provide the effect on the reliability of the selected processes and materials to the lowK FC die.

3.1.3.1 Phase 2 test vehicle description

The test vehicle used in the phase 2 evaluation process was a 10x10 Hybrid TFBGA package that have a point-to-point connection to the I/Os of the flip chip die. The wire bond die have no connection to maximize the available balls connection to the flip chip die and also considering that the wire bond process was already tested in phase 1.

The flip chip die was a lowK die with die size of 4mm x 8mm, fine bump pitch, eutectic bump, and normal top passivation layer.

The wire bond die used was the same as phase 1 experiment.

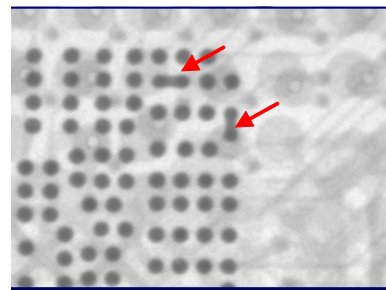
The substrate was a BU substrate using prepreg as dielectric. The wire bond finger and ball pad finish was Ni/Au while the C4 pad was with eutectic presolder.

3.1.3.2 Phase 2 initial evaluation result

The initial phase 2 experiment results showed several unexpected failures that we did not encounter on phase 1 evaluation. The following discussion will discuss in detail the defects found, the analysis, and the action taken to fix the problem.

3.1.3.2.1 Bump shorts

After FC attach, bump shorts were found as shown in figure 4 below. All the defects were located randomly near all corners of the die.

**Figure 4.** X-ray photo of solder bump after FC attach.

Analysis of these failures showed that a combination of factors led to this issue – the die is rectangular in shape with the long side twice as long as the short side compounded with the strip warpage could easily cause misalignment especially affecting the corner bumps; the bump size and C4 pad soldermask openings were also too big narrowing the distance between bumps which also made it easier for bump shorts to happen. Of all these factors, the bump size and C4 pad opening size were ranked the highest

realistic risk and contributor for these failures to be considered in actual application.

Table 3 and figure 5 below shows the phase 1 design and the phase 2 design in terms of bump size and substrate solder mask opening. This shows that the phase 2 design have bumps closer by 10um to each other. Phase 1 design did not encounter the bump shorting issue thus the phase 1 minimum distance between bumps and minimum distance between solder mask opening design was recommended to actual production design.

Table 3. Comparison between phase 1 and phase 2 design values.

Feature	Phase 1 design	Phase 2 design
UBM size (A)	X	X + 10 um
Bump size (B)	X	X + 10 um
Minimum distance between bumps (C)	X	X- 10 um
Solder mask opening size (D)	X	X + 5um
Minimum distance between solder mask opening (E)	X	X – 5um

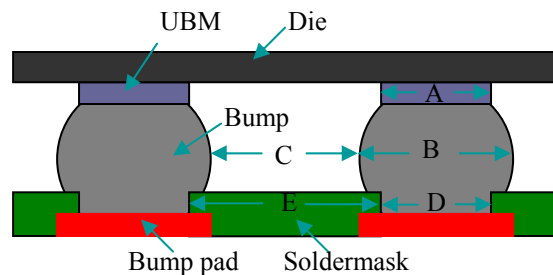


Figure 5. Illustration of bump sizes and distances.

3.1.3.2.2 Bump solder lumping

Bump solder lumping were found after molding process as shown in figure 6 below.

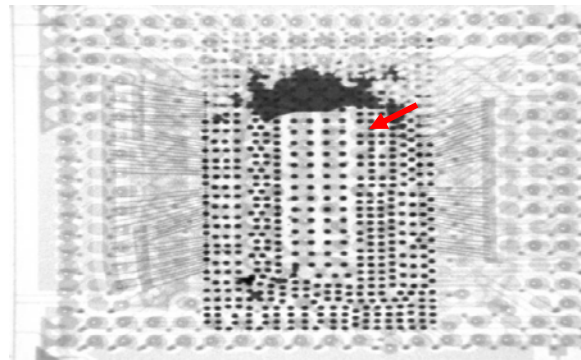


Figure 6. X-ray photo of bumps after molding.

Analysis of this failure showed that the normal molding temperature is too close to the melting temperature of eutectic solder. The nominal mold temperature was reduced to increase its gap to the melting temperature of eutectic solder. The verification lots showed good result thus the succeeding lots build for qualification used the lower molding temperature without any problem.

3.1.3.2.3 Delamination

Delamination was found after MSL3 preconditioning and 3x 260C reflow as shown in figures 7 and 8 below. Cross section revealed that the origin of delamination was between the die passivation layer and the the mold underfill.

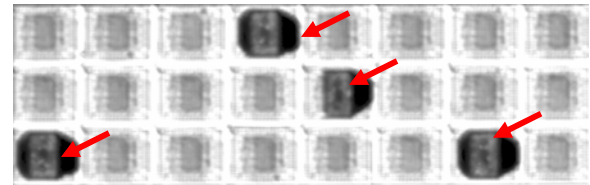


Figure 7. SAT photos of parts after precondition reflow. Parts with delamination are pointed with arrows on the pictures.

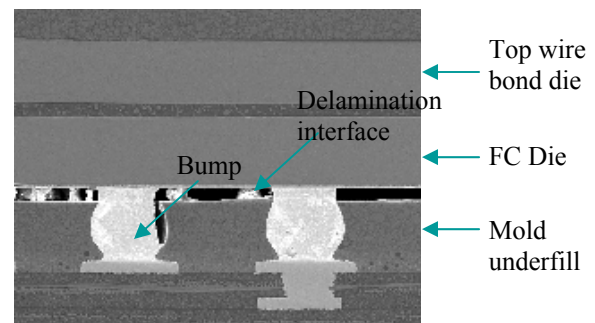


Figure 8. Cross section photos of delamination area.

Analysis of these failures showed that a combination of factors led to this issue, namely plasma cleaning method, substrate design, and die passivation material.

Plasma cleaning is a well know process used to roughen and clean surfaces in preparation for interfacial bonding between the plasma cleaned surface and another material. To name a few application, plasma cleaning is used at flip chip process before underfill dispense, on a die and substrate before wire bond process and molding process as well. However, the method of plasma cleaning is different between FC and wirebond or molding process. In a wirebond package, the plasma cleaning method is effective in cleaning exposed surfaces as shown in figure 9. For a flip chip package,

there is a narrow gap between the die and the substrate which the plasma cleaning method for wire bond packed is not optimized for. In this case a plasma method where the gas flows horizontally is a more effective way of getting into this area as shown in figure 10.

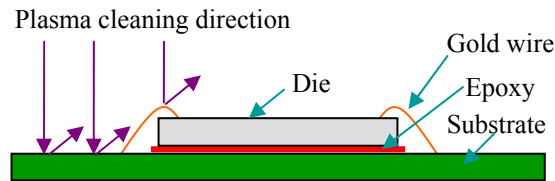


Figure 9. Wire bond package plasma cleaning method

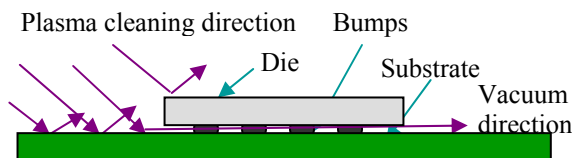


Figure 10. Flip chip plasma cleaning method

As molding process is normally used on wirebond package, the plasma equipment set-up for molding are usually the wirebond plasma equipment. Investigation of phase 1 and phase 2 process showed that phase 1 used the FC plasma equipment while phase 2 used the wirebond plasma equipment thus to resolve this issue the FC plasma equipment was defined in the process.

The other issue seen was the metal density on the layers of the substrate. Table 4 shows the comparison between phase 1 design and the phase 2 design in terms of layer metal density per layer. This shows that the inner metal layers of the phase 2 substrates were just a third of the phase 1 substrate. For a normal wire bond package the metal density may not be that critical as moisture will not be trapped on the small area between the die and the substrate. For a hybrid package, this proves to be critical. To have an effective moisture barrier from penetrating the package, a good metal density on the substrate layers was needed. Based on this data, higher metal density on the inner layers were recommended on the actual production design.

Table 4. Phase 1 and phase 2 design values.

Substrate layer	Phase 1 design	Phase 2 design
1	X / 2	X / 2
2	X	X / 3
3	X	X / 4
4	X / 2	X / 2

Another difference between phase 1 and phase 2 build was the die passivation layer. Phase 1 used polyimide while phase 2 used the normal passivation layer.

3.1.3.3 Phase 2 final evaluation result

After implementing the actions to fix the manufacturing process issues and reliability failures, a full qualification run was done on 3 assembly lots per mold underfill on all 3 assembly houses with good result on 2 mold underfill. Reliability test was done according to the conditions shown on table 2 except the multiple reflow test. Table 5 shows the detailed result. With this data, MUF-AMD1 will be used at ASSY_1 and MUF-AMD2 on ASSY_2 and ASSY_3. Further work will be done on an adhesion improved version of MUF-AMD3 as another alternative mold underfill.

Table 5. Phase 2 result

Assembly house	Mold underfill	Result
ASSY_1	MUF-AMD1	Pass
	MUF-AMD3	Pass
ASSY_2	MUF-AMD2	Pass
	MUF-AMD3	Fail
ASSY_3	MUF-AMD2	Pass
	MUF-AMD3	Pass

3.2 Substrate design improvement

The next step was to find a solution to maintain a bump pitch that will not significantly increase the die size. Several solutions were considered.

The first one considered is the use of more build up layers as escape layers. However, this significantly adds cost and thickness to the package which is undesirable.

The next one considered was to have a trace and space design better than the current design rule using a combination of subtractive and additive process. Through the cooperation of the substrate vendors, an advanced trace and spacing rule with values in between the normal wirebond substrate rule and the FC substrate rule was developed. Figure 11 shows that with a finer trace and space design, the bump pitch can be reduced.

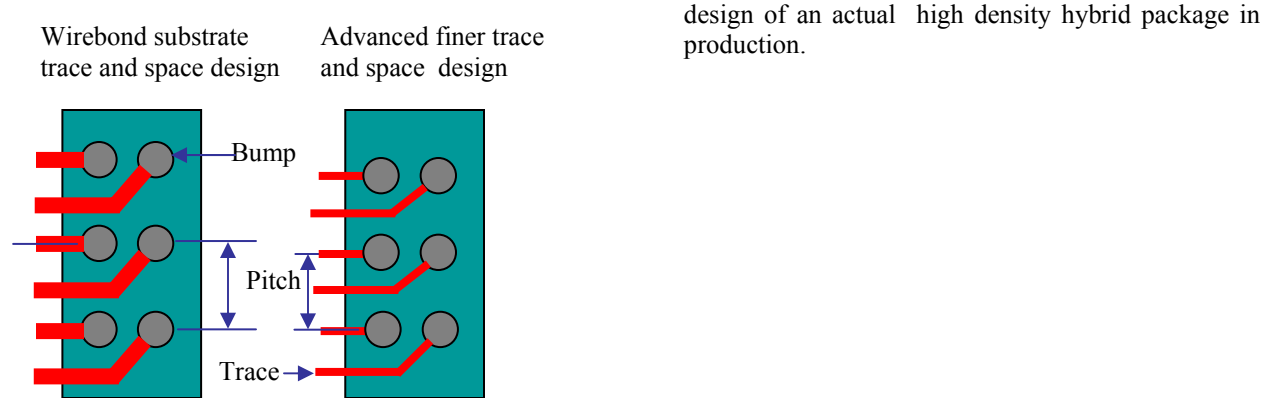


Figure 11. Comparison between normal wirebond substrate and advanced finer trace and space design.

Another design feature utilized was the use of a rectangular bump pad design. Rectangular bump pads can significantly increase the space between bumps. This feature combined with the advanced finer trace and space design rule significantly reduced the bump pitch while allowing trace or traces to be routed in between bumps. This feature is shown on figure 12 below.

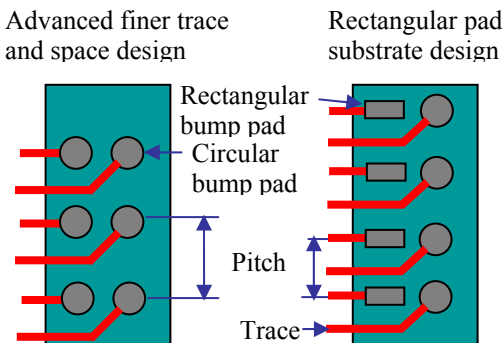


Figure 12. Comparison between advanced finer trace and space design with circular bump pads and rectangular bump pads.

4.0 Summary:

This paper has shown how a high density Hybrid CSP package can be designed on a smaller die and package by using mold underfill process, tighter substrate trace and space design rule, and use of rectangular bump pads. This paper has also shown the challenges in using mold underfill and the solutions on each challenges such as the use of the correct plasma equipment, lower molding temperature, optimum bump spacing rule, optimized substrate metal density, and the use of polyimide as die passivation material. This work has lead to the