

High Reliable Resin Core Bump Technology for 20 μ m pitch COG (Chip on Glass) Interconnection

Haruki Ito, Shuichi Tanaka, Hideo Imai, Shinji Mizuno, Nobuaki Hashimoto, Akira Makabe
Advanced Technology Development Center, Production Engineering & Development Dept.
SEIKO EPSON Corporation
Fujimi 1010, Fujimi-Machi, Suwa-gun, Nagano 399-0295, Japan
Phone: +81-266-62-7534, Fax: +81-266-62-4415
Ito.Haruki@exc.epson.co.jp

Abstract

The Resin Core Bump technology is an innovative COG (Chip On Glass) technology. It has compatibility with conventional Au bump with ACF (Anisotropic Conductive Film) COG technology, fine pitch capability due to eliminating conductive particles from the bonding system, and superior reliability due to direct interconnection between bump and substrate electrodes. In this paper, we report reliability test result of 20 μ m pitch interconnection. It showed stable and high reliable results.

Keywords: Chip-On-Glass, Fine Pitch Bumping, Interconnection, Reliability

Introduction

Chip on glass (COG) technology has been widely used as interconnection technology of mounting Liquid Crystal Display (LCD) driver ICs directly onto the glass substrate of LCD panels, for about 20 years^[1]. Most common (conventional) COG interconnection structure is established by flip-chip bonding process with electro-plated gold bumps and anisotropic conductive film (ACF). In this bonding structure, electrical path is formed through conductive particles that are trapped between gold bump and electrode of the glass substrate. In addition, its interconnect reliability is maintained with the balance of shrink force of ACF binders and elastic force of compressed conductive particles^[2].

Recently the high-definition LCD panels are required, especially for mobile electronics application. However, in the case of fine pitch interconnection with conventional COG structure, the risk of the electrical short circuit failure caused by conductive particles agglomeration between adjoining gold bumps will increase^[3, 4, 5]. Even if it does not become electrical short circuit failure, conductive particles form capacitive losses between adjoining gold bump at high frequency range. Shrinking diameter of conductive particles decreases the occurrence of these problems but also decrease interconnection reliability because the elastic forces of

conductive particles is reduced. On the other hand, forming bump with larger gap and narrow bump width might decrease the occurrence of short circuit failure, but the number of trapped conductive particles that determine interconnection resistance and reliability might decrease due to narrow bump width^[3]. From these reasons, it is hard to achieve ultra fine pitch reliable COG interconnection with conventional Au bump with ACF technology.

The Resin Core Bump technology

The Resin Core Bump technology has been developed to achieve making fine and high reliable COG interconnections^[6, 7]. With 40 μ m pitch TEG (Test Element Group) modules, the Resin Core Bump with NCF interconnection has shown higher reliability than Au Bump with ACF. In addition, with 5 μ m line width and 5 μ m gap 40 μ m test vehicles, fine pitch capability up to 10 μ m pitch has been shown.

The concepts of the Resin Core Bump are listed below.

1) Bonding with Non Conductive Film (NCF)

In order to achieve the conductive particle problem free bonding, NCF is adopted instead of ACF. In addition, NCF bonding enables direct contacts between bumps and substrate pads, thus it enables obtaining larger contact area than ACF bonding. It reduces electric resistance and improves reliability. As a result, it reduces the bump size and increases the capability of fine pitch bonding. On the

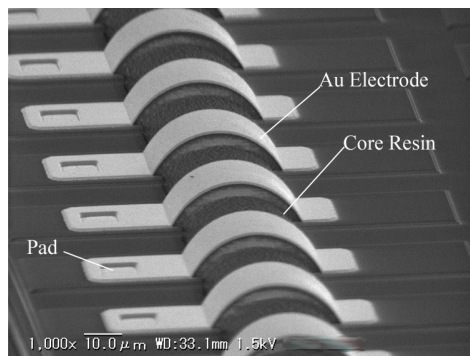


Fig. 1: SEM image of Resin Core Bump

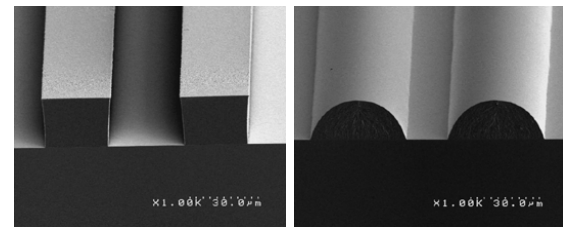
other hand, how to avoid trapping NCF at the interfaces between bumps and substrate pads is important issue of the bonding structure.

2) Resin Core with thin film electrode structure

To achieve a reliable NCF bonding, bump materials also must be changed to compliant materials because the COG bonding maintains reliability with elastic forces. Resin was applied as a core of the bump. Figure 1 shows the Resin Core Bump we developed. The Resin Core Bump is located by the side of Pad; it differs from the conventional electroplated gold bump. The core resin has semispherical topology to avoid trapping NCF between contact interfaces. Firstly bump surfaces contact very narrow line shape with the substrate, then in accordance with increasing bonding pressure, a resin core gradually deforms with excluding NCF from contact interfaces and line shape contact becomes wide rectangle contact.

The electrodes fabrication process uses a thin film process. A thick resist process for electroplating is not required. Moreover, the resist thickness do not require thicker than bump height. Thus, it improves fine pitch bumping formation capability. In addition, in case of electroplated bump process, when the bump footprint design was changed, it influences the height of the bump. There is no influence when the electrode width changed in the Resin Core Bump structure.

The conventional Au bump with ACF structure establishes interconnection with compression forces of conductive particles and summation of very small contact area, in contrast, the Resin Core Bump with NCF structure was designed to establish interconnection with compression force of a resin core and continuous large contact area. These



a) After Developed b) After Cured

Fig. 2: Cross Sectional SEM Images of after developed and after cured resin.

differences improve capability of reducing bump size especially in adjoining direction. Moreover, resin core and thin film electrode structure enables redistribution bumping only with its bumping process. It increases flexibility of circuit design and bump design.

3) Compatible with conventional bonding process

Resin Core Bump bonding process is compatible with conventional Au Bump and ACF bonding process. Physical properties of the bump were optimized to use conventional bonding infrastructures. Thus, The Resin Core Bump bonding process is able to take over conventional COG process advantages, such as short time, low cost, and lead free bonding.

The Resin Core Bumping Process

The process of the Resin Core Bump described below is a simple wafer level process.

Step 1: Core Resin formation

The fabrication process of Core resin adopted usual photolithography process. Photosensitive thermosetting resin is applied on a wafer, exposed, developed and cured. Semispherical topology is obtained with newly developed photoresist that is designed to flow and form semispherical topology during cure process. Figure 2 shows cross sectional SEM (Scanning Electron Microscope) images of after developed and cured resin patterns respectively. Because the core resin height is determined by spin coat conditions, and patterned resin becomes liquid state during the cure process, the bump height (almost core resin height) shows excellent tolerance. Especially, compared to an electroplated bump, bump heights in a wafer do not vary by the bump design. It is also an advantage over the electroplated Au Bump.

Step 2: Electrode formation

The electrode formation process uses a thin film process. That enables not only fine pitch capability, also reduction of chemical consumption and gold consumption. Firstly, Electrode materials, under bump metal (UBM) and Au; are sputtered onto the wafer. Then photo resist is coated, exposed and developed onto the wafer as etching masks. In this process, photo resist thickness is only required to cover the top of electrode. Sputtered Au and UBM are etched with wet process. Finally, photo resist is stripped.

Evaluation of Fine Pitch Interconnection

To evaluate fine pitch Resin Core bump, 20 μ m pitch and 30 μ m pitch TEG (Test Element Group) chips were designed. Especially electrodes width of Resin Core Bump was shrunk to compensate bonding equipment alignment accuracy. Shrunk electrode design has an advantage to bonding accuracy. This is not possible in conventional Au bump with ACF COG technology due to necessity of certain area to capture certain number of conductive particles.

TEG chip size was 2.1mm x 20.1mm. 20 μ m pitch and 30 μ m pitch sample were same size. Figure 3 shows schematic illustration of TEG chip. Bump layout was symmetrical, two sides peripheral and straight to imitate typical driver ICs bump design. To evaluate interconnections electrically, four-point probe traces and daisy chain traces were formed on the TEG chip. These traces were formed with electrodes of the Resin Core Bump. Figure 4 shows the schematic illustration of the trace designs of the TEG chip. Two daisy chain traces were formed in parallel also enabled dielectric evaluation as well as open mode failure. The number of bump in 20 μ m pitch TEG was 1920. The number of bump in 30 μ m pitch was 1280. The Resin core height and width were 13 μ m and 33 μ m respectively. Electrodes of the Resin Core Bump were formed with sputtered UBM (Under Bump Metal) and sputtered Au. SEM (Scanning Electro Microscope) images of TEG chips were shown in Fig. 5. Electrode widths for the Resin Core Bump were varied as shown in Table 1. Electrodes of glass substrates were formed with sputtered Contact Metal and ITO (Indium Tin Oxides). Substrates bonding pad widths are also shown in Table 1. Each

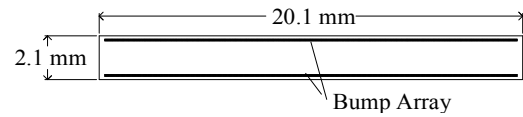
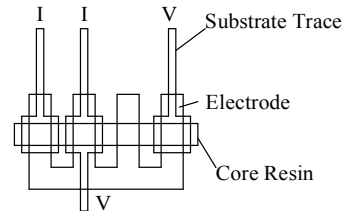
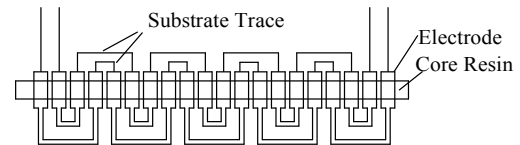


Fig. 3 : Schematic illustration of TEG Chip



a) Schematic Illustration of Four Points Traces



b) Schematic Illustration of Daisy Chain Traces

Fig. 4: Schematic Illustrations of TEG Chip Traces

Table 1 : Line and Space of Electrodes

	Bump Line/Space (L/S)	Substrate Pad Width
20 μ m Pitch	5 μ m/15 μ m	10 μ m
	10 μ m/10 μ m	
30 μ m Pitch	10 μ m/20 μ m	20 μ m
	20 μ m/10 μ m	

pad gap was 10 μ m.

Bonding was performed with conventional COG process and equipment; a NCF was attached on a glass substrate, a chip was aligned to the substrate and pre-bonded with moderate temperature that NCF viscosity became low, and then thermo-compression bonding was processed with a constant heat tool. The bonding force was 2.25 g/bump at 5 μ m width, 4.50g/bump at 10 μ m width and 9.00g/bump at 20 μ m width. In this evaluation, bonding equipment alignment accuracy was 5 μ m in 3sigma.

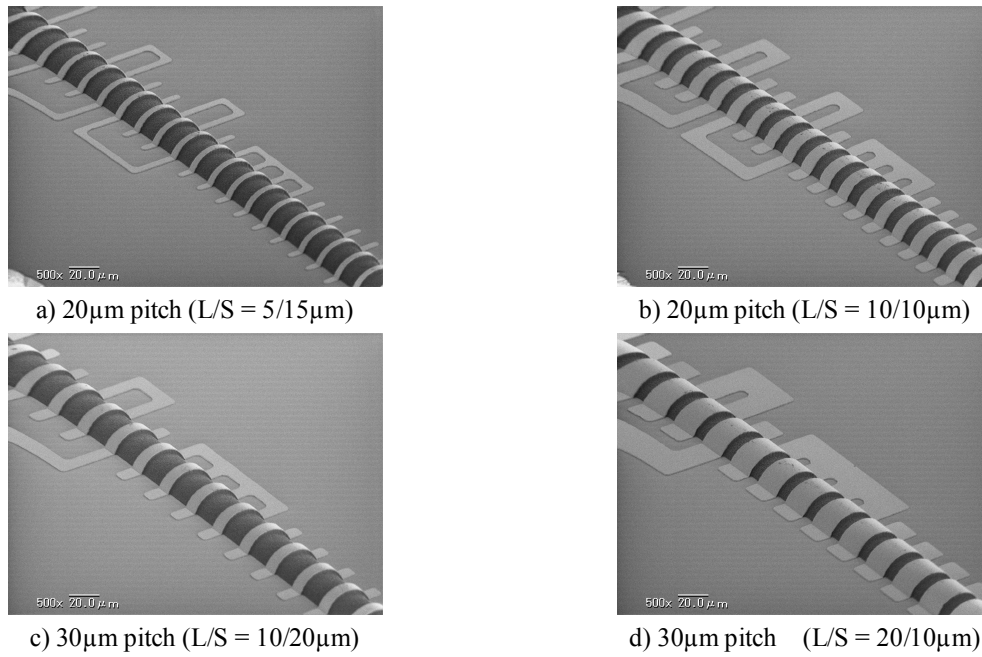


Fig. 5: SEM image of Resin Core bump on TEG chip

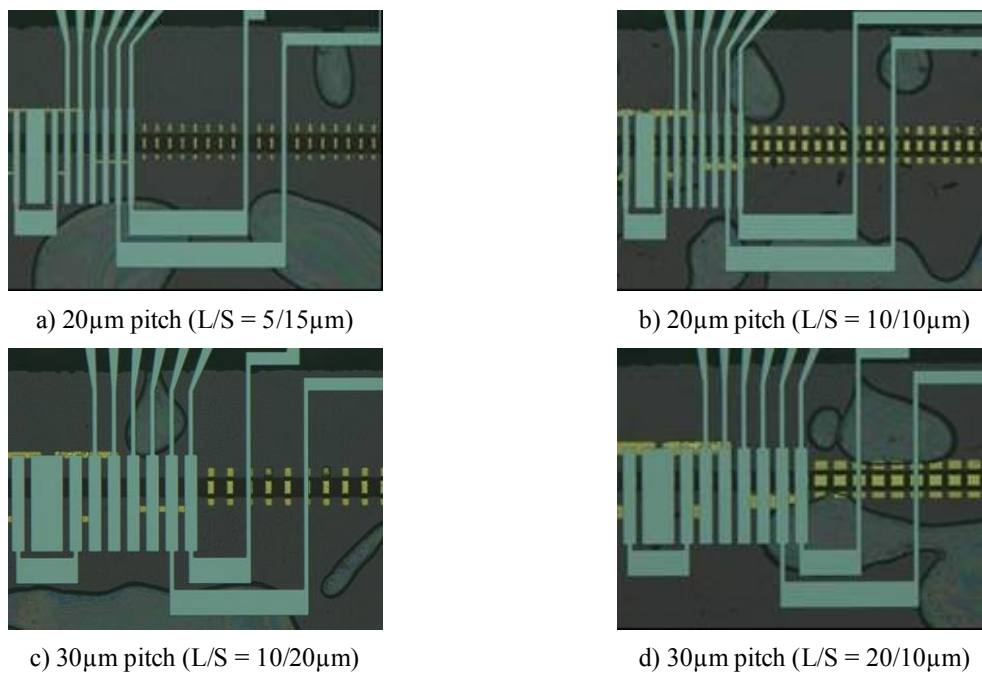


Fig. 6: Microscope images of the Resin Core bump after COG bonding

Appearances of bonded interfaces were observed by a microscope. Microscope images were shown in Fig. 6. There was no miss alignment to cause a short circuit failure. The Resin Core Bump was deformed and forms good facial contact interfaces between the Resin Core Bump electrodes and the glass substrate. Open mode failure was checked with daisy chain patterns. There were no failed observed. Interconnect resistance was measured with the 4-point probe measurement patterns. Figure 7 shows interconnection resistance results. Figure 8 shows an image of measurement locations in a chip. Results of average resistance are summarized in Table 2. Because the measurement results included resistance of ITO trace, absolute resistances were higher. Moreover the substrate trace width of 20 μm pitch was narrower than that of 30 μm pitch; absolute resistance of 20 μm was higher than 30 μm pitch. Results showed quite stable until 20 μm pitch/10 μm width sample. Although 20 μm pitch/5 μm width result was 4.28 Ω in 3sigma, compared with 5.7 Ω in 3sigma of 40 μm pitch Au bump + ACF structure result [6, 7], 20 μm pitch/5 μm width still showed advantage to the conventional COG structure.

Reliability Evaluation

Fine pitch interconnection reliability was evaluated with thermal cycle test and thermal humidity bias test.

Thermal Cycle Test

Thermal cycle reliability test of Resin Core bump in COG modules was performed. The temperature condition was from -40°C to 80°C and dwell time was 30min in each temperature. Resistances were measured at 100, 250, 500, 750, 1000, 1500 and 2000 cycles. The test results of resistance increments through the test are shown in Fig. 9. Resistance was raised in accordance with both electrode width and bump pitch were decreased. The sample of the largest increment of resistance was 20 μm pitch /5 μm width sample. But the maximum increment of resistance was under 2.0 Ω . Figure 10 shows appearances of the bonded interfaces after thermal cycle test. Compared with initial state, NCF was turned dark because of the heat of thermal cycle,

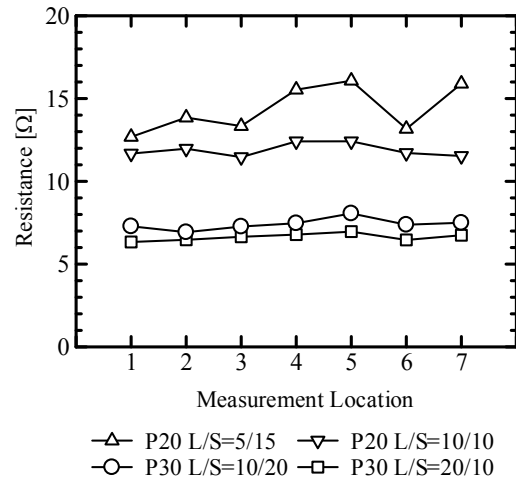


Fig. 7 : Test Result of Initial Contact Resistance

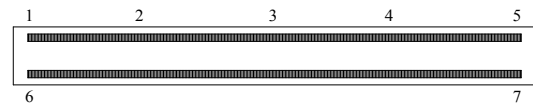


Fig. 8 : Schematic illustration of four-point measurement locations

Table 2: Interconnect Resistance Results

	20 μm pitch		30 μm pitch	
	5/15	10/10	10/20	20/10
Ave.	14.37	11.89	7.42	6.63
3 σ	4.28	1.19	1.03	0.66

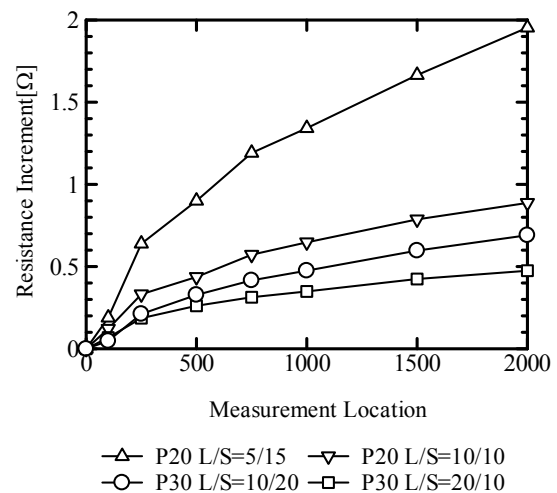


Fig. 9: Figure of Thermal Cycle Test Result

but the size of the contact didn't show significant changes. Figure 11 shows the cross sectional SEM image of 20 μm pitch samples interconnections. Core resins were deformed and electrodes and substrates were contacted.

Thermal Humidity Bias Test

Reliability for electrochemical-migration on the glass was evaluated with thermal humidity bias test. Evaluation was performed with 20 μm pitch TEG sample. Bias of 5V (0.5V/ μm) was added between the parallel daisy chain traces. Test condition was 85%/85°C R.H. Figure 12 shows the measurement result of dielectric resistance until 500 hours.

Dielectric resistance kept over 1M Ω .

Conclusion

We evaluated fine pitch Resin Core Bump COG bonding with 20 μm and 30 μm pitch TEG. Electrode width and space was varied to evaluate bonding alignment error compensation. Even 5 μm electrode width TEG chip showed excellent interconnection reliability through the thermal cycle test. Electrochemical-migration reliability was evaluated with 20 μm pitch TEG. There was no failure occurred by 500 hours.

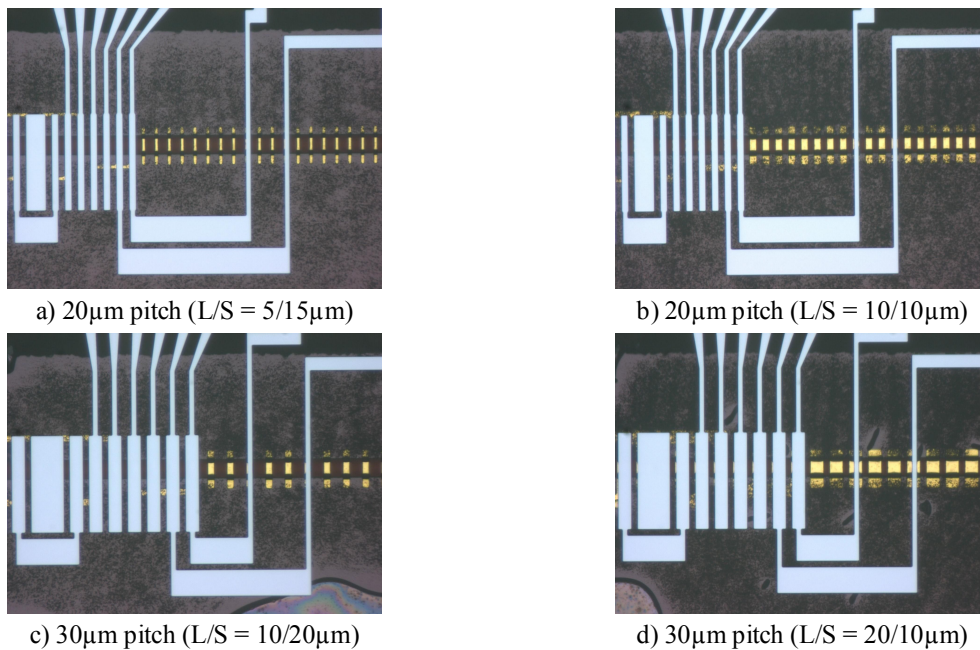


Fig. 10: Bonding Appearances after Thermal Cycle Test

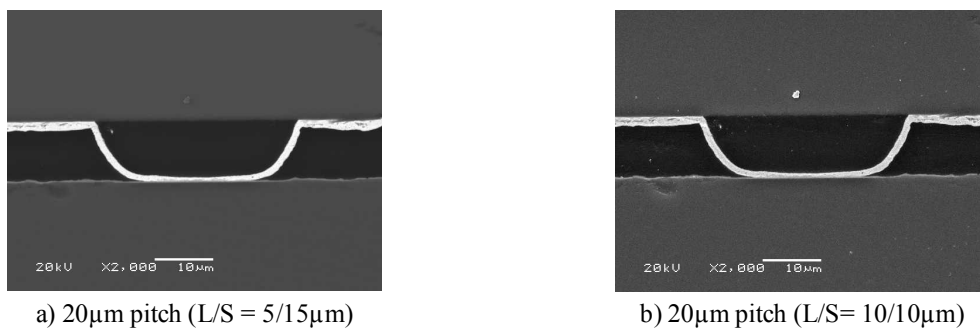


Fig. 11: Cross Sectional SEM Images of 20 μm pitch interconnection after 2000 thermal cycles

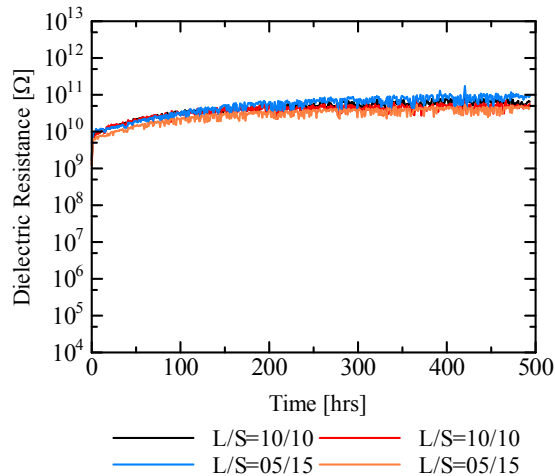


Fig. 12: Dielectric Resistance measurement result of 85°C/85% R.H. Thermal Humidity Bias Test

reliable COG (Chip On Glass) interconnection technology", Proceeding of Micro Electronics Symposium (MES) 2007, pp.51-54

[7] S. Tanaka et al, "The Resin Core Bump Technology for COG (Chip on Glass) application", Proceeding of IMAPS 2007, pp.1084-1089

References

- [1] M. Masuda et al, "Chip on Glass Technology for Large Capacity and High Resolution LCD", Proceeding of the 1989 Japan IEMT Symposium, pp.57-60
- [2] H. Nishida et al, "Micro-pitch connection using anisotropic conductive materials for driver IC attachment to a liquid crystal display", IBM Journal of Research and Development, Volume 42, Numbers 3/4, 1998.
- [3] M.J. Yim et al, "Anisotropic conductive films (ACFs) for ultra-fine pitch Chip-On-Glass (COG) applications", International Journal of Adhesion and Adhesives Volume 27, Issue 1, January 2007, Pages 77-84.
- [4] Y. W. Chiu et al, "Study of short-circuiting between adjacent joints under electric field effects in fine pitch anisotropic conductive adhesive interconnects", Microelectronics Reliability, Volume 42, Issue 12, December 2002, Pages 1945-1951.
- [5] M. J. Yim et al, "Recent advances on anisotropic conductive adhesives (ACAs) for flat panel displays and semiconductor packaging applications", International Journal of Adhesion and Adhesives, Volume 26, Issue 5, August 2006, Pages 304-313.
- [6] S. Tanaka et al, "Fine pitch capable and high