

Packaging Technology for Recent Notebook PCs

Ryo Kanai, Naoki Nakamura, and Shigeru Sugino

Fujitsu Advanced Technologies Limited

1-1, Kamikodanaka 4-chome, Nakahara-ku,

Kawasaki-si, Kanagawa-ken 211-8588, JAPAN

Phone: +81-44-754-2191

E-mail: kanai_ryo@jp.fujitsu.com, nakamura.naoki@jp.fujitsu.com, sugino@jp.fujitsu.com

Abstract

Along with increasing global demand for notebook PCs, there seems to be no end to the need for making highly-mobile multi-purpose notebook PCs that are lighter and smaller than the last generation. One of several measures for decreasing the size and weight is a packaging technology approach using thinner and downsized components, such as packages, printed wiring boards (PWBs), connectors, and sockets. Within this context, this paper focuses on packaging technology problems attributable especially to PWBs. PWB warpage greatly affects the packaging process and is an important factor in achieving higher output quality during production. The occurrence of any defective products results in extra costs, such as for correcting the defects manually, which increases the price of the finished products. To avoid this problem and reduce costs, an environment that enables efficient packaging work must be established.

To prevent the occurrence of product defects, we measured PWB warpage and attempted to eliminate problems that were caused by the design. PWB warpage was evaluated with measuring equipment using shadow moiré technology. Although warpage is a hard problem to solve because it involves multiple factors, we show in this paper that adequate solutions can be found based on an understanding of the observations from our warpage evaluations. In an example discussed in the paper, the PWB design was adjusted to enable significant improvements in output quality during production.

Key words: Packaging Assembly, PC, Printed Wiring Board

1. Introduction

1.1 Contribution of packaging technology to reductions in weight and size

There is high demand for weight and size reductions for the latest mobile devices, including portable multi-purpose notebook PCs. For this reason, increasingly smaller and thinner components are mounted in these devices.

From the viewpoint of consumers, however, it is also important that these devices will become cheaper. In order to meet these expectations, the purchased parts in general purchasing processes must become cheaper, and the persons in charge of

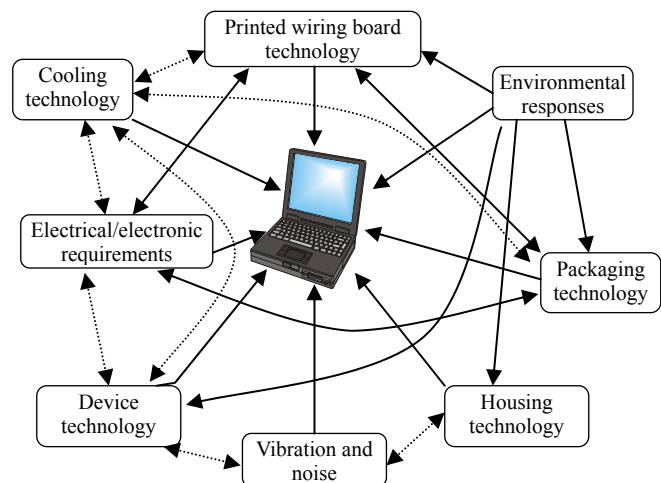


Figure 1: Peripheral technologies for Notebook PCs.

device design and production must also realize improvements in the output quality during production.

1.2 Role of packaging technology

As shown in Figure 1, the development of notebook PCs is intimately connected to various secondary technologies.[1]

Among these secondary technologies, printed wiring board technology and packaging technology serve as the main "engine" in the drive to downsize devices and make them more lightweight.

2. PWB warpage from the perspective of packaging technology

2.1 Circumstances surrounding PWB warpage

This paper mainly discusses PWB warpage.

Problems from warpage occurrence become evident, for example, in package downsizing. Pins have less distance between them. The shortest distance between pins currently used in our products is about 0.6 mm in BGA packages. The whole industry expects packages to continue to have smaller pitches, reaching a BGA solder ball pitch of 0.5 mm.[2]

In this case, the solder ball diameter in the

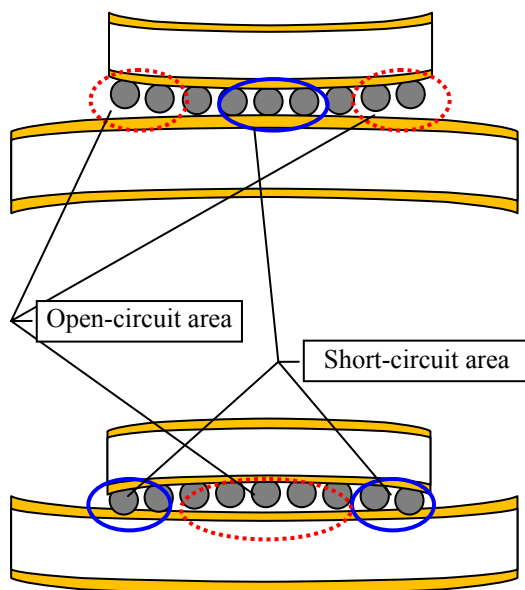


Figure 2: Effects of warpage.

mounted package will probably have a downscaled dimension of about 0.25 mm. This means that the distance between the PWB and package would be 50 μm less than that of today. It also means that the allowable distance for warpage will be shorter by 50 μm , increasing the risk of open circuits and short circuits.

The smaller pitches of connectors and other package parts mounted on PWBs will cause the same problem. In addition, lead-free packaging at high temperatures causes PWB warpage.

To obtain stability in quality from the perspective of packaging technology, more consideration than ever before must be given to the application of thinner and more-lightweight parts.

2.2 Non-wetting and short circuits caused by PWB warpage

The problems actually caused by the occurrence of PWB warpage are open circuits and short circuits. Open circuits occurs with a large distance between the PWB and a mounted part; conversely, a short circuit occurs with a small distance between them (Figure 2).

2.3 Causes of PWB warpage

The causes of PWB warpage can be roughly classified into factors in PWB manufacturing, factors in packaging, and factors in designing.

This paper focuses on design factors.

3. Description of Evaluation

3.1 Evaluation equipment

This equipment uses measurement principles based on shadow moiré, and it uses phase stepping for increased precision in monitoring moiré fringes.[3] Figure 3 shows the appearance of the equipment, and Figure 4 shows the measuring mechanism of the equipment.

3.2 Evaluation conditions

PWBs without any mounted parts were used as evaluation samples.

For preprocessing, the PWBs were baked at 115°C for two hours.

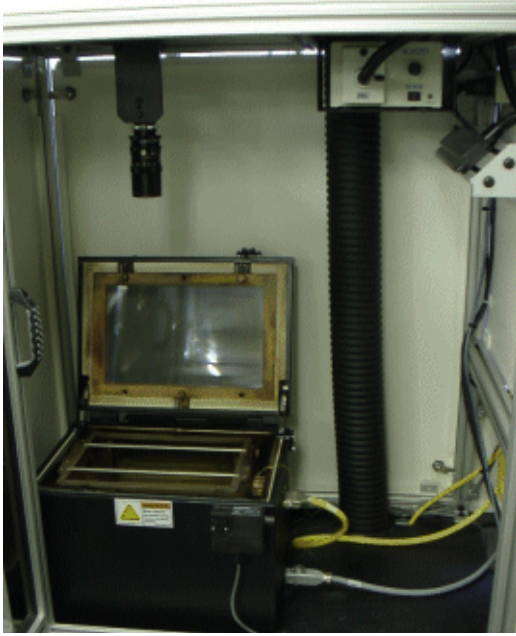


Figure 3: Measurement equipment using shadow moiré.

Each sample was heated at a temperature increasing at a rate of about $0.3^{\circ}\text{C}/\text{second}$, and cooled at a rate of about $0.5^{\circ}\text{C}/\text{second}$. Warpage was measured when the surface temperature of the PWB was 220°C .

3.3 Necessity of understanding the characteristics of the warpage measuring equipment

As shown in Figure 4, this equipment is configured such that the sample is heated by the

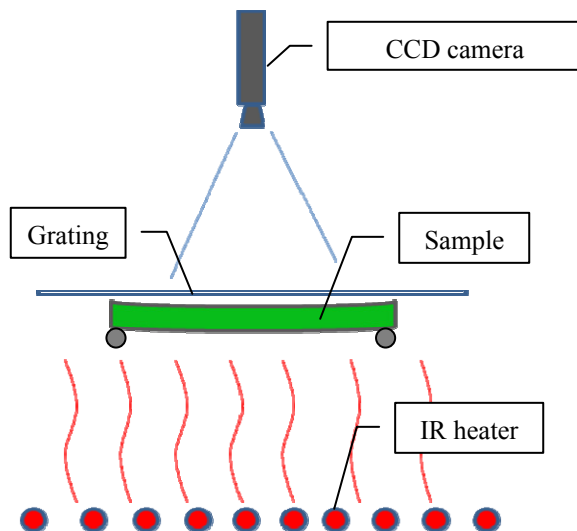


Figure 4: Warpage measuring mechanism.

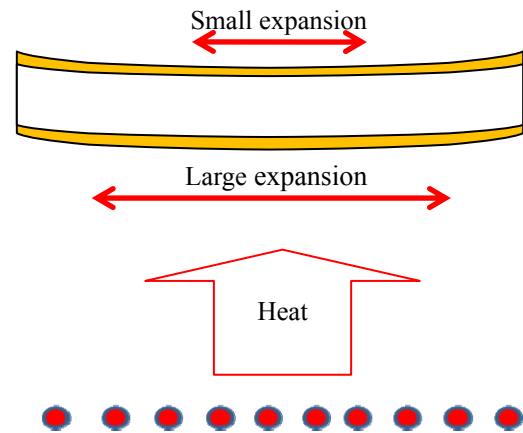


Figure 5: Warpage measuring mechanism.

heater beneath it and filmed by the camera above it.

Because of the characteristics of this equipment, there is a temperature difference between the top and bottom of the heated sample. Figure 5 shows that thermal expansion on the heater side is greater than on the other side (observation side). This may cause an error in the PWB warpage measurement results.

Because of this concern, we performed a confirmation test.

In this test, we evaluated the warpage of a PWB designed for the simplest configuration, and evaluated the characteristics of the warpage measuring equipment itself.

3.4 Confirming the characteristics of the warpage measuring equipment

Evaluation conditions

- PWB: FR-4
- Thickness: 1.0 mm
- Size of the measurement range: 230 x 170 mm
- Number of layers: Double-sided board
- Copper foil thickness: 35 μm
- Design of copper: Copper plain
- Temperature conditions: Room temperature $\rightarrow$ 255°C $\rightarrow$ 180°C (Figure 6)
- Warpage measurement temperature: 220°C (PWB surface temperature)

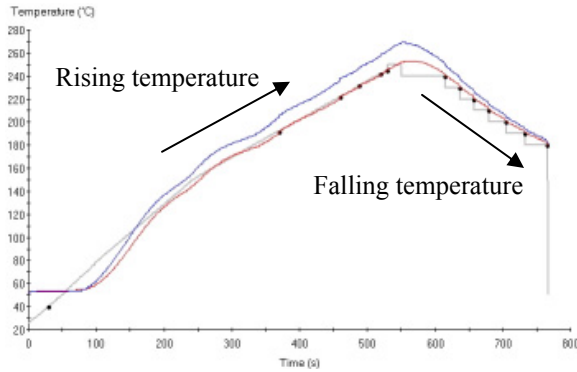


Figure 6: Evaluation profile.

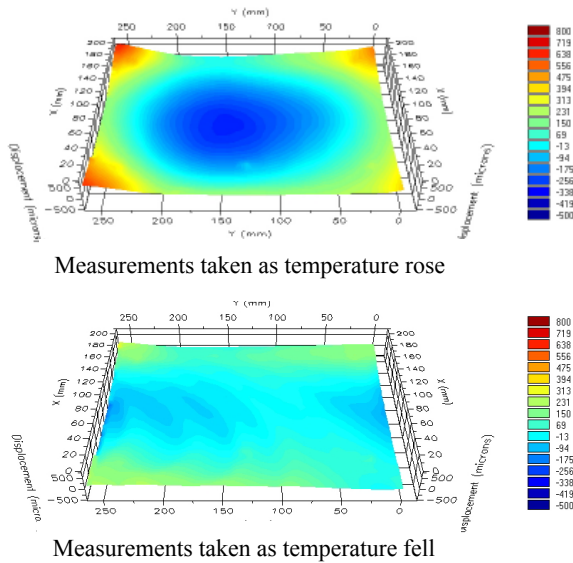


Figure 7: Effect of warpage.

Warpage was evaluated with the above sample.

With the surface of the evaluation PWB arranged in a solid copper pattern, the evaluation results shown in Figure 7 could be obtained.

As the temperature rose (heated from under the PWB), thermal expansion on the back side became dominant. We confirmed characteristic concave warpage in the downward direction at the center and convex warpage in the upward direction at the four corners of the PWB.

We confirmed that the PWB returned to the flat state in measurements taken at the same temperatures as the temperature fell.

The results show that relatively good results can be obtained by measuring warpage as the temperature falls.

3.5 Evaluation results of a PWB for products (Evaluation conditions)

- PWB material : FR-4
- Thickness: 0.6 mm (PWB for a HDD device)
- Size of the measurement range: 23 x 14 mm
- Number of layers: 4-layer board
- Copper foil thickness: Internal layer, 18 μ m copper thickness with plating on the surface
- Surface copper design: Product design
- Temperature conditions: Room temperature $\rightarrow$ 255°C $\rightarrow$ 180°C
- Warpage measurement temperature: 220°C (PWB surface temperature measured as the temperature falls)

PWB warpage was evaluated in the same way on both the front and back sides to check for changes in warpage characteristics (convex or concave direction of warpage).

Actual products were used as evaluation samples. Figures 8 to 11 show the results.

Figures 8 and 9 show the measurement results for the L1 side (Figure 8) and L4 side (Figure 9) of a PWB from the same vendor.

Figures 10 and 11 show the measurement results for the L1 side (Figure 10) and L4 side (Figure 11) of a PWB from another vendor.

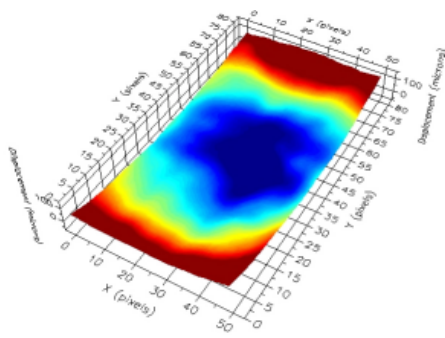
The evaluation results are as follows: in a comparison of the shapes of the L1 and L4 sides between both vendors, the L4 side for either vendor became convex, and the shapes show relatively the same contours.

Table 1 lists figures showing the coplanarity.

We thus confirmed that this evaluation method can be used to measure warpage regardless of whether it is on the front or back of a PWB.

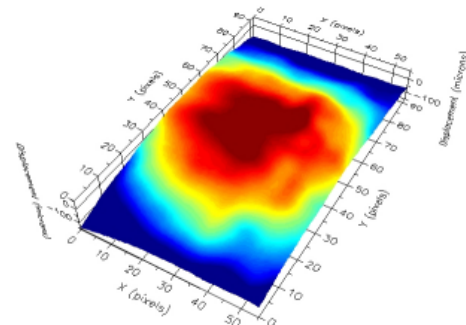
Table 1: Coplanarity comparison.

	L1 side	L4 side	Ratio (L1/L4)
Vendor A	199 μ m	194 μ m	102.6%
Vendor B	188 μ m	206 μ m	91.3%



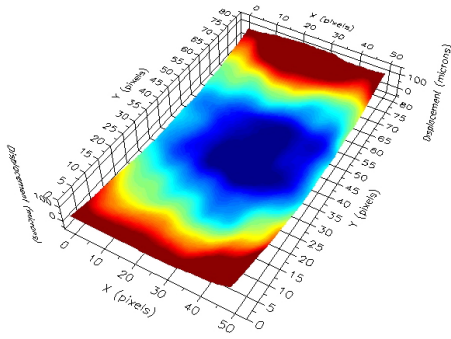
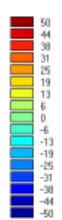
Coplanarity = 199 microns

Figure 8: Warpage (L1 side, vendor A).



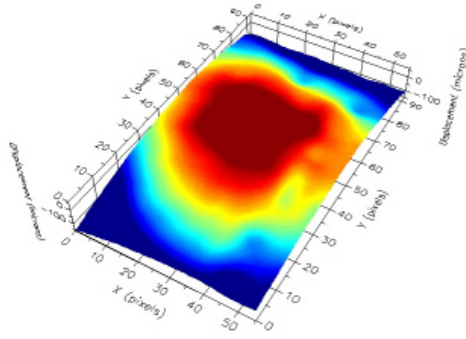
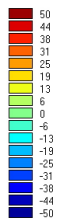
Coplanarity = 194 microns

Figure 9: Warpage (L4 side, vendor A).



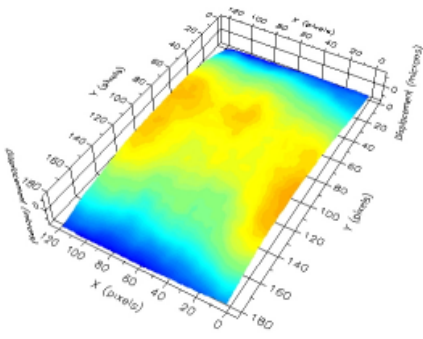
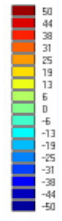
Coplanarity = 188 microns

Figure 10: Warpage (L1 side, vendor B).



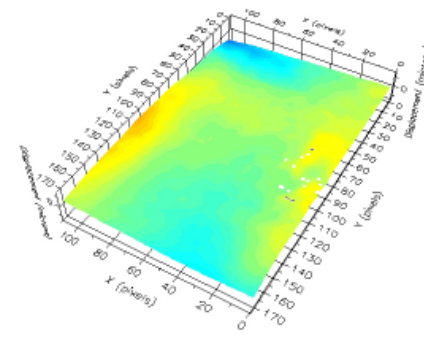
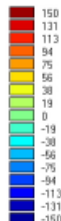
Coplanarity = 206 microns

Figure 11: Warpage (L4 side, vendor B).



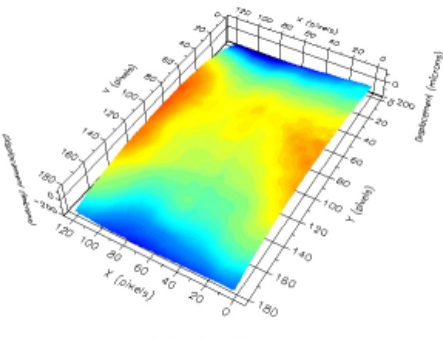
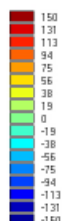
Coplanarity = 204 microns

Figure 12: Warpage (development stage 1, vendor C).



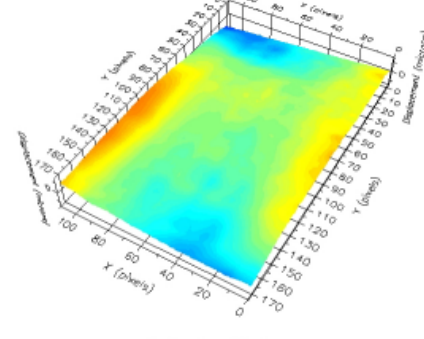
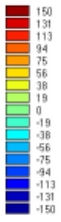
Coplanarity = 157 microns

Figure 13: Warpage (development stage 2, vendor C).



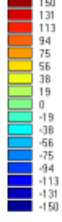
Coplanarity = 255 microns

Figure 14: Warpage (development stage 1, vendor D).



Coplanarity = 188 microns

Figure 15: Warpage (development stage 2, vendor D).



3.6 Example of warpage evaluation applied to product development

- Evaluation conditions
 - PWB: FR-4
 - Thickness: 1.0 mm
 - Size of the measurement range: 70 x 45 mm
 - Number of layers: 6-layer board
 - Copper foil thickness: Internal layer, 18 μ m
 - copper thickness with plating on the surface
 - Surface copper design: Product design
 - Temperature conditions: Room temperature -> 255°C -> 180°C
 - Warpage measurement temperature: 220°C (PWB surface temperature measured as the temperature falls)

In the following example, warpage evaluation was applied to the development of PWBs in actual products for notebook PCs.

Figures 12 and 13 show the measurement results for PWBs from the same vendor at each development stage.

Figures 14 and 15 show the measurement results for PWBs from another vendor at each development stage.

Warpage was evaluated at development stage 1. As shown in Figures 12 and 14, we confirmed that warpage tended to be downward at the sides of the PWB and upward at the center of the PWB. We changed the design accordingly. We mainly changed the design of the copper pattern layout so that the neutral axis is at the center of the PWB thickness.

As a result of the design change, circumstances could improve such that the both vendors' PWBs (Figures 13 and 15) at development stage 2 showed relatively even contours all across the observed surfaces.

The design change also significantly improved the packaging quality.

We thus confirmed that an evaluation of such warpage at an early stage of product PWB development can produce improvements that will be properly reflected in products specifications and that good packaging quality can be obtained at the next development stage.

4. Conclusion

We have determined the characteristics of a suitable warpage measurement method to apply.

Under the conditions described, we could check the warpage attributable to poor packaging and make improvements at the development stage of our products.

References

- [1] Ryo KANAI, Yoshikazu HIRANO, "Packaging Technology for Slim Note-PC", Journal of Japan Institute of Electronics Packaging, Vol. 3, No. 3 pp. 194-197, May 2000.
- [2] Y. Wang and P. Hassell, "Measurement of Thermal Deformation of BGA Using Phase-shifting Shadow Moiré", Experimental/Numerical Mechanics in Electronic Packaging, Volume 2, pp. 32-39, Society for Experimental Mechanics, Inc., 1998.
- [3] "Assembly & Packaging of ITRS 2007 Edition", ITRS, The International Technology Roadmap for Semiconductors, April 3, 2008.
http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_Assembly.pdf