

Electrochemical Process for Through Via 3D SiP without CMP and Lithographic Processes

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Abstract

A serial electrochemical process consist of copper via filling, electropolishing, electroless copper plating and electroless tin plating is presented for the TSV 3D SiP application. Defect-free copper via filling was achieved by controlling current modes and additives. After via filling, electropolishing was performed to planarize over-plated copper. Electropolishing within the potential of mass-transfer region and with the assistance of additives, fine polished surface without thickness disparity was achieved. For bump formation process, electroless copper and tin plating which is a self-aligned process was applied. Consequently, Cu/Sn bump on via patterned wafer was obtain without using the conventional CMP and lithographic processes.

Key words: TSV 3D SiP, copper via filling, electropolishing, electroless Cu/Sn bump

As electronic systems such as portable computers and mobile phones get smaller in its size and lighter in its weight and faster in its speed, the attention on packaging technologies of microelectronic components grew up immensely[1-3]. Among these microelectronic packaging technologies the current Three-Dimensional System in Package (3D SiP), in which multiple active and passive LSI chips are stacked vertically, is attracting attention as a means of greatly reducing the mounting area of electronic components to improve system performance while reducing system size. There are several kinds of methods for chip stacking, but the stacking and interconnection through Cu filled through-hole via is considered to be one of the most advanced stacking technologies[4-5]. Through via 3D SiP is competitive over other chip stacking technologies with several decisive benefits. Connection lengths can be as short as the thickness of a chip. High density, high aspect ratio connections are available. Through via interconnections also overcome the RC delays and reduce power consumption by bringing out-of-plane logic blocks much closer electrically.

A typical through copper via chip stacking process is consist of through via formation on Si wafer by Deep-RIE, barrier and seed layer deposition by IMP sputtering, copper via filling by electroplating, wafer thinning by overplated copper CMP and back side grinding, planar Cu/Sn bump formation by electroplating and finally chip stacking. However, this conventional process (Fig. 1) has many disadvantages during CMP and Cu/Sn bump

formation. For overplated copper CMP, the demerits are scratch and damage on copper surface, mechanical stress on substrate, high process cost and long process time[6-7]. The planar Cu/Sn bump formation, the conventional electroplating method followed by lithographic process, also has problems such as high cost due to the high production cost of mask, align difficulties due to the minute via patterns.

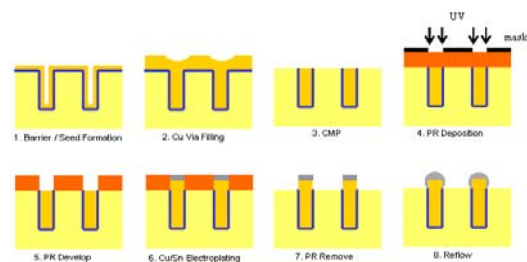


Fig. 1. Conventional Cu/Sn bump formation process.



Fig. 2. Proposed electroless Cu/Sn bump formation process.

Here we developed a new serial electrochemical process to overcome the disadvantages of CMP and lithographic processes. (Fig. 2) In this new process copper electropolishing was applied as a replacement of CMP process and electroless copper, tin plating

was applied as a replacement of the conventional Cu/Sn bump formation process. Copper electropolishing is a scratch-free, damage-free and proposed process is a serial electrochemical process which lowers the total process cost and time efficiently due to the equipment compatible between all processes.

Experimental Procedures

The patterned silicon wafers of via holes (50 μm in diameter and 170~190 μm in depth, 20 μm in diameter and 100 μm in depth) fabricated by DRIE were used in this research. Ta layer with 200 nm thickness as the diffusion barrier and adhesion promoter, and Cu layer with 700 nm thickness as the seed layer were deposited using ionized metal plasma sputtering method. Subsequently, the wafers were electroplated with copper in an electrolyte consisting of copper sulfate, sulfuric acid and various organic additives, e.g. polyethylene glycol (PEG), chloride ions (Cl^-), bis(3-sulfopropyl) disulfide (SPS), Janus green B (JGB). After electroplating, the wafers were electropolished in a phosphoric acid bath with additives, acetic acid and glycerol, under galvanostatic control at room temperature and the stirring speed was fixed at 400 rpm. During electroplating and electropolishing, analysis of the electrochemical behaviors of electrolytes the galvanostatic measurements were performed by EG&G potentiostat/galvanostat 273A. The surface and cross-sectional morphologies after electroplating and electropolishing were observed using optical microscope (OM) and scanning electron microscope (SEM).

Table 1. Composition of electroless Cu bath.

Chemical components	Conc.
Cu source	10g/L
Reducing agent (HCHO)	10mℓ/L
Complexing agent (EDTA)	40g/L
Bath conditions	
pH adjuster	NaOH (12.8)
Temperature	60°C

After electropolishing, electroless copper plating was performed. The bath composition and condition of this work is listed in Table 1. For the copper source, copper sulfate was used and for complexing

stress-free process. Electroless copper, tin plating is a non-lithographic self-aligned process. Above all, this

agent, EDTA was used. The pH of the bath was fixed at the value of 12.8 which is reported by previous researchers to be a value where the deposition rate of copper is uniform and independent to pH value[8]. The selective deposition of electroless copper plating depends on the substrate and pre-activation[9]. PdCl_2 was used to activate copper surface and to remove copper oxide the specimen was pretreated in 10% H_2SO_4 .

After electroless copper plating, electroless tin plating was performed. The bath composition of this work is on Table 3. To determine the deposition thickness of electroless tin plating, plating on flat substrate (electroplated copper on flat brass) was performed before plating on via patterned wafers.

The plating temperature was fixed at 80 °C where the deprotonation by hypophosphite occurs most actively. After selective electroless tin plating on electroless copper bumps, tin reflow was performed to ball-up the Cu/Sn bumps. The reflow was operated at 270 °C for 20 seconds. After reflow, the specimens were rinsed with trichloroethylene for 60 seconds to remove the remaining flux.

Table 2. Composition of Electroless Sn bath

Chemical components	Conc.
Stannous sulfate(SnSO_4)	28.0 g/L
Sodium hypophosphite(NaH_2PO_2)	100 g/L
Thiourea (Tu)	80 g/L
Sulfuric acid(H_2SO_4)	77.5 g/L

Results and Discussion

The effects of additives and current modes on copper via filling were examined. The effects are shown in Fig. 3 and 4. Voids are formed inside the via when direct current was applied without additives as shown in Fig. 3. (a) and 4. (a). Due to the converged current at the via entrance, more rapid deposition at the via entrance than at the bottom of the via cause the entrance to be blocked before the via was fully filled with copper. The void-free via was obtained when pulse-reverse current was applied with additives. The additives played roles of gradient plating kinetics inside the vias. The concentration of accelerator, SPS, is higher at the inside of via and the concentration of inhibitor, PEG, is higher at the

entrance. Also the copper dissolution at the via entrance during reverse current keeps the via open during copper electroplating. The complete filling profiles using pulse-reverse current with full additives are shown in Fig. 3. (c) and Fig. 4. (b).

The galvanostatic results of electropolishing with various constant current densities are shown in Fig. 5. The potential starts at a low value and suddenly rises to a high value. This surge in potential demonstrates the formation of boundary layer between anode/electrolyte interface and also indicates the conversion of rate controlling reaction from surface reaction to diffusion limit. Once this surge in potential occurs, the potential remains constant due to the steady state diffusion controlling reaction. The time to form the boundary layer is a strong function of applied current density. As the applied current density increases the time to form the boundary layer decreases. The effects of additives on planarization are shown in Fig. 6. The electrolyte containing acetic acid accelerates the dissolution of copper. On the contrary glycerol suppresses the dissolution of copper. The formation of a significant gradient of copper dissolution rate within the via feature caused by the two additives in the phosphoric acid bath enhances the planarization efficiency during electropolishing. Fig. 6. (b) shows the enhanced planarization after electropolishing with additives.

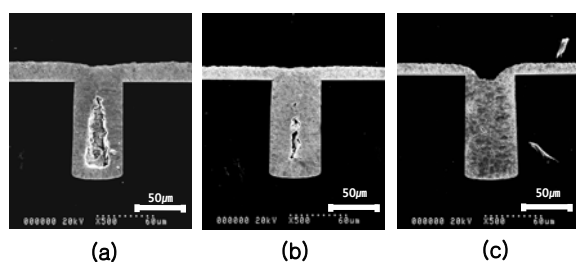


Fig. 3. Cross-sectional view of 50 μm diameter via. (a) DC current & no additives, (b) PRC current & no additives, (c) PRC current & full additives.

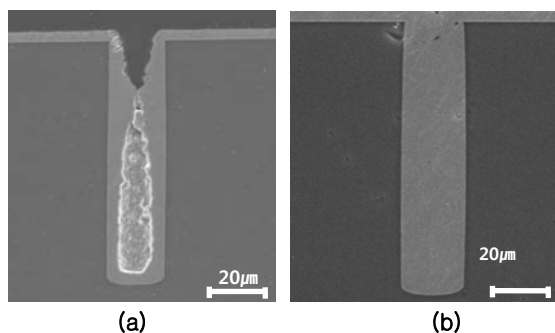


Fig. 4. Cross-sectional view of 20 μm diameter via. (a) DC current & no additives, (b) PRC current & full additives.

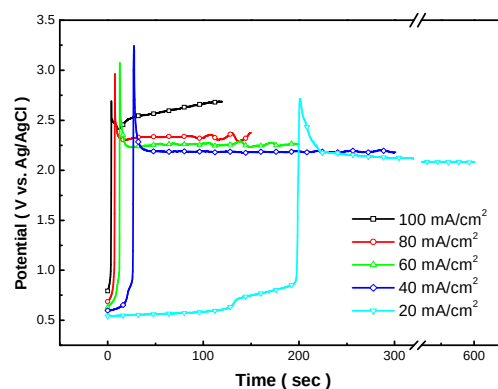


Fig. 5. Effect of applied current density on the electrode potential with time.

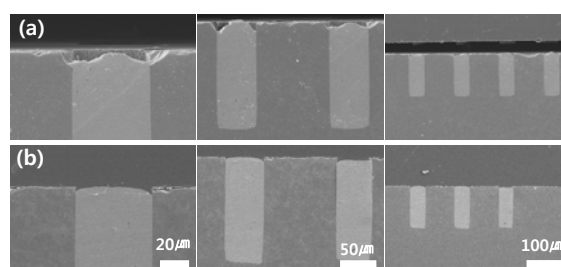


Fig. 6. The effects of additives on planarization. Electropolishing (a) with no additives (b) with additives.

Selective copper bump formation by electroless plating method is expected due to the patterned surface of the wafer after electropolishing. After overplated copper removal, the wafer surface is patterned as copper surface on via hole and tantalum surface on outside of via hole. Native oxides are formed easily on both metal surfaces but, during acid cleaning copper oxide is preferentially etched compared to tantalum oxide. This provides selectiveness for electroless copper bump formation. Before immersing into the plating bath, the specimens are activated in palladium chloride solution. In general, electroless copper deposition occurs only on activated surface. Tantalum oxide obstructs the displacement reaction between palladium ions and barrier layer providing selective activated sites on copper via hole. However, in spite of this electroless copper plating basics, plating results after only activation treatment were unsatisfactory. No selectiveness was observed as shown in Fig. 7 (a). To enhance the selective copper deposition, stabilizer (2,2-bipyridyl) was added in the plating bath. 2,2-bipyridyl delays the autolysis reaction of the electrolyte and enhances uniformity of the electroless copper plated layer. Fig. 7 (b) shows the effect of stabilizer added in the plating bath. Selective copper deposition was obtained but still copper islands were observed on tantalum oxide

surface. To eliminate this, additional acid cleaning treatment was performed after activation. Fig. 7 (c) is the result of electroless copper bump formation using stabilizer containing bath after acid cleaning. The plating time was 90 minutes.

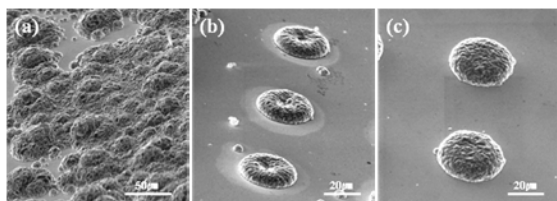


Fig. 7. SEM image of electroless Cu bump (a) No additives, (b) effect of stabilizer, (c) effect of stabilizer & acid cleaning.

Tin electroless plating is consist of displacement process and reduction process[10]. To determine the plating time, electroless tin plating on flat substrate was performed prior to the plating on copper bump formed specimens. Fig. 8 shows that for 4 hours plating the thickness of electroless plated tin increase to $\sim 8\mu\text{m}$. But, the cross-sectional image shown in Fig. 8 (a) indicates poor uniformity of deposited tin layer. This profile is also observed when electroless tin plating was performed on via patterned wafers. However, after the reflow process the tin on electroless copper bumps made a ball-up feature. So, it may be assumed that the poor uniformity of tin deposits before reflow process has little effect on forming the proposed Cu/Sn bump. If the plated amount of tin is equal the height of the final Cu/Sn bump is expected to be equal. The results are shown in Fig. 9.

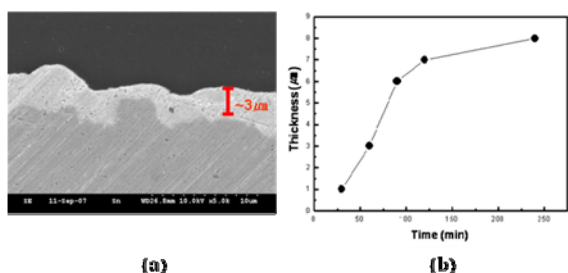


Fig. 8. Electroless Sn plating cross-sectional results. (a) Electroless Sn plating 1hr, (b) Thickness of Sn layer as time.

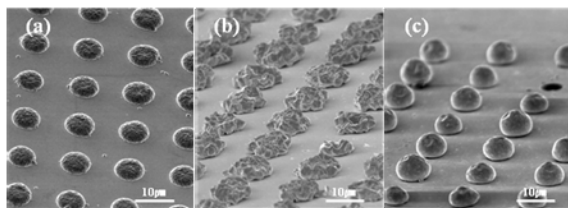


Fig. 9. SEM image of each process. (a) electroless Cu bump, (b) electroless Sn plating, (c) reflow

Conclusions

To obtain defect free via filling, pulse-reverse plating method was applied with proper concentration of additives. The electrochemical etching of via entrance during reverse current can keep via open. Electropolishing process can replace high cost CMP process in the removal of overplated copper on through vias. Efficient polishing can be achieved within the potential range where the dissolution of copper is controlled by diffusion through the anode/electrolyte boundary layer. Combined effect of acid and alcohol additives assist planarization of overplated copper by eliminating thickness disparity during electropolishing. The optimized conditions for electroless copper bump are 1 minute activation, acid cleaning and plating in stabilizer containing bath for 1 hour and 30 minutes. For uniform bump formation, the amount of plated tin is important. After 2 hours of plating time and 20 seconds reflow at 270°C , Cu/Sn bump with $\sim 10\mu\text{m}$ height was achieved. A new serial electrochemical process is expected to overcome the disadvantages of CMP and lithographic processes. Also equipment compatible between all processes can lower the total process cost and time efficiently.

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