

Materials and Process Selection for High Frequency Flip Chip

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Abstract

Flip chip has since decades been the primary choice for chip interconnect for high performance circuits. Over the last few years, interest from the microwave arena has increased, and at this point in time microwave flip chip is a possible option for volume production.

Three groups of experiments are reported. The first experiments are on stud bumping thin film substrates for subsequent flip chip bonding. The wire was 17- μm diameter Au/Pd and bumping was uniform and successful, after some initial equipment problems. The second is a set of tests on flip chip bonding using gold stud bumps, gold tin solder-on-substrate, and plated gold pillars on alumina carriers. To evaluate the joining process using these different bumps, chips made of alumina with coplanar waveguide transmission lines were thermocompression bonded to the bumped carriers. Bonding parameters were assessed related to the different bump types and materials. The bonding results were analyzed using shear tests, transmissive x-ray and scanning electron microscopy on cross-sections. The third experiment lot contains early results on reliability of stud bump flip chip of gallium arsenide microstrip chips. Since the sample availability was very low and the joining process still under development, the results are indeterminate, although it was fruitful to establish adequate methods of analysis and test.

Introduction

One significant hurdle to microwave flip-chip experiments is the lack of bumping. Most users are not able to obtain undiced wafers, especially not for the expensive III-V materials such as GaAs. Test chips are typically handled as parts of a multiproject wafer run. Furthermore, the selected bump type will most likely dictate what joining method can be used, and thus the possible degree of process automation.

Bumping III-V Chips

Die bumping must be performed by the wafer producer directly, or as a singulated die. Few options remain, among these are bumping the carrier, discussed in another section. Wafer bumping is an additional process performed before dicing. If thinned wafers are subjected to bumping, the yield is less than for unthinned wafers. Most bumping houses do not handle wafers thinned to the dimensions typical for GaAs designs, i.e., typically 100 - 150 μm thickness.

The pads on GaAs and InP dice are often gold, while Al or Cu pads are typically used for Si dice. Since tin/lead solders do not wet to Al, a so-called under bump metallurgy (UBM) on top of the Al pads is required to provide wettability. Tin/lead solders do wet to gold, but the dissolution rate is very high. Furthermore, some of the intermetallics formed in

the system are not beneficial to reliability, a well-known fact. Therefore, it may be essential, or at least advantageous, to use an UBM for most solder alloys also for dice with gold pads.

Bumping GaAs is a challenge in manufacturing microwave flip chips, since both conductors and pads on the chip are gold. When implementing any chemical bumping process without a mask, the chemicals chosen to react with the gold on pads will also react with the gold on lines and air bridges, which is certainly not attractive.

For InP dice, an interesting approach to tin/lead bumping of small diameters has been realized [1]. The process has a few hundred Ångström layers of Ti/WN, NiV, and Au as an UBM, followed by 60/40 SnPb solder, all deposited by evaporation. Because the gold layer is thin, it is not harmful to the SnPb joint formed. The bumps are in general 30- μm diameter and 25 μm high. Since the InP and GaAs dice has the same Au pad metallurgy, it is likely that the same structure and process would also be compatible with GaAs.

Methods for flip-chip bumping of GaAs are similar to the ones used for silicon, apart from the pad metallurgy. At present, plating methods such as

electroplating and electroless plating are the dominating metal-deposition techniques. Transfer bumping and stud-bumping are also in use, as are solder paste printing on wafers, and conductive adhesive applied to the board or bumps.

Gold bumps are typically either electroplated or attached by stud bumping using a wire ball bonder. In both cases, thermocompression bonding is the most common method for subsequent joining. Other methods include soldering using, e.g., gold/tin solder, thermosonic bonding, or adhesive joining.

Plating gold is an ordinary process in GaAs-wafer manufacturing. Therefore, it is natural that the initial bump offerings from most wafer manufacturers are gold-plated bumps. Normally, a resist of about 20 – 25- μm thickness is applied to a wafer. Openings are generated in the resist, followed by gold plating, electrically or possibly electrolessly at locations where bumps are desired. It is vital to understand that, since pads, conductor pattern, and air bridges of GaAs die are gold, any unmasked electroless plating will react with all these surfaces.

The gold is not reflowed, due to its high melting point. Hence, the plated bump shape is the same through the joining steps, with some reduction in height and increase in width due to thermocompression bonding. The constant shape is an advantage also when bumps are used for cooling. In instances where H-shaped bumps are advantageous for cooling, a plated, non-melting bump is a good option.

The *gold/tin* alloy system is among the most reported in literature. Brittle phases may form in the system and must be avoided. However, the 280°C melting point of the 80Au20Sn eutectic alloy makes this solder beneficial since it remains unaffected by a soldering profile for eutectic tin/lead, which melts at 183°C. Therefore, gold/tin solder may be used for attaching dice on a module or inside a package to be soldered to a board in a normal surface mount process. The gold/tin system must have an under bump barrier layer to ensure that the gold conductor of the die is not consumed by the solder.

In 1989, Delco's original *silver*-bump process for silicon flip chips was transferred by Hughes [2] to an MMIC bumping process. The bumps were about 75 μm high and 150 μm in diameter. Thermal silver bumps of 75- μm height

are grown directly on the source-interconnect bridge of the power field effect transistors. The bumps are created in a dry-film photoresist process. The die is mounted on the carrier with solder paste or adhesive. Since silver reacts easily with elements in the atmosphere, silver bumps are not suitable for non-hermetic packages.

20 to 30 μm in diameter "microsolder bumps" were investigated [3], for a co-planar waveguide structure up to 60 GHz. Three bump alloy compositions were evaluated: pure *indium*, 70% InPb, and 50% InPb. The 50% InPb shear strength was determined to be three times that of pure indium. In a laser diode application [4] a Ti/Ni/Au under bump metallurgy was used before evaporating Pb/In to heights of 10 – 40 μm .

There are some indium alloys that are lead free. Environmental concerns with lead in solders may become an additional driver for their use but this not yet reported for GaAs flip-chip dice. A drawback to some applications, the melting points of indium solders are typically lower than for eutectic tin/lead.

No significant difference in electrical performance up to 2 GHz has been found when comparing the same chip design from wafers with bumps made by *printing conductive adhesives* to plated gold/tin eutectic bumps [5]. A major loss in microwave energy was caused by the underfill used, however, since the dielectric constant of underfills is higher than that of air and that was not taken into account in the chip design. The conductive adhesive did not cause loss over the chip surface, since it was localized only at the points of electrical interconnect.

Over the last few years, the most common version of bumping for research purposes involves *bumping on the carrier* instead of on the chip [6, 7, 8, 9]. For example, the carrier may be electrolytic gold bumped as part of a regular process for four-inch, thin-film substrates. An advantage with this method is that the chips do not need preprocessing and may be used off the shelf [10, 11]. NEC has also reported results on carrier bumping [12]. Here, gold-stud bumps are attached to an alumina chip carrier and the die is mounted to the carrier by thermocompression bonding.

The die-to-carrier joining method is naturally closely related to both bumping and carrier technology. Several schemes are being explored, for example thermocompression and thermosonic bonding, soldering, and adhesive joining

Experiments

As previously discussed, the chips under test are typically part of a multiproject wafer (MPW), and few suppliers bump MPWs, if any at all when it comes to GaAs. Also, when the test chips from an MPW are delivered, they are typically already diced into tiny chips. Hence, the following experiments focus on bumping on the carrier instead of on the chip wafer.]

A number of experiments on flip-chip joining using alumina substrates were carried out. In all the experiments a flip chip made from alumina was placed on an alumina carrier, with coplanar waveguide lines on both chip and carrier.

Three bump variants were assessed, Table 2. The gold stud bumps were made as a part of the following experiments, whereas the plated columns and gold tin solder pad plating were delivered by the respective carrier manufacturer.

Table 2. The experimental cases

Chip	Bump	Carrier
Al ₂ O ₃ CPW	Au stud, experimental	Al ₂ O ₃ CPW
Al ₂ O ₃ CPW	Plated columns	Al ₂ O ₃ CPW
Al ₂ O ₃ CPW	AuSn solder	Al ₂ O ₃ CPW

Experiments on Stud Bumping

Stud bumping was selected as a means of generating the bumps required to enable flip-chip bonding of the chips on the alumina substrates. The chips were not possible to hold down during wire breakage using only vacuum, because they were so tiny, 2 mm by 1.5 mm. The only alternative in this case, where only diced chips were available, was to place the bumps on the substrate pads.

The machine settings were chosen based on a combination of experience and guesswork from the operator's side. Settings from similar tests were used as a starting point and shear tests were made to assess the process parameters. The only parameter that is operator dependent is the precision in alignment. One and the same operator made all samples, so the operator factor must be considered eliminated.

A Delvotec thermosonic wire bonder F&K 5410 and a 25 μ m Au1Pd wire were used for the bumping. Pd is added to the wire to facilitate reproducible breaking of the wire above the bump, as described earlier. The stage temperature, bonding force, ultrasonic power and ultrasonic time were modified in the bumping parameter variation. The bumping results were assessed by means of bump shear strength measurements. The ball bump geometry was measured with the ocular scale of a light microscope and studied by scanning electron microscopy (SEM) inspection. The total height,

including the tail was 80 μ m and 40 μ m excluding the tail. The bump diameter was 80 μ m.

For reliable mechanical bumping a good welding between bump and bond pad must be achieved. However, it is important to understand that the bonding of the flip chip to the carrier also leads to a better welding and an increase of bump shear forces, since the ball bumps then experience a second bonding sequence.

The ball deformation should be as small as possible to allow for a large deformation in the subsequent flip-chip bonding. In order to obtain minimal deformation of the bump, the lowest ultrasonic power, bonding force and shortest application time possible for reliable bonding are beneficial. The sensitivity to substrate cracking is also reduced with lower values of these parameters, Table 3.

Table 3. Parameters selected for stud bumping the substrate.

Bond weight 38 g	Power 0.55 W
Time 25 ms	Temperature 220°C

The shear force of the bumps was measured to 45 cN $\pm$ 7 cN. The bump does not cover the whole pad when the ball is placed, but the bump swells when the chip is bonded. It is believed that there is no strict limit for height tolerance, since the soft gold tail of the bumps can accommodate for reasonable variations in height.

Experiments on Gold-Pad Chip Joining

For the experiments on flip-chip joining, three types of bumps were tested. These variants have been listed in Table 6 earlier. The gold stud bump process that was used for some of the carriers in this set of experiments is described in detail in the previous chapter.

A set of carriers were purchased with plated gold columns or pillars on the pads for flip-chip joining. These columns were simply the pillars for air bridges that are available in regular production as a special feature.

The columns were measured to 75 μ m in diameter and there were samples of two different heights, approximately 35 and 60 μ m respectively. Note in Figure 25 the coplanarity in height of the bumps. Some carriers purchased were delivered with AuSn preplated on the pad surfaces. This plating cannot be referred to as a bump since the volume of AuSn is so small that it just becomes a flat layer on top of the pad, see Figure 2. It is comparable to the traditional hot air solder leveling on printed circuit boards in that it provides a solderable surface on which to solder a bump in this case. Notice the layered structure of the plating on the pad, indicating that the solder has not been reflowed.

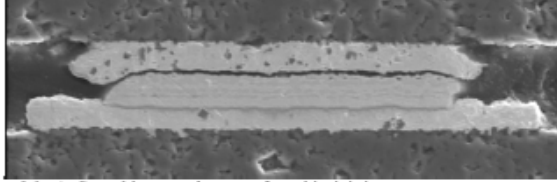


Figure 2. AuSn solder on substrate after chip joining.

Thermocompression Bonding Experiments

Previous experience at the bonding subcontractor's has shown that bonding sensitive chips using ultrasonics, i.e., thermosonic flip-chip bonding, is less suitable for thin chips, such as GaAs or InP chips, and that these chips survive thermocompression better. The coplanarity of the chip bumps is not an issue, since the gold bumps are soft and will deform to equal height when the chip is placed. The bumps are not coined, since the bonds get stronger if the bump tail remains. Therefore, thermocompression flip-chip bonding experiments were made using stud bumped alumina substrates and GaAs chips. The bonding was made using a flip-chip bonder.

The bonding process starts with lifting the chip using the vacuum pick up tool on the bonding arm. The substrate is then placed on the heating plate of the bonder. The chip and substrate are aligned using overlapping images in the stereomicroscope of the bonder. Then the preprogrammed heating cycle for both substrate plate and chip pick up tool is initiated. The chip is pressed against the substrate with a controlled force after the temperature has stabilized in both the heating plate and in the heated pick up tool. The tool is completely flat to the chip backside. The tool is held in place for approximately 15 s and then the vacuum in the pick up tool is released and the bonder arm lifted. After this, there is a slow cool-down of the test sample to approximately 150 °C, still on the heating plate. The parameters found to be suitable for the thermocompression flip-chip bonding are given in Table 4.

Table 4. Parameters used for thermocompression flip-chip bonding.

Substrate temperature 310°C	Time 15 s
Chip temperature 210°C	Force 25 cN/bump

After thermocompression bonding the bumps have a fairly symmetrical look, Figure 3. There is a clear neck at the chip side of the bump, where the bump tail was. It is obvious that this is the weakest part of the joint.

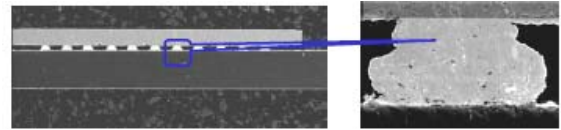


Figure 3. Chip bonded to substrate with stud bumps.

The chip shear force was tested using three samples, 15 – 20 grams per bump. The 5 grams limit stated in MIL STD 883 would not be accepted by the subcontractor, it is far too low. The shear tool was applied at the bottom of the bump for bump shear and at the height of the bottom surface of the chip for chip shear. This is not according to standard practice, where it is clearly stated that the tool shall be applied to the middle of the bump.

Figure 4 shows a view of the chip surface after the shearing. Parts of the bumps were left on the chip. The shearing force for the chip with 36 bumps was 630 g which corresponds to 18 cN/bump. Furthermore, in these first tests, the chips were found to be inclining on the substrate.

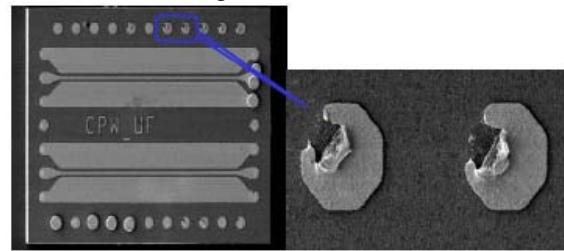


Figure 4. View of chip surface after the chip has been sheared off the substrate.

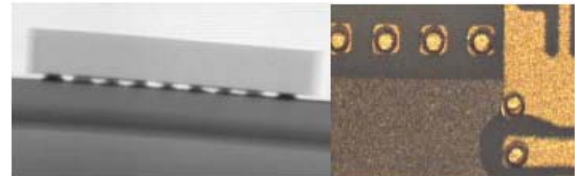


Figure 5. Chips are inclining after assembly. Side view in X-ray, left, and optical microscopy image of carrier, right.

Figure 5 left shows a side x-ray view of an assembly, where the trained eye can see a difference in height at the chip edges. The right image illustrates the carrier surface after chip shear, where it is clear that the bonded area is not equal at the different bump locations. This means that the chips are not pushed down evenly. Chip to carrier gaps over a chip short edge were measured to 30 – 34 μm , meaning that there is a 10% change in the height over less than 1.5 μm distance.

When the chip is aligned to the substrate using the split vision optics, the pickup head is at its top position. During the next step in the bonding sequence, the arm moves in a circular fashion, rotating the head down toward the bonding site. Other types of bonding machines make the final

approach to the chip site in a linear, z axis motion thus allowing the chip to hit the surface in a horizontal fashion. Therefore bonding using that type of machine construction becomes more precise.

AuSn Soldering

For the AuSn plated substrates the parameters used are given in Table 5. Unbumped chips were joined to these substrates. The AuSn plating was just a few microns in height, so the electrical and mechanical results of this experiment set is not expected to be excellent.

The chips were soldered in air, not using any inert atmosphere such as N₂ or formic acid. The settings were selected based on hints from literature. The solder melted after a few tries. The chips were held with a small force until the temperature dropped before they were released.

Table 5. Parameters used for flip-chip bonding on the AuSn plated substrates.

Substrate temperature 310°C	Time 20 s
Chip temperature 240°C	Force 20 cN/bump

In an automation case, this method could be used with prebonding to hold the chip in place, followed by sending the assembly through reflow. In general, a solder with lower melting point is needed, because the chip must be kept at temperatures below 250 °C. This is also why heating had to be applied from the bottom, through the substrate.

It is not desirable to hold the chip in place with force during a soldering operation. If there is no force holding the chip, the surface tension of the molten solder can act freely and will then align the chip perfectly, in x and y directions. Also, the solder will take its natural height, based on the solder volume, chip weight and number of bumps.

Bonding on Plated Columns

Thermocompression bonding on plated columns was straightforward. Parameters used were the same as for bonding on stud bumped substrates. The cylindrical bumps were 56 µm high after bonding including the pads, and 51 µm high without the pads. The bump diameter at the bottom surface, towards the carrier, was between 82 and 84 µm and the center diameter was 78 – 80 µm. A cross-section of a resulting joint is shown in Figure 6.

Discussion

The optimal flip-chip process to be used in a production situation is one that is suitable for a high level of automation. The automated process requires a smooth flow in the production and any subprocess that requires more time to complete than the process before or after can be stalling the flow.

Looking at the thermocompression bonding described above, there are some obvious bottlenecks. The chip bonding consists of preheat, force application during 15 seconds, followed by cool-down. This is a limiting factor in an extension to volume production. Implementing preheating and cool-down stages, where one substrate can be heated or cooled down while another one is bonded, will reduce the throughput time

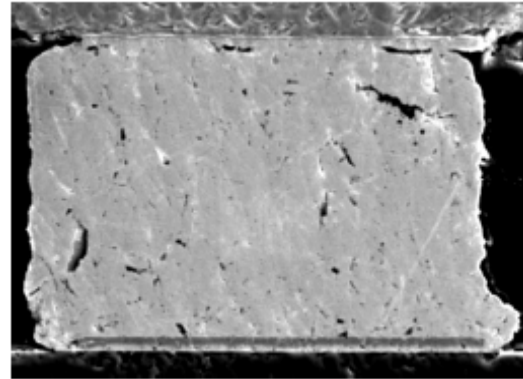


Figure 6. A plated column bump after thermocompression joining is shown. A dark line of Ni can be seen near the bottom of the bump.

Regarding the tool size, for thermocompression joining the tool can take any chip size up to the tool size. This is a benefit compared to thermosonic bonding, where edges on the tool are necessary. These tools are often called collets and the edges are basically holding the chip in place during the sideways motion of the ultrasound during bonding. This implies that there must be one tool per chip size to be bonded, meaning that if there is more than one chip size on the same substrate, it might be necessary to change tools during the assembly.

In the alignment of chip to substrate, the pad pattern was used. Chevron marks can be used for post-bonding check. With a set of two or more chevrons at each chip corner it is very easy to optically inspect the alignment by verifying that the same number of chevrons is visible at each corner. For example, in the case of two chevrons at each corner, with precisely one chevron showing at each chip corner and one hidden by the chip, the chip is well aligned. In future substrate designs, one chevron may be removed, since for checking the bonding it will be enough to have one not visible when the chip is correctly placed. This reasoning is valid only if the chip dicing is well made, which may not be the case for lab work and prototypes.

Rework and repair of chips bonded to substrates using thermocompression is not possible. Therefore the first pass yield sets the limit to the

fruitfulness of this process, especially when mounting many chips on one substrate.

The pitch in this case, 150 μm , is the minimum pitch possible today with regard to the stud bumping process. If the pads are made smaller the wire diameter would have to be changed to 17 μm . A regular wire bond capillary was used, and this could possibly be changed to a fine pitch capillary if needed.

Conclusions

Many large companies involved in telecom and radar communication are carrying out research and development in the field of advanced die-interconnection technology. The benefits provided by flip-chip over wire bonded chips are well documented for lower frequencies, and now there is a significant body of information published in favor of flip-chip interconnected dice for RF, microwave, and millimeter-wave applications.

The overall conclusions on using area-array interconnect for high-frequency applications are:

- Dice should be of coplanar design, to attain the best field distribution, and to avoid interaction with the carrier.
- Wafer back grinding, via-hole generation and back plating of dice can be avoided completely by using coplanar dice. This gives a significant cost reduction due to increased yield in wafer fabrication and assembly.
- The general electrical performance of flip-chip assembled microwave dice is much better than for equivalent wire-bonded dice.

There are also disagreements in some basic fundamentals, for example the most favorable stand-off height (the chip-to-carrier gap). Some studies claim that 20 μm is the most beneficial, and others prefer as high as 100 μm , which is a more favorable dimension from a production perspective.

To commence activities in gallium arsenide flip-chip technology it is necessary to have a relationship with a chip manufacturer, and to identify a well-suited bumping procedure.

In parallel, die designers must focus on designing for flip-chip rather than wire-bonding, which includes converting from microstrip to coplanar designs. The assembly and bonding process chosen will greatly depend on the bump material selected, and carrier performance required. Much effort remains before flip-chip gallium arsenide is commonly available, but one fact prevails: Since the consumer demand for products with ever increasing frequencies, low cost, high reliability is a trend expected to continue, the need to incorporate flip-chip technology is obvious.

A total of approximately 200 substrates have been bumped, with over 6000 bumps in total, and chips attached on them by thermocompression flip-chip bonding. The wire stud bumping process produced bumps with a shear force of 45 cN, and the shear force per bump after the flip-chip bonding was between 15 and 20 cN.

A number of substrate samples had plated gold pillars or thin AuSn pad plating fabricated by the substrate manufacturers. These substrates also had flip chips attached by thermocompression bonding. The pillars were easy to work with and this is definitely the preferred bump type based on these experiments. No shear tests on chips bonded to the pillar substrates were made, only a tweezers push.

The solder plating was not so straightforward. It was difficult to achieve a bond. Possibly, this is caused by coplanarity issues that are not handled well when the solder height over the pad is only a few microns. It might be easier to generate a good solder joint if the chip to be soldered had a wettable bump that can receive the soldering.

In summary, stud bumping substrates with Au1Pd wire is entirely possible, especially for prototyping and lab work. It takes some process development to achieve good bumps, but once the process has been set up properly, the bumps become very uniform. Thermocompression bonding of chips to these carriers, however, has some severe limitations. The time consumption for bonding one chip is high, and there is no reworkability. The small difference in coplanarity of the stud bumps does not seem to affect the bonding result, but the motion of the bond head may cause height differences even over a small chip. Carriers with plated gold cylinders for bumps tested well and are easy to work with. There is a premium in the cost of the carrier, but on the other hand, the electroplating of the gold pillars must be considered more reliable and repeatable than the stud bumps.

Soldering remains the best solution both from repeatability and throughput perspectives. However, regular flip-chip bumping on gold pads is hard to find today, and thus it may be necessary to use other methods for the next years to come.

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