

A Low Power 5.5 GHz Current Reuse LNA for Unlicensed National Information Infrastructure

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Abstract - This paper presents a fully integrated CMOS LNA with on-chip spiral inductors in 0.18 μ m CMOS technology for 5.5-GHz unlicensed national information infrastructure (U-NII), 802.11a and IEEE 802.11n wireless LAN Receiver. By using a cascode current reuse structure with inter-stage inductors we achieved low power consumption and high power gain. We proved that the inter-stage inductors must be designed with a new method compared to newly published papers. This structure is based on two cascode configuration which provides a good output swing thus allowing the integration in low voltage technology. This configuration also permits good input impedance matching, low noise figure and high reverse isolation. Complete simulations of the circuit at 5.5-GHz center frequency, have shown that the circuit has 3.1dB NF, 1.2GHz 3dB power bandwidth, 20.63dB power gain (S_{21}), high reverse isolation (S_{12}) < -45dB, -29.4dB input matching (S_{11}), -25dB output matching (S_{22}), and -15.9dBm 3rd order input intercept point (IIP3). The power consumption is 3mW at 1.8V supply voltage.

Index Terms— LNA, Wireless local area network, Low noise amplifier, Inductive degeneration CMOS LNA, Receiver Front-End, current-reused LNA

I. INTRODUCTION

THE demand for wireless local area network (WLAN) systems which can support data rates in excess of 20 Mb/s with very low cost and low power consumption is rapidly increasing. Some WLAN standards, such as IEEE 802.11a (5 - 5.825GHz), IEEE 802.11n (2.4 - 2.485GHz, 5-5.825GHz) and the newly released unlicensed national information infrastructure (U-NII) in the United States require a transceiver with approximately 5.5-GHz center frequency, with 1-GHz bandwidth [1].

Since Low Noise Amplifier (LNA) is the first power gain stage in wireless receivers it plays a crucial role for the link budget and for the receiver's total performance [2]. LNA amplifies the weak signal received from the antenna and the duplex filter, which is normally driven by an unknown length transmission line [3]. Therefore, to reduce the reflections from LNA back to the antenna, the circuit requires a stable input impedance matching approximately equal to 50 Ω . Several matching methods have been presented in [2], [3].

The minimum acceptable signal level at the receiver according to the U-NII regulations is 70-dBm while the maximum strength of the received signal is 20-dBm. The large dynamic range, the high operating frequency and the wide channel bandwidths impose very stringing requirements for

the front-end circuit of receivers [1]. In order to have a large dynamic range, high linearity must be achieved. This parameter is typically is measured in terms of third-order input intermodulation point (IIP3) [3], [4].

To alleviate the effect of gate-drain capacitance, that reduces the forward gain, the isolation and the operating frequency, cascode configurations are widely used in CMOS RF LNAs. Particularly, unilateralization and neutralization are two circuit-level techniques often used to enhance the reverse isolation and operating frequency in CMOS RF LNAs [5]. The inductive source-degenerated LNA, on a cascode structure, is another popular architecture in RF integrated and microwave circuit designs [6], [7], but some applications need high power gain to amplify the weak signals with the lowest power consumption and noise figure.

This paper presents a CMOS LNA with reduced power consumption and improved power gain. It keeps acceptable noise performance, good input/output matching, and sufficient linearity at the same time. This is obtained by using a cascode current reuse structure with careful design of the inter-stage inductors. This paper is organized as follows: Section II explains in detail the design steps for the LNA in a 0.18 μ m TSMC RF technology. The design details of the inter-stage inductors are discussed in this section. Finally, in Section III accurate simulations and comparisons with other works available in literature are presented.

II. DESIGN

We can summarize all the important parameters that are usually considered to design and to define the performance of an LNA in the following categories: Input impedance matching, stable power gain with acceptable linearity, noise figure, and power consumption. Since achieving optimized values for all the above mentioned parameters for a single LNA is impossible, the designer must trade off among the most important parameters by selecting the most significant constraints.

The LNA designed in this paper uses a cascode current reuse structure with inter-stage inductors as shown in Fig. 1. In this circuit M_1 , M_2 are the cascode transistors, M_3 is used to create the bias quantity for the LNA, L_{g1} , L_s are used to input matching, L_{d1} , L_{g2} and C_2 are the inter-stage filter components. In order to optimize the design of the elements of the circuit we present the employed five design steps.

1st step: Calculating the optimum width of M_1 in order to obtain the best noise performance. This task can be carried out according to [8],

$$W_1 = W_{opt} F_{\min} \cong \frac{3}{2\omega L C_{ox} R_s Q_{Lop}} \quad (1)$$

where C_{ox} , Q_{Lop} , R_s , ω , and L are the oxide capacitance, the optimum quality factor of input circuit, the source resistance, the operating frequency and the length of the transistor, respectively. The quantity $Q_{Lop} \geq 2.598$ [8] is defined as

$$Q_{Lop} = |c| \sqrt{\frac{5\gamma}{\delta}} \left[1 + \sqrt{1 + \frac{3}{|c|^2} \left(1 + \frac{\delta}{5\gamma} \right)} \right] \quad (2)$$

Where γ and δ are the transistor channel coefficients. In this equation, it is stated that there is a correlation between the channel resistance noise and the non-quasi static effect noise typically denoted by c , correlation coefficient [9], [10].

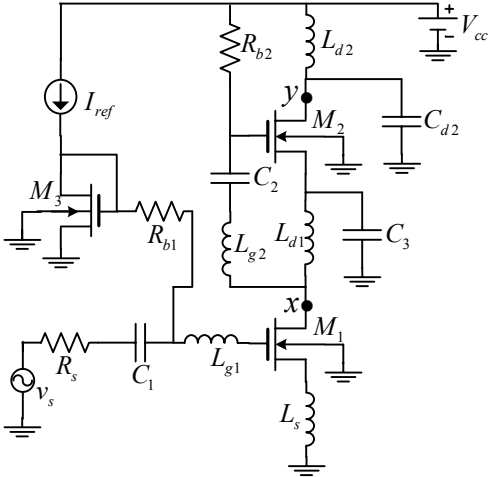


Fig. 1 The designed LNA structure.

The optimal length of M_2 requires a trade-off to suppress the noise contribution and enhance the gain. Normally, it is chosen as a half or similar to M_1 [3], [11]. In this paper the width of M_2 , is chosen with the same width of M_1 . The gate-source capacitance of transistor M_1 denoted C_{gs} , can be expressed by [3],

$$C_{gs} \cong \frac{2}{3} W_1 L C_{ox} \quad (3)$$

Transistor M_3 is used to bias the LNA by mirroring the reference current to the transistor M_1 . There are two restrictions for size of M_3 , technology and current mirroring. For example in a 0.18 μ m RF CMOS technology the minimum size of transistor is five fingers and each finger has 5 μ m. In order to reduce the noise figure and power consumption, it is necessary to set its width to a small fraction of W_1 . In this design, we assumed $W_1 = 3W_3$.

2nd step: Determining the bias or reference current in order to limit the total power consumption. As shown in Fig. 1, the current source magnitude is equal to the drain current of M_3 . Considering that the widths of M_1 and M_3 have a ratio of 3, we

can express the total supplied current with the following equation,

$$I_{Vcc} = P_{dis} / V_{cc} = I_{DM1} + I_{DM3} \cong 4I_{ref} \quad (4)$$

Where I_{Vcc} is the total supply current.

3rd step: Calculation of L_g and L_s . For this computation the following equations stating impedance matching can be used [12], [13]:

$$\omega_o = \sqrt{\frac{1}{(L_s + L_g)C_{gs}}} \quad (5)$$

$$R_{Lg} + R_g + R_{nqs} + \frac{g_m L_s}{C_{gs}} = R_s \quad (6)$$

It is necessary to consider an initial value for $R_{Lg} + R_g + R_{nqs}$ and simulate the circuit. We repeat the third step until the simulation results confirm that the input matching is achieved within a given tolerance. For example the iteration is considered successful if S_{11} coefficient is below -15dB. The resistors R_{b1} and R_{b2} , used to mitigate the effect of gate-source capacitance of transistor M_3 and to bias transistor M_2 , must be higher than the input impedances. Their values are arbitrary chosen between 2 and 4 k Ω in a 0.18 μ m technology [11]. They must be much larger than 50 Ω and their upper bound depend on their thermal noise. To achieve a low noise figure, their thermal noise contribution must be much lower than input referred noise of the transistors.

4th step: Design the inter-stage circuit. Fig. 2 shows the small signal equivalent circuit of the inter-stage sub-circuit of Fig. 1 between points x and y [14],

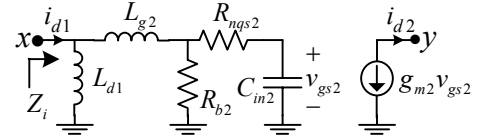


Fig. 2 Small signal equivalent of current reuse part of designed LNA

In the figure, C_{in2} and R_{nqs2} are the gate-source capacitance and the non-quasi static effect of transistor M_2 , respectively. By choosing the value of R_{b2} larger than the input impedance at the gate of M_2 , the input impedance from x can be written as,

$$Z_i = sL_{d1} \parallel (sL_{g2} + R_{nqs2} + \frac{1}{sC_{in2}}) \quad (7)$$

Then

$$v_{gs2} = \frac{sL_{d1}}{s^2(L_{g2} + L_{d1})C_{in2} + sR_{nqs2}C_{in2} + 1} i_{d1} \quad (8)$$

To achieve the maximum gain through the inter-stage network, the derivative of (8) with respect to s , must be equal to zero. Thus,

$$L_{d1}[s^2(L_{g2} + L_{d1})C_{in2} + sR_{nqs2}C_{in2} + 1] - sL_{d1}[2s(L_{g2} + L_{d1})C_{in2} + R_{nqs2}C_{in2}] = 0 \quad (9)$$

By solving equation (9) we obtain,

$$s = 1/\sqrt{(L_{g2} + L_{d1})C_{in2}} \quad (10)$$

Therefore by choosing the width of M_2 we observe that the total value of inter-stage inductors are constant and may resonate with the total capacitance (C_{in2}) of M_2 . In [14] the value of L_{g2} is adjusted for resonating with the input capacitance of M_2 .

On the other hand, for larger values of R_{b2} compared to the input impedance at the gate of M_2 , the current gain transfer function can be expressed as follows:

$$\frac{i_{d2}}{i_{d1}} \cong \frac{g_{m2}}{sC_{in2}} \frac{sL_{d1}}{sL_{d1} + sL_{g2} + R_{nq2} + 1/(sC_{in2})} \quad (11)$$

This transfer function has one zero and two poles that are, respectively

$$\omega_z = 0 \quad (12)$$

$$\omega_{p1,p2} = \frac{-C_{in2}R_{nq2} \pm \sqrt{C_{in2}^2 R_{nq2}^2 - 4(L_{d1} + L_{g2})}}{2(L_{d1} + L_{g2})} \quad (13)$$

Equation 13 shows the poles of transfer functions are on the left side of imaginary axes, thus the inter-stage circuit will be stable. In the other case if the impedance of L_{d1} is chosen sufficiently higher than those of L_{g2} , it is possible to approximate (11) as follows:

$$\frac{i_{d2}}{i_{d1}} \cong \frac{g_{m2}}{sC_{in2}} \cong \frac{g_{m2}}{sC_{gs2}} \cong \frac{\omega_T}{\omega} \quad (14)$$

From equation (14) we can note that it is possible to provide a significant amount of current gain from the drain of M_1 to the drain of M_2 , thus leading to an high overall power gain. In this design, we considered the minimum amount of L_{g2} compatible to the on-chip spiral inductor technology and then we determined L_{d1} in such a way that equation (10) is verified. After these considerations another important contribution needs to be considered: the Miller effect. In fact, the input impedance matching at the gate of transistor M_1 , needs to be modified again to overcome the limitations due to this effect. To solve this problem it is necessary to come back to the 3rd step and repeat the calculations.

5th step: Calculation of L_{d2} . As shown in Fig. 1, the use of an output inductor connected to the drain of M_2 is mandatory. This is due mainly for two reasons: First, because it resonates with the total drain capacitance and makes the circuit meet the desired frequency bands. Second, because it increases impedance enough to obtain a high gain. The maximum of L_{d2} required for the maximum power gain, is bounded by the total drain capacitance. On the other hand, the minimum of C_{d2} is restricted by the load (e.g. Mixer) and by the LNA output capacitances. Having considered this, L_{d2} and C_{d2} are chosen by trading off between gain and bandwidth.

These simple design steps can be repeated iteratively according to the required circuit performance.

III. SIMULATION RESULTS

By using our proposed algorithm, the fully integrated LNA has been designed in a 0.18 μ m CMOS technology with the

help of Cadence Spectre RF. In the simulations the transistors and the RF inductors are inclusive of parasitic components. Complete simulations of the designed LNA, are shown in Figures 3, 4, 5 and in table 1. Fig. 3 and Fig. 4 show the noise figure and power gain of designed LNA, respectively. We achieve high power gain and good noise figure, thus proving the reliability of our circuit for highly sensitive transceivers. Fig. 5 shows that this circuit has good matching properties, -29.4dB input matching (S11), -25dB output matching (S22). The circuit has a center frequency of 5.5-GHz, 3.1dB NF, 1.2GHz 3dB power bandwidth, 20.63dB power gain (S21), and -15.9dBm 3th order input intercept point (IIP3). The power consumption is 3mW at 1.8V supply voltage. Also simulation results showed good stability in all of band width.

In order to identify more clearly the differences with other solutions, table 1 shows a comparative analysis with respect to other works available in literature.

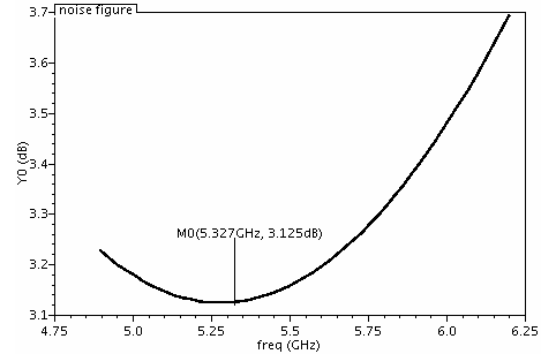


Fig. 3 LNA Noise Figure (NF)

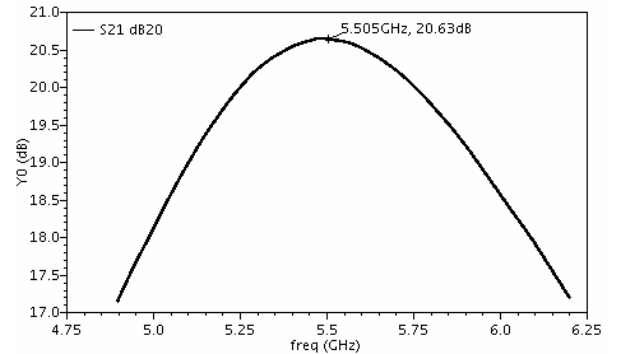


Fig. 4 LNA power gain (S_{21})

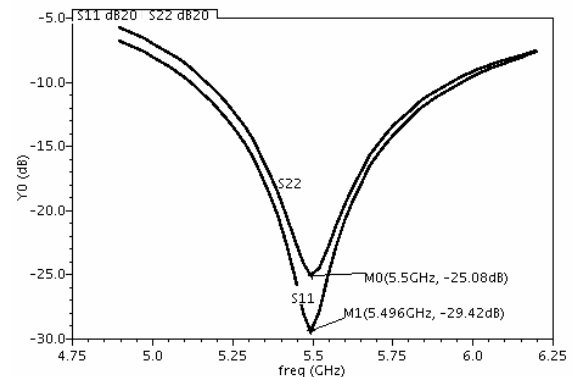


Fig. 5 LNA S_{11} and S_{22}

TABLE 1
COMPARISON BETWEEN THIS WORK AND OTHER PUBLISHED LNAs

LNA	Ref.[7]	Ref.[14]	This work
f_0 (GHz)	5.7	5.2	5.5
Bandwidth (GHz)	-	0.15	1.2
NF (dB)	3.65	2.45	3.12
Current [mA]	8	8	1.6
Supply [V]	1.8	3.3	1.8
$IIP3$ (dBm)	-3.3	-	-15.9
S_{11} (dB)	-15.2	-	-29.5
S_{21} (dB)	14.5	19.3	20.63
S_{12} (dB)	-	-	<-45
S_{22} (dB)	-14	-	-25
Technology	0.18 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS

Conclusions

In this paper we designed and simulated a fully integrated CMOS Low Noise Amplifier with on-chip spiral inductors in 0.18 μ m CMOS Technology by employing Cadence Spectre RF. The circuit shows high power gain and high reverse isolation. It provides high reverse isolation, and increases the 3dB power bandwidth with respect to other works. Power consumption and noise figure are quite low compared to other published works. The LNA has good power gain, low power and low noise figure. These are achieved by employing a current reuse structure and iteratively designing the inter-stage network.

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