

Full Tape Thickness Features for New Capabilities in LTCC

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Abstract

Full tape thickness features (FTTF) using conductors, high K and low K dielectrics, sacrificial volume materials, and magnetic materials are useful as both technically and cost-effective approaches to multiple needs in laminate microelectronic and microsystem structures. Lowering resistance in conductor traces of all kinds, raising Q-factors in coils, and enhancing EMI shielding in RF designs are a few of the modern needs. By filling with suitable dielectric compositions one can deliver embedded capacitors with an appropriate balance between mechanical compatibility and safety factor for fabrication. Similar techniques could be applied to magnetic materials without wasteful manufacturing processes when the magnetic material is a small fraction of the overall circuit area. Finally, to open the technology of unfilled volumes for radio frequency performance as well as microfluidics and mixed cofired material applications, the full tape thickness implementation of sacrificial volume materials is also considered. We discuss implementations of FTTF structures and discuss technical problems and the promise such structures hold for the future.

Key Words: LTCC, RF, full tape thickness,

1. Introduction

Applications for low temperature cofired ceramic have been expanding as flat board technology has been augmented with three-dimensional features including cavities, channels, rolled tubes, formed shapes, sacrificial volume materials (SVM), and various embedded components. The embedded components include resistors, capacitors, inductors and heatsinks. In this paper we discuss recently introduced techniques for fabricating full tape thickness features (FTTF).[1] These are based on via fill technology and use the full thickness of the tape to improve performance. In the case of conductors this is accomplished by substituting full thickness lines for surface-printed traces that are typically thin. An example of such a line is shown in Figure 1. The result is traces with very low resistance and special structures, such as coils, where the resistance decrease and the cross section of the traces is responsible for very high Qs. Electromagnetic isolation can also be improved with these structures. When high thermal conductivity materials are used, the capability to remove heat is greatly enhanced. In the case of capacitors the larger

size of the gap is traded for an ability to reliably make capacitors. When the fill material is an SVM, full thickness cavities as well as vented and blind unfilled volumes are possible. The interest in embedding structures in LTCC has been strong from its inception. Resistors are most commonly embedded albeit typically with high tolerances ($\pm 30\%$).

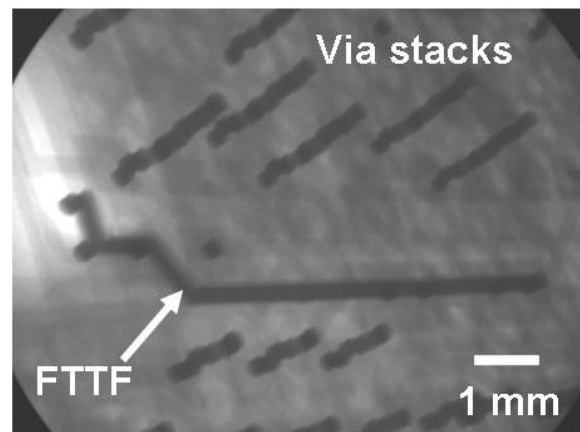


Figure 1. X-Ray view of FTTF conductor trace.

2. Background

Low temperature cofired ceramic (LTCC) can meet many integration needs while bringing well-known advantages including high conductivity electrical traces, low dissipation factor dielectrics, inherent manufacturability, high temperature operation, chemical inertness, and versatility in integrating multiple interrelated devices in a variety of critical proximities, orientations, and environments. This integration can be accomplished with superior performance at a reasonable cost. Literature documents the appeal to ceramic sensor and system applications (macro-, meso-, and micro). [2,3] In this paper we will discuss processing techniques we have used to generate new structures. By tailoring processes to meet specific program needs, LTCC can interface to microsystem components at their tiny scale and present them in usable form to the outside world.

LTCC is a well-known commercial technology based upon flexible tapes composed of glass and ceramic particles held together by an organic binder that can accommodate thick film and other traces as well as punching, machining or deformation operations. Most of our work is done with various DuPont tapes (951C2, PX, AT, and 943). The tapes are collated, laminated, and then fired with a prescribed temperature profile to accomplish sintering to a monolithic piece. More specific details are addressed in a comprehensive review. [2]

LTCC technology continues to advance from its roots in thick film hybrid microcircuit technology. One of the most significant reasons for which it was established was to address the need for a single thickness of dielectric (resulting from a tape layer) to be sufficient to eliminate pinholes between layers that required multiple printed dielectric layers with thick film. Additionally, the serial nature of thick film hybrid microcircuits meant that technical difficulties on upper layers negated the value added to the lower layers, which were usually built up in laborious print-dry-fire cycles. Multiple prints of a dielectric paste worsened cumulative planarization problems for upper layers. Finally, attempts to cofire thick film dielectric and conductor layers produced undesirable interactions that do not occur using LTCC. Starting with embedded resistors and proceeding to other integral structures, the capability of LTCC is rapidly advancing.

FTTF using conductors are based on via fill techniques and have been fabricated by stenciling the

full thickness lines at the same time as via fill. The level to which the via is filled will play an important role in its tendency to protrude above the surface or 'post-up'. They are also an additional feature with a material discontinuity and so can be fragile in the handling that follows drying of the vias and thick film. It is sensible to limit the length of the channels. A second technique is screeding, where the punchable backing on a tape layer is used in lieu of the stencil. An experiment has been performed in the past wherein silver thick film lines 0.75 mm wide were screeded in 75mm lengths in a single layer of 254 micron (0.010" tape) and cofired as single sheets.

The thick film was strongly adhered to the fired tape such that when a moment was applied at the thick film-to-LTCC interface, the fractures were in the LTCC. These parts are shown in Figure 2. Additional work is required for this to be usable in production environments.

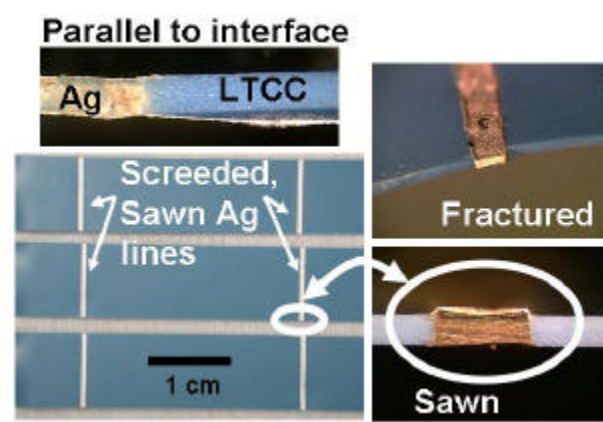


Figure 2. Conductive Silver Screeding

3. Applications

3.1. Low resistance traces

Certain critical applications benefit from reduced parasitic resistance such as RF lines buried in a multilayer MCM. The conductivity and edge definition of screen printed thick film lines are adequate for many surface features including microstrip and stripline features, but low-resistance FTTF lines have been used with advantages such as the case shown in Figure 1. Another approach has been shown by filling embossed features with conductor inks. 4

The ability to make these features leads to an interest in embedded features such as inductors. Inductors have been fabricated in planar implementations as well as 3 dimensional features

using planar traces connected by interlevel vias.[5] Figure 3 illustrates coils that have been designed to use the FTTF approach to minimize parasitic resistance.

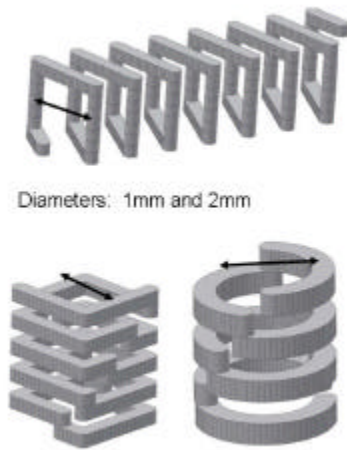


Figure 3. FTTF coils; horizontal rectangular, vertical rectangular, and vertical round designs.

By utilizing silver thick film materials in place of gold, the resistances are reduced even further. Such coils have been fabricated and the frequency response is illustrated for square coils in Figure 4. One can see that very high Qs are possible. The frequency response for the vertical axis round inductor is shown in Figure 5. While initially it seemed reasonable to exercise caution for Qs greater than 100, additional experience has shown that these very high Q values are real.

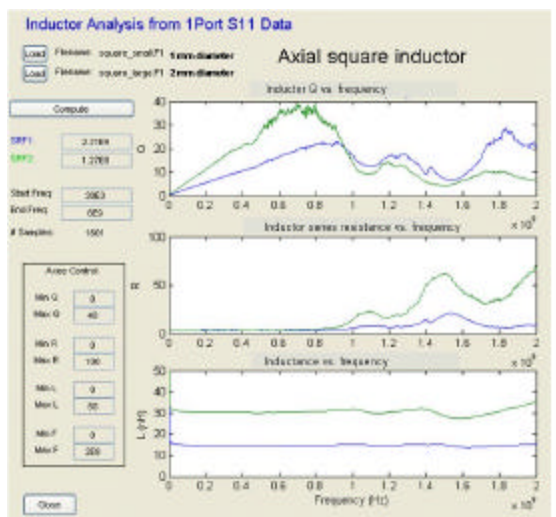


Figure 4. Frequency response for axial square inductor (measurements made by Prof. Bill Kuhn, Kansas State University)

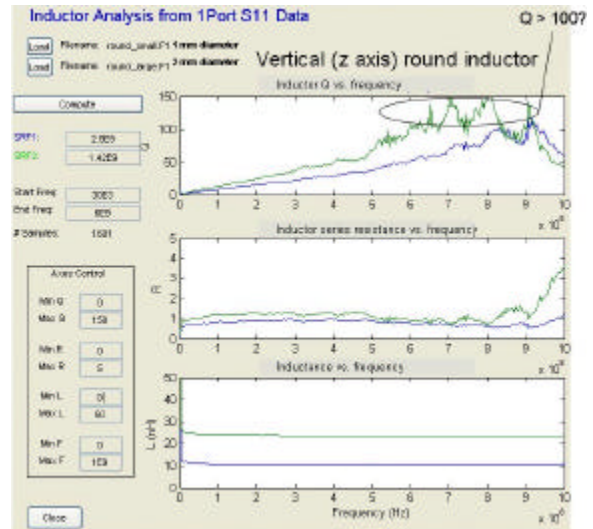


Figure 5 Frequency response for axial round inductor (measurements made by Prof. Bill Kuhn, Kansas State University)

3.2. Electrical isolation structures

Additional electromagnetic isolation structures have been used. Via fences have been used by others and by us as well. [6] Initial measurements have indicated that the extremely high isolation required for some applications (150db) has not been attained with via fences. Overlapping FTTF conductors have been designed to provide more complete shielding. Modeling has been performed using two adjacent cavities with antennas in the floors as shown in Figure 6. The structure of the walls is shown in Figure 7. The assumptions include a metal lid and solid ground planes on either side of the cavities. The modeling was performed for staggered rows of via fences as well as FTTF structures. As shown in Figure 8 the isolation is expected to be better using the FTTF.

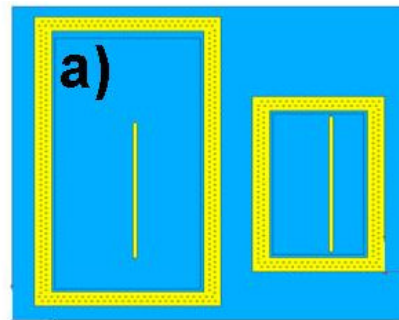


Figure 6. FTTF isolation structures. a) Simulated radiating and receiving antennas.

Figure 9 shows a view of actual FTTF EMI structures beneath a thick film seal ring and Figure 10 shows a saw cut through such a feature. A higher magnification image is shown in Figure 11.

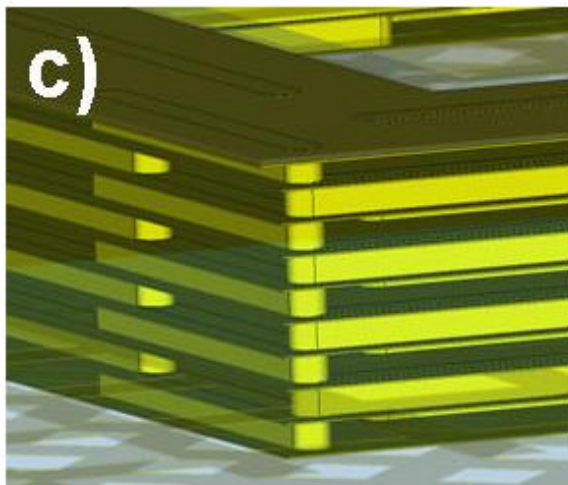
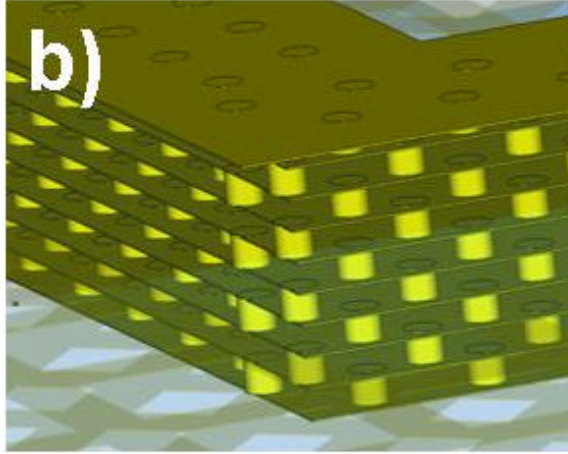


Figure 7. FTTF isolation structures.
b) conventional 2 row via fence c) New two row FTTF wall isolation.

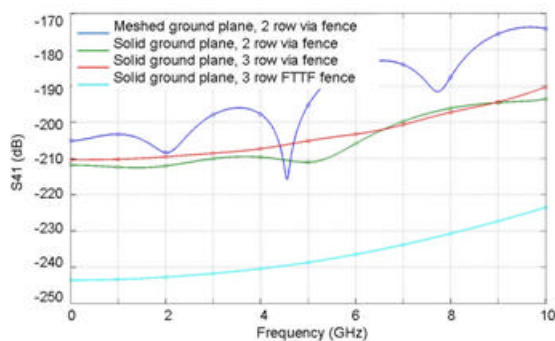


Figure 8. Frequency response of EMI isolation.

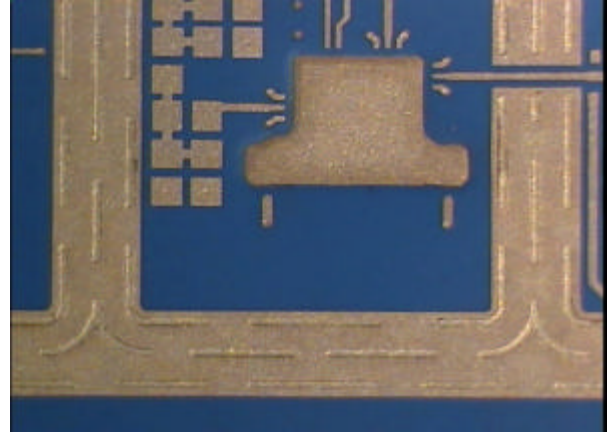


Figure 9. FTTF conductor line segments used for EMI.

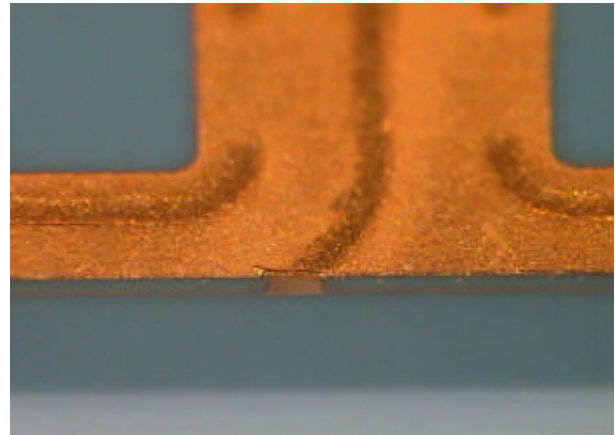


Figure 10. Sawn section of FTTF conductors.

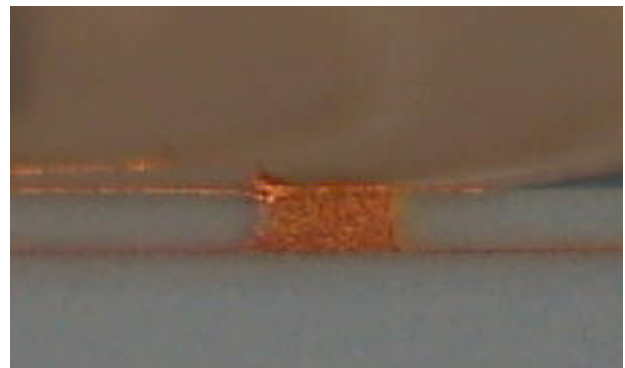


Figure 11. Cross sectional view of a single feature from the interleaved slot EMI shield.

3.3. Solid wall cavity isolation

A combination of techniques has made it possible to construct an experimental solid wall Faraday enclosures. The wall is constructed of

stitched together FTTF. One set of stitches is punched and filled with conductor. The first set of stitches has been staggered for improved mechanical integrity. They are laminated in sets of two, and then the alternate set of stitches is punched and filled with conductor. By collating and laminating these sets of tapes, a single track solid conductor wall is constructed as shown in Figure 12, Figure 13, and Figure 14.

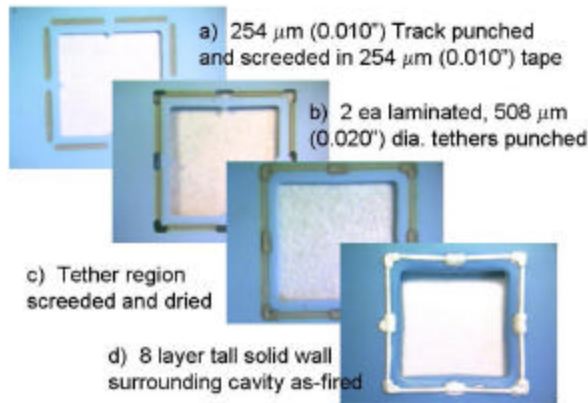


Figure 12. FTTF solid wall construction sequence.

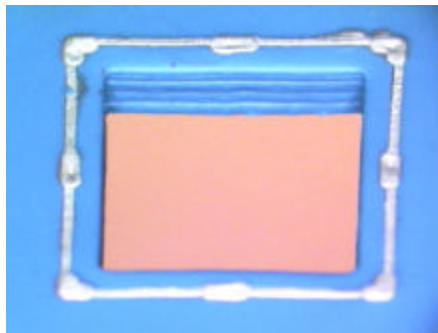


Figure 13. Perspective view of solid wall structure.

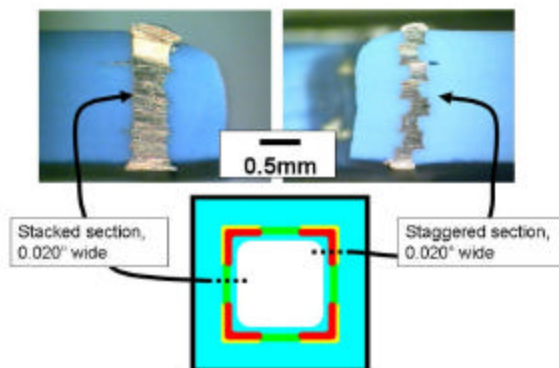


Figure 14. Cross-sectional view of solid wall regions

3.4. Thermal structures

Prior work has used the placement of thermally conductive materials in the form of pastes and tapes.[7,8] Our screeding of 3 mm diameter silver plugs resulted in hermetic seals. These plugs can be used as heat-sinks to exchange the thermal conductivity of LTCC ($\sim 3\text{W/m}\cdot\text{K}$) for that of the fired ink ($140\text{ W/m}\cdot\text{K}$ and higher). Another FTTF that has been fabricated in 500 μm lengths is shown in cross section in Figure 15. These structures have been designed into circuits with particular attention to the locations of hot areas of GaAs RFICs. The interlocking structure promotes mechanical compatibility. Metallization systems for these stacked silver FTTF are currently being evaluated.

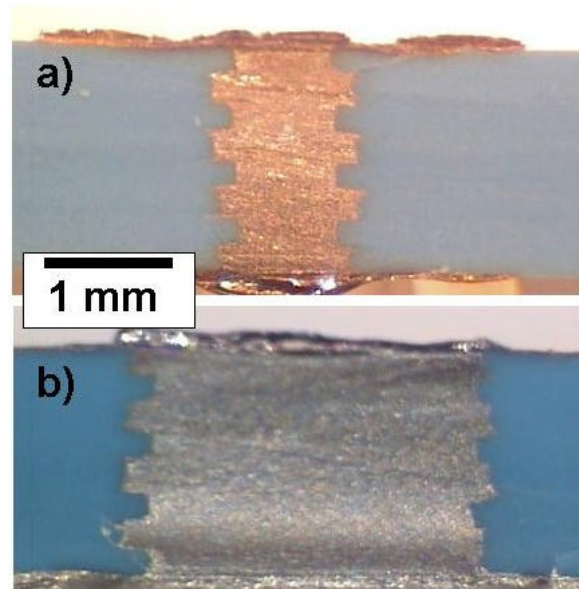


Figure 15. Cross sectional view of a) 0.64 mm wide heatsinks and b) 2.3 mm wide heatsinks (heatsink length is 5 mm).

3.5. Capacitors

Prior work has summarized several techniques for embedded capacitors, including printed paste dielectrics, full thickness tape inlays, and continuous layers of tape dielectric.[9] Another description locally places inlays of dielectric tape.[10] Another FTTF termed 'paste filled cavity' has been described.[11] In early evaluations on thick film capacitors using vendor materials, shorting proved to be a problem. Pinhole free printing would be thought to solve this problem. As with isolation dielectrics, multiple prints can be used to mitigate shorting. Another technique has been employed that is a trade-off using FTTF techniques or what have been known as via capacitors. To minimize the penalty due to the

increased gap, 51 μm tape (0.002") was used. Due to the difficulty of handling this tape, it was prelaminated to the bottom electrode layer prior to dielectric screening. An example of this pattern is shown in Figure 16. This pattern was employed to provide many capacitor edges where shorts would be accentuated if they were to be a problem. The dielectrics were three high-K compositions supplied by DuPont (K=60, 500, and 1800). Cross sectional views of the dielectric and tape only are shown in Figure 17. The capacitor values resulting from the pattern shown above are indicated in the plot of Figure 18. Finally, sawn cross sections of the actual capacitors are shown in Figure 19. Additional testing of these capacitors is ongoing.

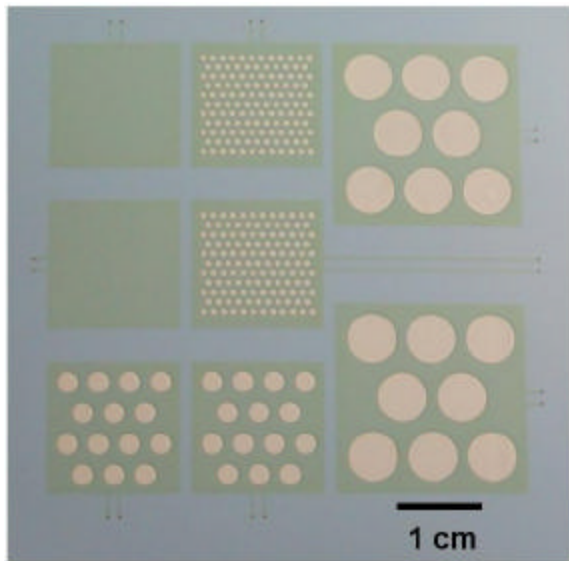


Figure 16. Screened dried unfired capacitors ready for lamination of top plate.

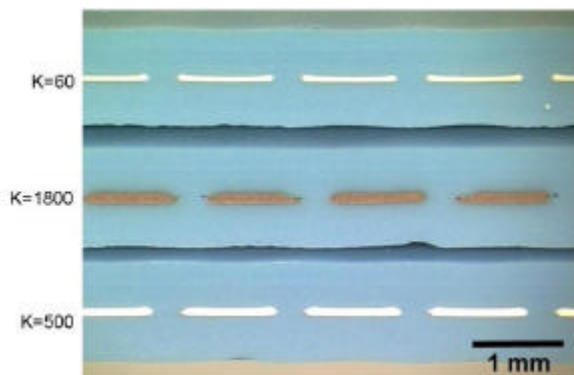


Figure 17. Cross sectional view of FTTF capacitor structure

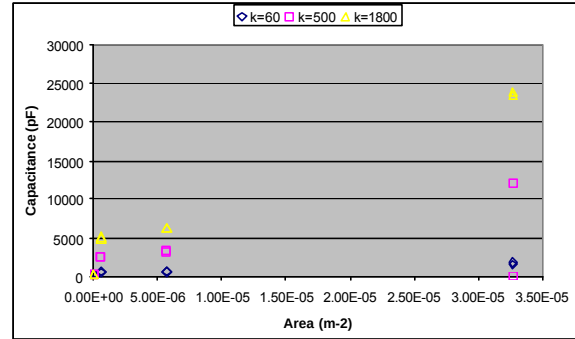


Figure 18. Capacitance related to area of dielectric FTTF.

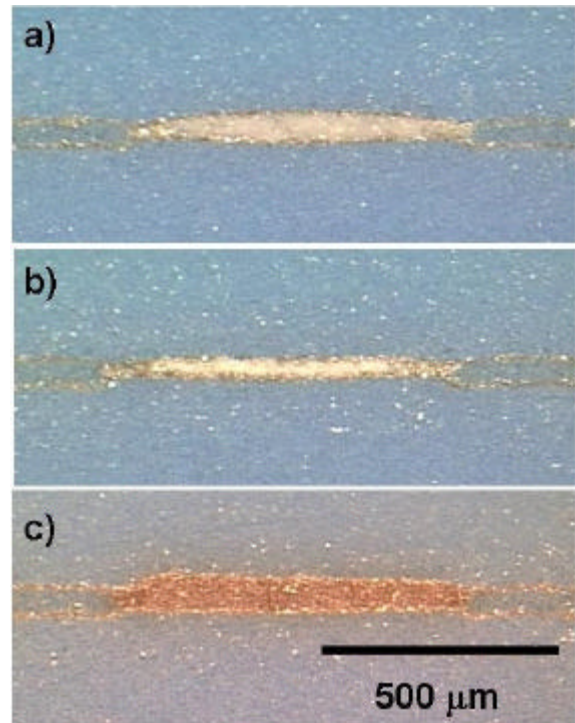


Figure 19. Capacitor cross sections for a) K=60, b) K=500, and c) K=1800 dielectrics

3.6. SVMs

Sacrificial volume materials (SVM) are used in another form of FTTF—internal unfilled volumes in LTCC devices. While the feature left behind is a void in this case, they can be interconnected, staggered, stacked and otherwise integrated. By stenciling, dispensing, screening, or otherwise applying an SVM, the volume is preserved during lamination. Thermally fugitive materials can affect the finished product according to their behavior with respect to compliance, thermal expansion, softening, melting, boiling, condensation, pyrolysis, sublimation, exothermic and endothermic reactions, combustion, delamination, and shrinkage.

Presently, the goal of using SVMs as an addition to the suite of materials used in familiar thick film and dielectric tape techniques is being realized to create enclosed unfilled volumes for channels and cavities. We have also obtained setter pastes and mixed pastes which consist of a carbon paste mixed with a setter paste.[12] Several prototypes have been fabricated by serial lamination for proof of concept when individual filled layers were hard to handle without damage. Yet only when individual tape layers can be handled with filled microfluidic channels does the technique take full advantage of existing practice and avoid the prior inefficiencies of fabrication associated with serial processing.

Channels can be incorporated by standard punching and laminating. They can also be punched into tape layers which are then filled with SVM. Another technique is to pattern SVM by a variety of techniques and permit the lamination step to deform the tapes to a net shape which is functional and easy to make. Figure 20a shows an example of closely spaced channels fabricated by filling pre-punched features. Figure 20b shows a comparable result fabricated by laminating intact tape layers between staggered arrays of SVM channels. The resulting

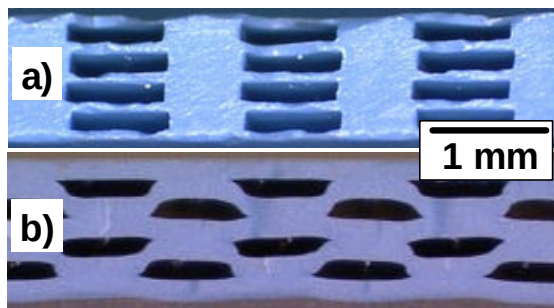


Figure 20. a) Channels that are predefined (punched) and SVM-filled prior to lamination are compared to b) channels formed by patterned SVM during lamination.

wall shape in the latter case indicates a sharing of thickness of the backing helps add thickness in view of the shrinkage of the carbon paste (TFT Paste-CARB-1 High Viscosity) [12] upon drying. Multiple screeding passes may also be used. An example of screeding of open ports in LTCC for a microfluidic pattern to match the backside of a silicon microfluidic die is shown in Figure 21. The streaking shown atop the vendor's polymer backing in Figure 21a is an artifact of the squeegee and the fine size of the carbon particles. This is analogous to the smear that remains on a thick film screen or stencil under certain circumstances. The same properties make

cleanup of the paste more challenging than with other thick film pastes but this is an acceptable inconvenience.

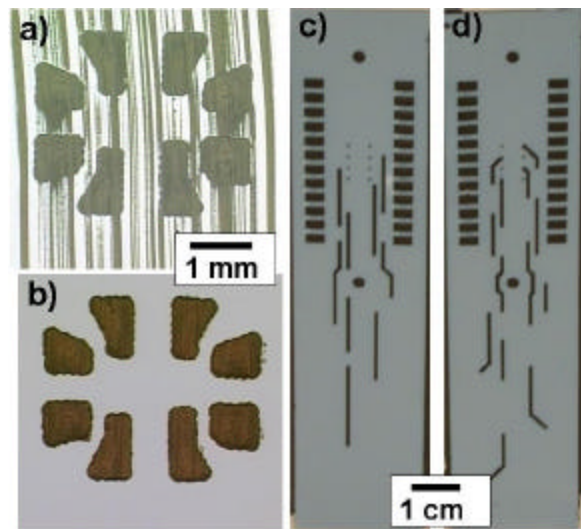


Figure 21. Screeding carbon paste onto unfired tape masked by a punchable backing is shown a) with backing intact and b) with backing removed. Screeding is used for a microfluidic module in c) and d) to preserve channels during lamination.

The structure in Figure 21b results when this backing is peeled off. The slight bleeding of carbon between backing and tape, shown at edges in Figure 21b, arises from separation of the backing from the tape at the deformed edge of a punched perforation. We have experimented with re-lamination of these layers, but prefer to use squeegee pressure to seal the backing to the tape. The bleeding can largely be eliminated as shown in the more complicated screeded device of Figure 21c. Punching with the backing facing the punch, rather than the die, is also helpful in minimizing the separation. In addition, screeding ceramic tape on a polymer film release layer backing that is stretched and held in tension until carbon paste dries has significantly enhanced yield and handling durability of filled channels. This permits the release layer to detach itself from the tape in a shear mode. While long channels can be filled successfully, the tape handling results are better when a channel on a single layer can be stitched to run instead between two available layers with overlapping segment ends. This avoids long slits in the tape and tethers the smaller open areas to reduce its tendency to deform or break in handling. This channel geometry is more than tolerable for many applications and actually ideal for others such as micromixers.[13]

4. Conclusions

We have discussed processing techniques we have used to accomplish particular structures based on filling the thickness of an LTCC tape layer with conductors, dielectrics, and sacrificial volume materials.

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