

## BEOL Thermal Characterization for 3-D Packaging

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### Abstract

*Little research has been conducted to thermally characterize the Back End of Line (BEOL) interconnects since they play little role in conventional 2-D electronic packages. This is changing with the emergence of 3D packages, which place BEOL layers directly in the primary thermal path when die are stacked. In this study we look at the impact of the BEOL layers on a realistic 3-D stacked package to gauge the thermal penalty and to understand the necessary accuracy for BEOL thermal resistance calculations. We then describe various BEOL structures and evaluate the thermal resistance using detailed finite element micro-models. We compare the results to analytical techniques and simple approximations schemes to find effective resistance values that can be used in conventional package or system level thermal models. The primary goal of the work is to establish suitably accurate ways to account for different BEOL designs in a macro-level model.*

Key words: BEOL, thermal resistance, modeling, effective resistance

### Introduction

Although significant work has been undertaken to understand the mechanical and electrical reliability of BEOL structures, little thermal analysis of the BEOL structures has been conducted. Much of the previous thermal analysis has been focused on the Joule heating effects of small scale interconnects. The BEOL layers are not in the primary thermal path (from transistor to heat sink) for most high power applications, which to date have been primarily 2-D flip chip packages.

Some of the previous works include Gill [1] who used quasi-analytical models to calculate effective thermal conductances of different BEOL geometries. The work was based on the results of Harmon [2] and Billotti [3] who used Schwarz-Christoffel transforms to solve for the conductances of simple geometries. Measurement results agreed well with the models, however the geometries were simple enough to model in 2-D, and the model did not account for the surrounding metal structures.

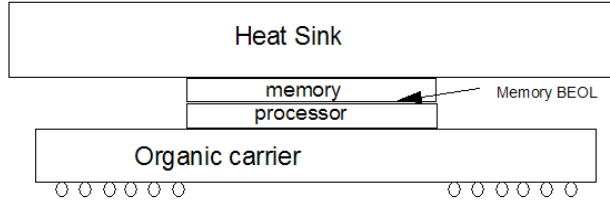
Ney [4] looked at extracting values for models based on Billotti's work, which accounted for several heat flow paths and edge effects that were neglected by the previous works. Chen [5] measured the thermal resistance of various BEOL stacks with different line widths, spacings, and dielectric materials. No vias were included however. Effective thermal conductivities were extracted using the Harmon-Gill model. In [6], Chiang used a closed

form solution to the problem of an embedded wire with vias at both ends. The modeling incorporated shape factors in the equations, which would have to be found numerically or analytically. An earlier publication of Chiang [7] summed the temperature rise of each level to get the total temp rise for any multilevel structure. However, the solutions did not include the temperature field within the vias, as was in [6]. Other strategies included the work of Filippi [8] who applied for a patent for the basic concept of pixelizing a geometry, and calculating effective properties for each pixel for macrolevel analysis. The work of Lee [9], which used energy integrals to find effective conductivities of a composite material, is part of a larger class of work focused on finding effective conductivities for multiphased materials, where inclusions of one material are randomly or orderly distributed in another matrix material. However, the materials can generally be assumed homogeneous or made of very repetitive simple geometries, such as an ordered array of metal cylinders in a cubic block for example. This does not represent the typical geometry of BEOL layers.

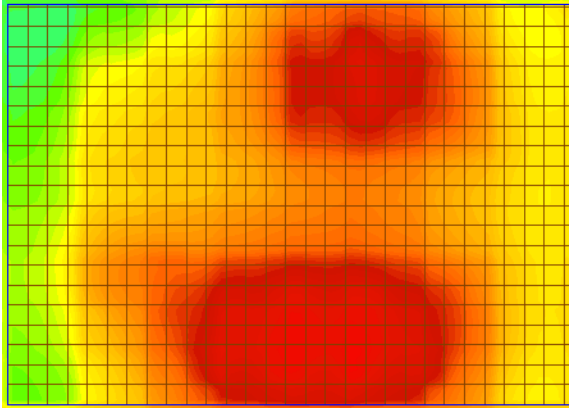
### Impact on Junction Temperatures

To gauge the impacts on chip temperatures in actual applications and estimate the required accuracy of effective-resistance calculations of BEOL layers, a package level model was created which incorporated realistic application boundary

conditions. The Flotherm™ finite volume modeling tool was used. A two-stack die containing a memory on top of a high powered processor was modeled. An organic carrier connected the stack to a printed circuit board, and an aluminum heat sink base was attached to the back side of the memory die. A heat transfer coefficient was applied to the heat sink base to simulate the heat sink performance. The heat transfer coefficient was based on actual heat sink performance for consumer applications in the 50W range, and suitable resistance values were used for interface materials. The processor dissipated 50W total power distributed on a 120 mm<sup>2</sup> die with multiple high power core regions. Figure 1 shows a schematic of the 3D structure, and Figure 2 is a temperature map of the processor showing the hotter core regions (red). The average power density of the die was approximately 0.5 W/mm<sup>2</sup> and peak power densities were over 2 W/mm<sup>2</sup>.



**Figure 1.** 3D package showing main components



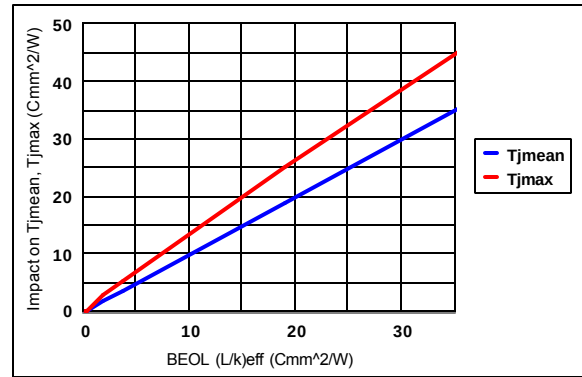
**Figure 2.** Die temperature map of processor in 3-D package.

Figure 3 shows the total thermal resistance impact (from processor junction to ambient) as a function of the BEOL resistance of the memory die. The BEOL resistance is in terms of the ratio of effective thickness to effective conductivity  $(L/k)_{\text{eff}}$  of the entire stack and is given in units of Cmm<sup>2</sup>/W, and can be thought of as an area normalized thermal

resistance. The y-axis gives the impact to the total resistance normalized to the chip area, for both Tjmean and Tjmax. It is simply

$$\frac{\Delta T_j}{pwr} \cdot Area_{die}$$

where  $\Delta T_j$  is the difference in temperature with and without the BEOL. This gives consistent units with the BEOL resistance  $(L/k)_{\text{eff}}$ . The BEOL resistance is assumed the same for the entire die area, and although not realistic, is still a safe assumption for the purposes of gauging the sensitivity of the key temperatures as a function of the BEOL resistance.



**Figure 3.** Impact of BEOL resistance on Tjmax and Tjmean for 3D stacked package with ram on top of processor.

The maximum, or peak temperature (Tjmax), is more sensitive to the BEOL resistance and is characterized by the following relation obtained from the modeling results:

$$\left( \frac{\Delta T_{j_{\max}}}{Pwr} \right) \cdot Area_{die} = 1.33 \cdot \Delta BEOL \frac{Cmm^2}{W} \quad (1)$$

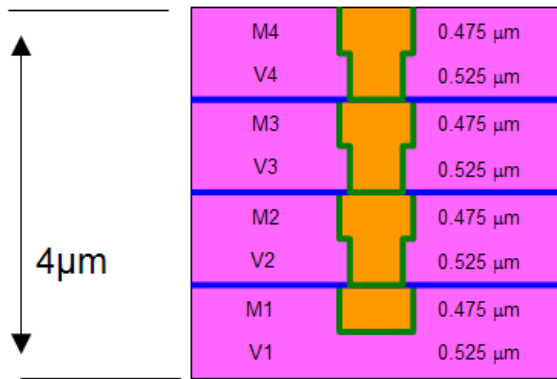
Eq. (1) shows the sensitivity of the maximum junction temperature to the BEOL resistance, for a two stack package with a memory on top of a high power microprocessor, under typical application conditions. In general, a one degree C impact would be well within the uncertainty of most macromodels. For a 100mm<sup>2</sup> die with 50W, the BEOL resistance required to cause 1C temp change would be:

$$\approx \frac{\left( \frac{1}{50} \right) \cdot 100}{1.33} \approx 1.5 \frac{Cmm^2}{W}$$

This implies that we shouldn't be overly concerned with two different designs that have BEOL resistances that differ less than  $\sim 1 \text{ Cmm}^2/\text{W}$  for typical applications.

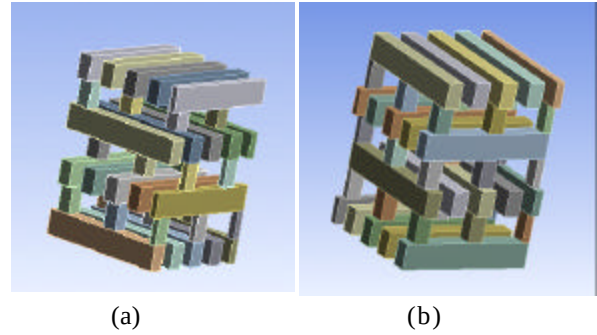
#### BEOL FEM Model Description

The ANSYS<sup>TM</sup> FEM modeling software was used to model various BEOL structures. Figure 4 shows a cross section of a four pair BEOL stack, with thickness dimensions shown. M refers to a metal layer and V refers to a via layer. Actual BEOL stacks can range to 14+ metal layers, with different thicknesses, and the effective resistances calculated in this work would need to be scaled accordingly. The thermal conductivities of the dielectric and metal were assumed  $0.54 \text{ W/mK}$  and  $380 \text{ W/mK}$ , respectively.



**Figure 4.** Cross section of the BEOL stack modeled.

Different in-plane layouts for the metal line and via layers were constructed. Figure 5 shows some isometric views of two different configurations, with staggered connected vias (a) and stacked vias (b). In all cases, the smallest unit cell was modeled, with symmetry conditions on the lateral sides, and constant temperature and heat flux applied on the opposite thru-plane boundaries. The inter-dielectric material is not shown for clarity. In all cases, the lines run parallel in each layer, and perpendicular in adjacent line layers. The line spacings are varied for different designs, and the vias are varied from stacked, to staggered connected; to staggered and not connected, etc.



**Figure 5.** Examples of different BEOL interconnect configurations modeled using ANSYS<sup>TM</sup>: staggered and connected vias shown in (a), stacked in (b).

Table 1 shows the different geometries modeled (designated as A1...F2) and the resulting area-normalized out-of-plane and in-plane resistance  $(L/k)_{\text{eff}}$  in units of  $\text{Cmm}^2/\text{W}$ . Specified are the total metal fraction as well as the metal fraction for the line and via layers (individually). It must be noted that the geometry also includes a layer of pure dielectric with no vias (V1), as shown in Fig. 4. Of interest are the cases with the same metal content in each layer but different configurations, such as A1 and B1; A2 and B2; B1 and C1; F1 and F2, etc. It must be noted that the in-plane component is only for the smallest unit cell for each structure, and over any appreciable area would be significantly large compared to the thru plane resistance, and thus is not a main focus of this work. At the micro-scales, some of the in-plane heat transfer is actually manifested in the out-of-plane component, since the geometry of a single unit cell will have some in plane heat conduction along favorable heat transfer paths such as the metal lines.

**Table 1.** Different designs modeled in ANSYS.  $k_{\text{diel}}=0.54\text{W/mK}$ ,  $k_{\text{met}}=380\text{W/mK}$ .

|    | Via Desc                       | Metal fraction:<br>Total / Line<br>layer / via layer | Out of<br>Plane<br>Norm<br>Rest. | In Plane<br>(per unit<br>cell)<br>Norm Rest. |
|----|--------------------------------|------------------------------------------------------|----------------------------------|----------------------------------------------|
| A1 | Stacked                        | 0.239/.5/.0031                                       | 2.9<br>Cmm <sup>2</sup> /W       | .67<br>Cmm <sup>2</sup> /W                   |
| A2 | Stacked                        | 0.262/.5/.0625                                       | 1.2                              | 0.15                                         |
| B1 | Connected<br>staggered         | 0.239/.5L/.0031                                      | 2.6                              | 0.53                                         |
| B2 | Connected<br>staggered         | 0.262/.5/.0625                                       | 1.3                              | 0.31                                         |
| C1 | Isolated<br>staggered          | 0.239/.5/.0031                                       | 3.6                              | .055                                         |
| C2 | Isolated<br>staggered          | 0.262/.5/.0625                                       | 1.8                              | 0.22                                         |
| D1 | Isolated<br>staggered          | 0.081/.167/.003<br>1                                 | 4.9                              | 1.2                                          |
| E1 | No vias                        | 0.079/.167/0                                         | 5.7                              | 1.3                                          |
| E2 | No vias                        | 0.239/.5/0                                           | 4.1                              | 0.21                                         |
| F1 | Stacked<br>(small<br>spacing)  | 0.24/.5/.0069                                        | 2.9                              | 0.32                                         |
| F2 | Stacked<br>(larger<br>spacing) | 0.24/.5/.0069                                        | 3.0                              | 0.53                                         |

### Analytical Modeling

The steady-state, orthotropic conduction equation with no heat generation, in Cartesian coordinates is as follows:

$$\frac{\partial}{\partial x} \left( k_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( k_y \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left( k_z \frac{\partial T}{\partial z} \right) = 0 \quad (2)$$

where the  $k_x$ ,  $k_y$ ,  $k_z$  are the thermal conductivities in the respective directions. For orthotropic and heterogeneous materials,  $k_x$ ,  $k_y$ ,  $k_z$  could be different in different regions. Rather than explicitly modeling the geometric intricacies, it is desired to find effective conductivities that allow simplified, representative geometries. The simplified models in this work are of two types: regression fits of FEM modeling results and the more generalized approximations based solely on fractions of metal and dielectric in the geometries. The first are specific to certain designs but more accurate since they account for the geometry details, the second type are more generic but less accurate.

We begin with the models using the FEM results as calibrations. The structures of Table 1

were modeled with varying metal and dielectric conductivities. The results were curve fit using linear regression, to the following function:

$$(L/k)_{\text{eff}} = \frac{p}{k_{\text{diel}}^m k_{\text{met}}^n} \quad (3)$$

where  $k_{\text{diel}}$  and  $k_{\text{met}}$  refer to the thermal conductivities of the dielectric and metal, respectively, and  $p$ ,  $m$ ,  $n$  are different constants for each design. The results are valid for  $0.3 < k_{\text{diel}} < 3.0$  and  $100 < k_{\text{met}} < 380$  w/mK. Table 2 gives the constants for each design.

**Table 2.** Coefficient values for designs to give  $(L/k)_{\text{eff}}$  using eq. (3).

| structure | p      | m      | n      |
|-----------|--------|--------|--------|
| A1        | 3.8864 | 0.8600 | 0.1377 |
| A2        | 1.3153 | 0.8678 | 0.0993 |
| B1        | 3.8872 | 0.8353 | 0.1534 |
| B2        | 1.4901 | 0.8561 | 0.1158 |
| C1        | 2.5094 | 0.9553 | 0.0391 |
| C2        | 1.4711 | 0.9272 | 0.0598 |
| D1        | 3.4340 | 0.9482 | 0.0396 |
| E1        | 2.8000 | 1.5924 | 0.0527 |
| E2        | 2.2271 | 1.0470 | 0.0048 |
| F1        | 2.9600 | 0.8936 | 0.0949 |
| F2        | 3.0230 | 0.8958 | 0.0941 |

Table 3 gives the results of equation (3) and compares to the FEM model (Table 1) when the dielectric conductivity is 0.54 and metal conductivity is 380 W/mK. As can be seen the agreement is excellent and the error is in general in the second digit.

**Table 3.**  $(L/k)_{\text{eff}}$  using eq. (3) and FEM model for  $k_{\text{diel}}=0.54$  and  $k_{\text{met}}=380\text{W/mK}$ .

| Structure | Eq. (3)<br>$(L/K)_{\text{eff}}$<br>Cmm <sup>2</sup> /W | FEM<br>$(L/K)_{\text{eff}}$<br>Cmm <sup>2</sup> /W | % Diff |
|-----------|--------------------------------------------------------|----------------------------------------------------|--------|
| A1        | 2.9                                                    | 2.9                                                | 0.5    |
| A2        | 1.2                                                    | 1.2                                                | 3.7    |
| B1        | 2.6                                                    | 2.6                                                | 0.6    |
| B2        | 1.3                                                    | 1.3                                                | -2.4   |
| C1        | 3.6                                                    | 3.6                                                | -0.4   |
| C2        | 1.8                                                    | 1.8                                                | 1.4    |
| D1        | 4.9                                                    | 4.9                                                | -0.7   |
| E1        | 5.5                                                    | 5.7                                                | -4.2   |
| E2        | 4.1                                                    | 4.1                                                | 0.6    |
| F1        | 2.9                                                    | 2.9                                                | 0.7    |
| F2        | 3.0                                                    | 3.0                                                | 0.1    |

Eq. (3) however does not account for other metal and dielectric fractions besides those of structures A1...F2. Less accurate models can be used to generalize to all geometric configurations and metal fractions. The Maxwell model for low volume fraction inclusions in a matrix is given by [10]:

$$\frac{k_{eff}}{k_a} = 1 + db\Phi_b$$

$$b = \frac{\frac{k_b}{k_a} - 1}{\frac{k_b}{k_a} + (d - 1)} \quad (4)$$

where the subscripts a and b refer to the matrix (in this case dielectric) and inclusion (in this case vias and lines) and  $\Phi$  is the volume fraction, k the conductivity. The parameter d accounts for the shape of the inclusions: 3 for spheres, 2 for parallel thin cylinders normal to the flux direction [10]. The generalized form for higher volume fractions is

$$\frac{k_{eff}}{k_a} = C_o + C_1\Phi_b + C_2\Phi_b^2 + C_3\Phi_b^3 + \dots$$

Fitting of the first four terms of the above with the numerical results for  $k_b = 380\text{W/mK}$  gives the following

$$\frac{k_{eff}}{k_a} = -15.12 + 382.41\Phi_b - 2653.5\Phi_b^2 + 5694.04\Phi_b^3 \quad (5)$$

Calculating the  $(L/k)_{eff}$  and comparing with the FEM results is shown in Table 4.

**Table 4.** FEM vs. regression fitting of the Maxwell form for the cases studied.

|    | Eq. (5)<br>(L/k) <sub>eff</sub><br>Cmm <sup>2</sup> /W | FEM<br>(L/k) <sub>eff</sub><br>Cmm <sup>2</sup> /W | %Diff |
|----|--------------------------------------------------------|----------------------------------------------------|-------|
| A1 | 3.0                                                    | 2.9                                                | 5     |
| A2 | 1.4                                                    | 1.2                                                | 16    |
| B1 | 3.0                                                    | 2.6                                                | 17    |
| B2 | 1.4                                                    | 1.3                                                | 7     |
| C1 | 3.0                                                    | 3.6                                                | -16   |
| C2 | 1.4                                                    | 1.8                                                | -23   |
| D1 | 5.0                                                    | 4.9                                                | 3     |
| E1 | 5.5                                                    | 5.7                                                | -3    |
| E2 | 3.9                                                    | 4.1                                                | -4    |

|    |     |     |    |
|----|-----|-----|----|
| F1 | 2.9 | 2.9 | 1  |
| F2 | 2.9 | 3.0 | -3 |

As can be seen from Table 4, the results are not as good as those from eq. (3), although the errors are less than 1Cmm<sup>2</sup>/W and should be considered adequate. It must be noted however that these results are for a four layer BEOL, and would have to be scaled appropriately for higher numbers of layers. A further limitation is that only continuous line segments were considered. The advantage of eq. (5) is that it is a simple expression which only includes the total metal fraction and the dielectric thermal conductivity as variables. The metal conductivity is assumed as 380W/mK.

Other simpler models, based on series, parallel approximations are also possible and can be generalized to all conductivities and metal fractions. In this analysis, the via and line layers are each calculated separately, assuming parallel heat transfer paths, and then the layers themselves are in series. This results in the following relationship for finding  $(L/k)_{eff}$  in the thru-plane direction:

$$\left(\frac{L}{k}\right)_{eff} \approx N \left( \frac{L_{lines}}{\Phi_{lines}^{met} k_{lines}^{met} + \Phi_{lines}^{diel} k_{lines}^{diel}} \right) + V \left( \frac{L_{vias}}{\Phi_{vias}^{met} k_{vias}^{met} + \Phi_{vias}^{diel} k_{vias}^{diel}} \right) \quad (6)$$

where N is the number of line layers, V is the number of via layers and L refers the thickness of the respective layers. The results of equation (6) for the various geometries are compared to the FEM results in Table 5.

**Table 5.** Comparison of effective resistance from eq. (6) compared to the FEM results for the different structures.

| Structure | Eq. (6)<br>(L/K) <sub>eff</sub><br>Cmm <sup>2</sup> /W | FEM<br>(L/K) <sub>eff</sub><br>Cmm <sup>2</sup> /W | %Diff |
|-----------|--------------------------------------------------------|----------------------------------------------------|-------|
| A1        | 1.9                                                    | 2.9                                                | -34   |
| A2        | 1.1                                                    | 1.2                                                | -8    |
| B1        | 1.9                                                    | 2.6                                                | -27   |
| B2        | 1.1                                                    | 1.3                                                | -15   |
| C1        | 1.9                                                    | 3.6                                                | -47   |
| C2        | 1.1                                                    | 1.8                                                | -39   |
| D1        | 1.9                                                    | 4.9                                                | -61   |
| E1        | 3.9                                                    | 5.7                                                | -32   |
| E2        | 3.9                                                    | 4.1                                                | -5    |

|    |     |     |     |
|----|-----|-----|-----|
| F1 | 1.5 | 2.9 | -48 |
| F2 | 1.5 | 3.0 | -50 |

The results of Table 5 suggest simple averaging schemes using parallel and resistance network without accounting for actual geometric configurations would not be sufficiently accurate representations for the BEOL thermal resistance. However, for very low power applications this estimate might be better than not accounting for the BEOL at all. It is interesting to note that Eq. (6) consistently under-predicts the thermal resistances.

### Future Work

The structures described in the modeling section will be incorporated into a test vehicle for model validation. Heaters and sensors will surround the structures to simulate 1-D heat conduction and the results will be compared to the modeling. Details of the test vehicle and results will be described in follow-on work.

### Summary and Conclusions

In this work we estimated the thermal impact of the BEOL resistance on the overall junction to ambient resistance for typical applications. We analyzed typical BEOL structures and calculated the effective thermal resistances which could be incorporated into macro-level thermal models. Detailed finite element micro-models were used for calibration or verification of simple analytical approximations. The main conclusions were:

- For typical applications, an error of  $1\text{Cmm}^2/\text{W}$  or less in BEOL stack resistance would fall well within the uncertainty of a macrolevel thermal model.
- The analytical models which are based on specific geometries and calibrated by numerical models can give very accurate results.
- The more generalized models which do not account for geometric factors may only be suitable for very low power applications.

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