

Thermal Simulations for 4-Layer Stacked IC Packages

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Abstract

Since the shortened wiring length between devices and chips in stacked IC package can reduce the signal delayed effects and improve many electrical characteristics, the topics of stacked IC package are now being studied extensively. Although the electrical benefits are greatly increasing in stacked IC packages, their corresponding thermo-mechanical problems are raising as well, including the problems of heat dissipation, induced stresses, interfacial delamination, via cracking and so on. These problems always cause failures or fatigues in stacked IC packages and become critical reliability issues. In order to obtain thermal distributions in stacked IC packages, the 4-layer stacked IC package (chip on chip) with TSV (through silicon vias) structure has been constructed as our test vehicle in this paper. Not only the temperature distributions but also the junction temperature and thermal resistances in 4-layer stacked IC package have been obtained. In addition, the hot spot effects induced non-uniform temperature distributions in the same structure have also been illustrated. These results will be useful design guidelines to engineers when optimum thermal solutions in 4-layer stacked IC package are demanded.

Keyword: Stacked IC, Thermal simulation, Thermal resistance, Hot spot

Introduction

As the electronic industry is making its progress to miniaturize the high performance IC packages in the near future, topics of 3D stacked IC packages are becoming attractive issues in electronic packaging areas. Due to the reason of IC stacking, the heat dissipations and its corresponding thermal induced stresses are more serious than those in traditional single IC package. Hence, problems of thermal induced stresses and thermal resistance are becoming major concerns [1, 2]. Although the use of spacers would cause deformations to packages and result in larger peeling stresses at the interfaces of die/spacer. However, the spacer with high thermal conductivity like Pyrolytic Graph or Diamond like Carbon film (DLC) can be effectively reduced in inner thermal resistance and helpful to uniform the chip temperature. Thus the thermal performance for packages will be greatly improved by employing spacers [3, 4]. For the sake of realizing thermal performance on 3D stacked IC package, the 4-layer stacked IC package with TSV configuration has been constructed as our test vehicle in this paper. Furthermore, unlike the in-plane MCM package, the power density of the stacked IC package is increasing with number of the die. The heat transfer mechanics inside stacked die are more complex than single die package or MCM package. Hence, there is a strong need to improve current capacities for the thermal management of stacked IC package. The challenge for thermal

engineers is to develop effective cooling schemes which are capable to remove the large amount of heat being generated from vertical stacked dies. The thermal management of stacked IC has brought about more attention gradually. In order to investigate the thermal performance of spacer in 4-layer stacked IC package, the computational fluid dynamics is conducted. The temperature profile and junction temperature on stacked IC package with various thermal conductivity of the spacer is illustrated.

Furthermore, the hot spot problems is also catch more attention since they can cause degradation of thermal performances and unacceptable large temperature gradient on dies, which can result in function failure and problems that have not been solved yet [5]. If the hot spot appears in stacked-die packages, the problems become more serious and complex. The passive cooling method by using high thermal conductivity spacer has been selected as the possible solution for stacked IC package with hot spot issue. For the purpose of reducing hot spot effects on thermal performance of stacked IC package, the simulation models with hot spot are employed.

Thermal Modeling for 4-Layer Stacked IC Packages

For the thermal performance analysis of the 4-layer stacked IC packages, a computational fluid dynamics software FloTherm is used to perform

thermal simulation of the package. The TSV structures are designed to connect with the copper micro-bumps directly and filling with copper. Four thin dies (100 μm of thickness) are vertically stacked and attached to the silicon substrate with micro-bumps. Silicon substrate is directly attached to thermal test board by Sn/Ag/Cu solder balls. The micro-bumps are enclosed by spacers that filled the gap between dies (Figure 1 and 2). This package level thermal model simulates experimental set up of the package and the 1S2P thermal test board assembly in an enclosure. In order to simplify the model, the rectangular solid blocks, construct all components including the TSV, micro-bumps and solder balls, with appropriate thermal conductivity in this section. Due to the symmetry characteristic, the model for the quarter section of this package has been modeled. Moreover, each solder ball is modeled as an individual block [6]. The planar heat source is modeled on the die with uniform heat dissipation. Furthermore, the total heat dissipation from the stacked dies is assumed 1W and each die is powered equally. In this study, base on JEDEC standard [7, 8], a three-dimensional laminar flow model is assumed in free convection condition (with an ambient air temperature of 25°C). The schematic view of numerical analysis model of a 3D die stacked packages are shown in Figure 4. The objects of this simulation are used to predict the thermal performance of the 4-layer stacked IC packages with various spacer material that range from 0.1Wm⁻¹K⁻¹ to 500 Wm⁻¹K⁻¹. The geometric dimensions and thermal conductivity of formations of 4-layer stacked IC package are, respectively, shown in Table 1.

Table 1. Geometric dimensions and thermal properties for 4 layer stacked IC package.

Dimensions	Length(mm)	Width(mm)	Thickness(mm)	Thermal conductivity(W.mK)
Silicon die	5.7	5.7	0.1	117.5
substrate	7.0	7.0	0.2	117.5
Test board	114.5	101.5	1.6	18.98(in-plane) 0.315(cross-plane)
Copper TSV	0.1	0.1	0.1	385
Micro-bump	0.2	0.2	0.1	385
Solder ball	0.35	0.35	0.35	58.7

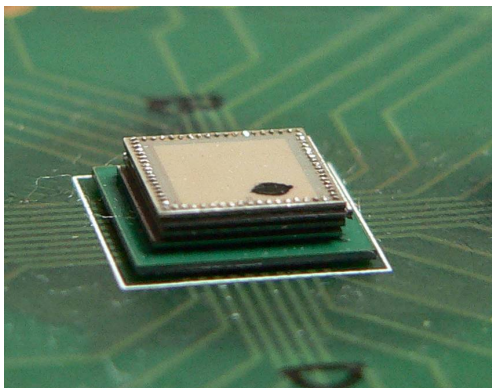


Figure 1(a). 3D 4 layers stacked IC packages.

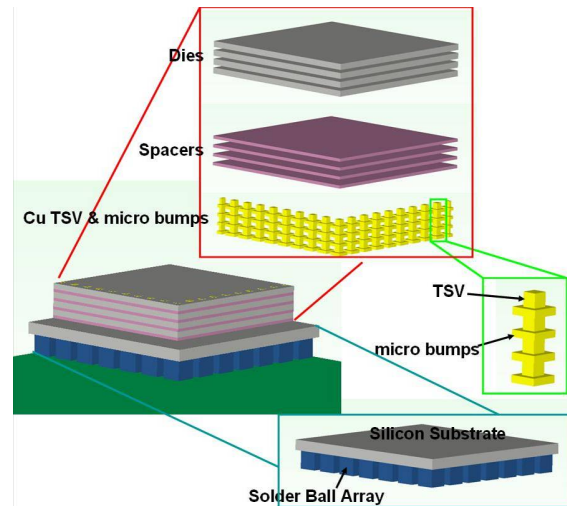


Figure 1(b). Schematics of 4-layer stacked IC package (Due to symmetry, only a quarter of the model is presented).

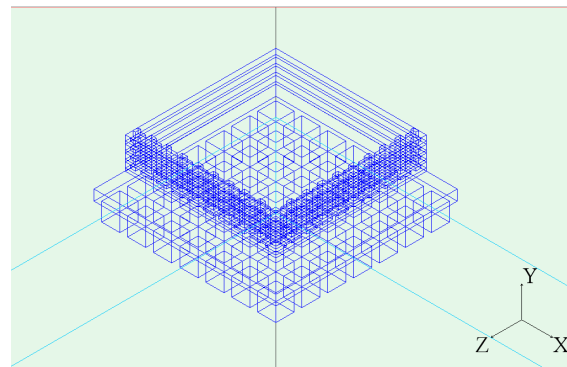


Figure 2(a). Finite volume model of 4-layer stacked IC package (Peripheral TSV and micro-bumps structure).

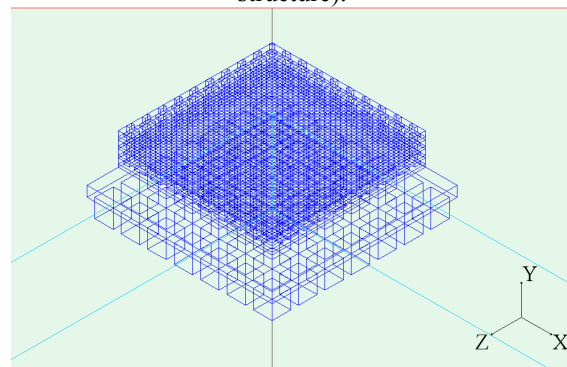


Figure 2(b). Finite volume model of 4-layer stacked IC package (Full array TSV and micro-bumps structure).

Results and Discussion

In general, the thermal performance of an electronic package can be represented by the thermal resistance, θ_{ja} . However, the definition of the thermal resistance for an MCP structure like 3D stacked IC package has yet to be defined. In this study, the maximum junction temperature of the chips is used to calculate the thermal resistance from junction to ambient, θ_{ja} is defined as

$$\theta_{ja} = (T_{j,max} - T_a) / P \quad (1)$$

where $T_{j,max}$ is the maximum junction temperature ($^{\circ}\text{C}$), T_a is the ambient temperature and P is the dissipated power from the 4 chips (watt).

Figure 3 illustrates temperature distribution of stacked IC package in cross section view. It can be investigate the heat transfer characteristics of the package/thermal test board. The heat generated from the each die, most heat flow transfer through the substrate to thermal test board by conduction and finally transfer to the air by convection. Moreover, higher thermal conductivities of the silicon substrate and thermal test board are helpful to spreading the heat flow and reducing the temperature difference on such component. The density differences propel fluid motion caused by temperature differences within fluid. The boundary layer separates from the central port of the downward-facing surface of the thermal test board. Only a few heat flow transfer directly from the die to the air. It is also clearly to observe the high temperature region is concentrate in stacked ICs. The heat conduction path might be obstructed by some resistance such as the gaps/spacers between the dies and the gap between the silicon substrate and thermal test board. Although micro-bumps and solder balls are designed to inside the gaps between dies. However, for the case of the package without spacer, the lower thermal conductivity of air would reduce the equivalent thermal conductivity in those gaps and also increase the thermal resistance. Moreover, the heat source of each die will become the thermal impedance with each other to obstruct the heat conduction from inner stacked dies to the top die or bottom die.

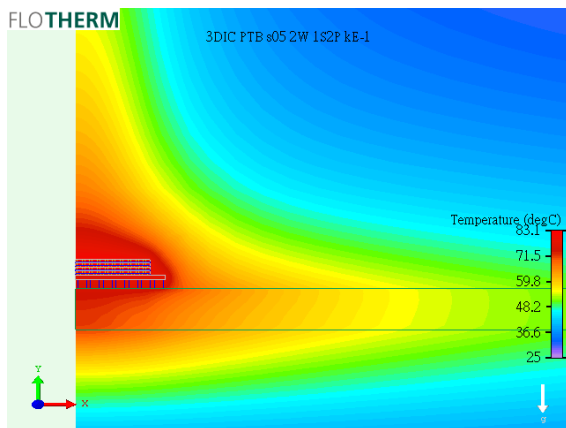


Figure 3. The temperature distribution of stacked IC package in cross section view (operating at 2W total power).

Geometrical effect: TSV and Micro-Bump distribution, thickness of Micro-bump/Spacer

Figure 4 shows the thermal resistances of 4-layer stacked IC packages with two different geometrical designs: full array and peripheral TSV/Micro-bump structures. It is found that the thermal resistance of

the package with full array TSV/Micro-bump shows a level-off trend on the range of various thermal conductivities of spacer except the package without spacer configuration. The reason may also come from the higher equivalent thermal conductivity not only in cross-plane direction but also the in-plane direction. Figure 4 also illustrates the thermal resistance of the case with peripheral TSV/Micro-bump design. Compare with result of the case with full array TSV/Micro-bump structure, there is a significant difference between two packages on thermal resistance. Although the TSV/Micro-bump is a good conductor and can be reducing the internal thermal resistance, however, due to its peripheral structure, the equivalent thermal conductivity is minimal. Therefore, increasing the TSV/Micro-bump area coverage might improve the internal heat conduction between dies. As shown in Figure 5(a) to 5(d), it is clearly to found that the in-plane temperature distribution on the stacked die package with full array TSV and micro-bump structure is more uniform than that of the package with peripheral TSV and micro-bump configuration because of the increasing of the thermal conductivity of TSV and micro-bump can be enhance the heat conduction in-plane direction.

Since the 3D stacked IC packages are expected to be thinner, the studies for effects on thermal performance for reducing bump/spacer thickness of 3D stacked IC package are becoming important. However, by varying the micro-bump/spacer thickness from 50 to 100 μm , there is no significant difference on thermal resistance between two thicknesses of micro-bump/spacer that illustrated in Figure 6.

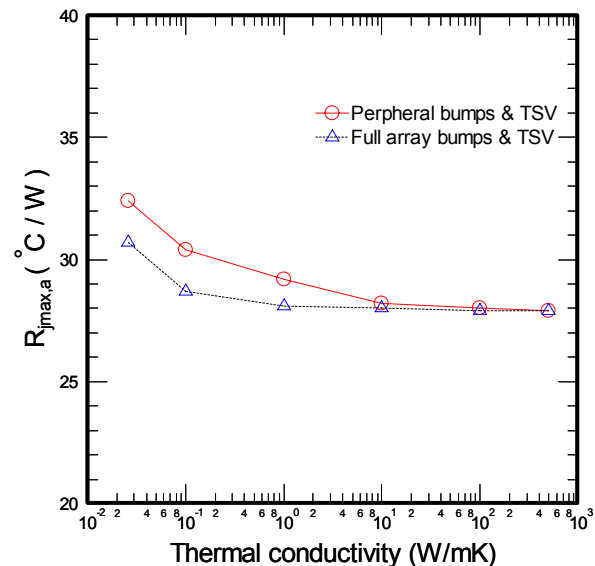
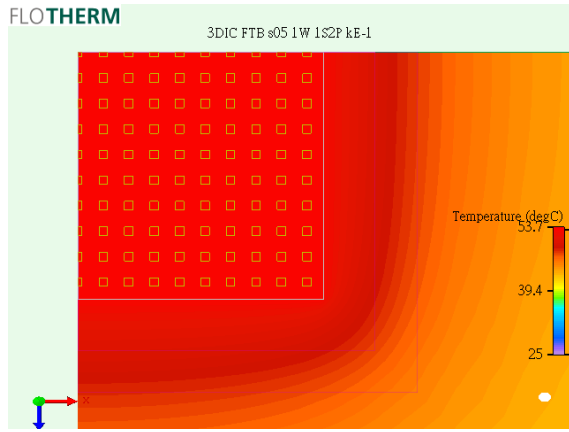
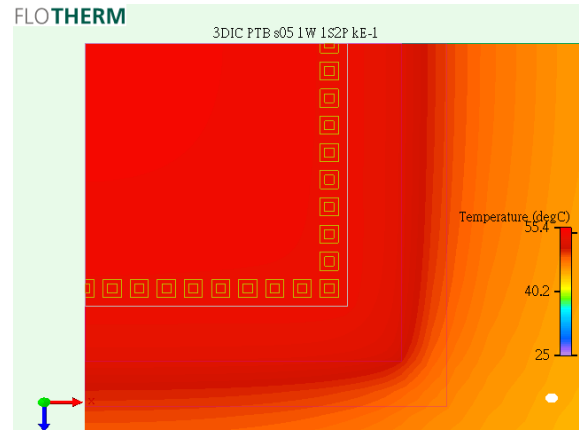


Figure 4. The thermal resistance comparison of the two types of TSV and micro-bump structure designs.

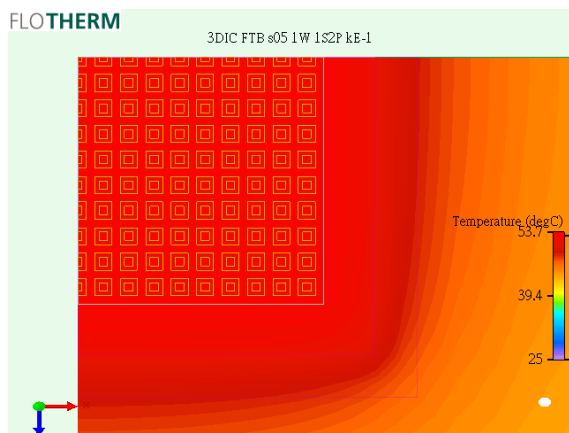


(a) Model with the full array TSV and micro-bump structure (top die).

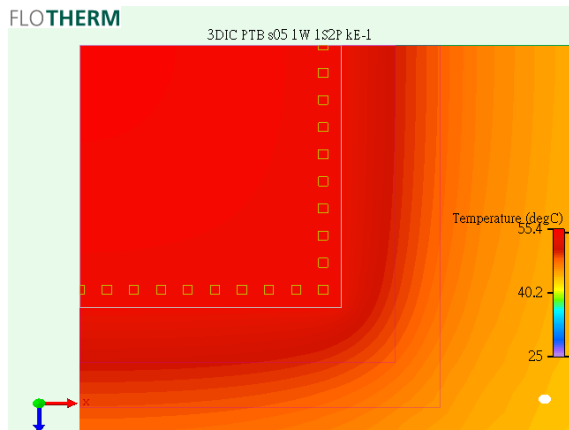


(d) Model of the peripheral TSV and micro-bump structure (bottom die).

Figure 5. The in-plane temperature distribution of the 4-layer stacked IC packages with different TSV and micro-bump structure.



(b) Model of the full array TSV and micro-bump structure (bottom die).



(c) Model of the peripheral TSV and micro-bump structure (top die).

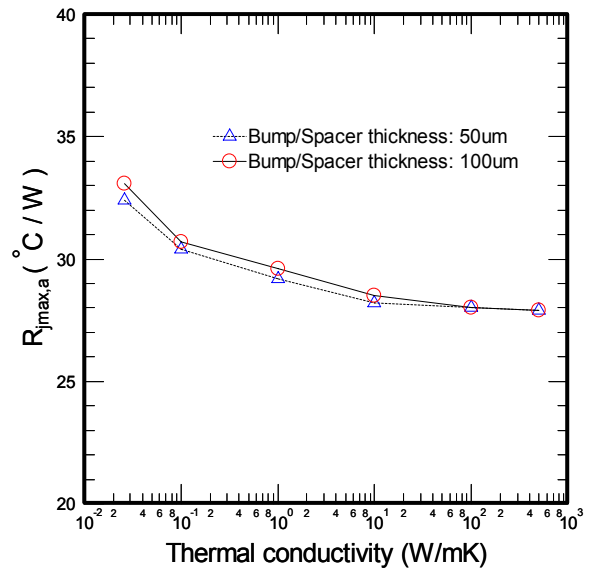


Figure 6. The thermal resistance of the stacked IC packages with two spacer thickness.

Thermal conductivity effects of spacer

The thermal resistances of the 4-layer stacked IC packages operating at 1W and 2W (total power) are shown in Figure 7. The plots presented in Figure 7 illustrate the changes of thermal resistance on stacked IC package with various thermal conductivities of the spacer. The plots show two distinct regions in thermal conductivity of spacer $k_{spacer} < 10 \text{ Wm}^{-1}\text{K}^{-1}$ and $k_{spacer} > 10 \text{ Wm}^{-1}\text{K}^{-1}$. In the region $k_{spacer} < 10 \text{ Wm}^{-1}\text{K}^{-1}$, one can see a significant decrease in thermal resistance that conduction heat transfer contributes the thermal performance of the stacked IC package. However, there is a negligible difference of thermal resistance for the range of $k_{spacer} > 10 \text{ Wm}^{-1}\text{K}^{-1}$. Furthermore, the simulation results demonstrate that the reduction of thermal resistance is limited due to the poor heat

transfer mechanism in vertical direction that conduction heat flow to the thermal test board. It is believed that increasing the thermal conductivity of spacer can reduce the junction temperature of stacked IC package because of the in-plane heat spreading. Although the higher thermal conductivity spacer is a good conductor with small internal resistance, the structure (multi-heat source of each die in vertical direction) might restrict its cross-plane conduction capacity. Therefore, increasing the thermal conductivity of spacer might only improve the in-plane direction heat conduction.

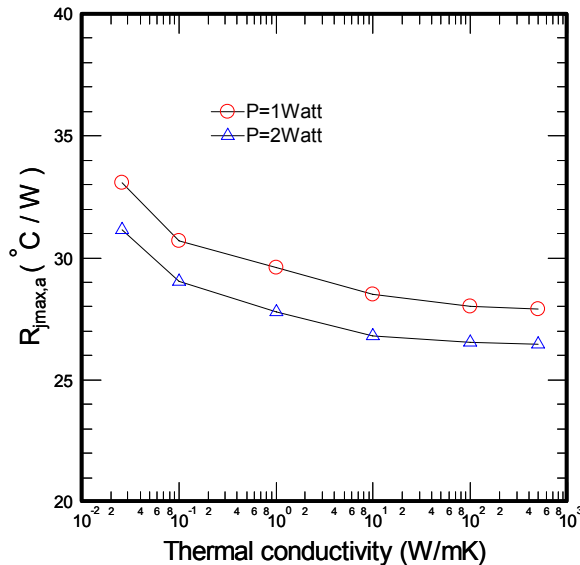


Figure 7. Thermal resistance on stacked IC package with various thermal conductivities of the spacer.

Hot Spot Effects

To investigate the phenomenon of the effects of hot spot on stacked IC package, a hot spot simulation analysis is carried out on 4-layer stacked IC packages. The hot spot region is considered in an area of 500 μ m $\times$ 500 μ m and located on the center of each die. The case of the hot spot simulation is set that hot spot operating at around 0.1W (0.025W for each hot spot) and surrounding area of die operating at around 1W (0.25W for each die). Figure 8 illustrates temperature distribution along hottest die of 4-layer stacked IC package with hot spot. In Figure 8, it is clearly to discern the significant temperature raise is located on the central portion and mostly concentrated on hot spot region. For the case of the stacked die package without any spacer, the temperature difference along the die would reach 40°C and might induce the damage of the die. However, the simulation results also indicate that heat conduction through the spacer with high thermal conductivity can efficiently to reducing the maximum junction temperature in hot spot region and uniform the temperature distribution on dies.

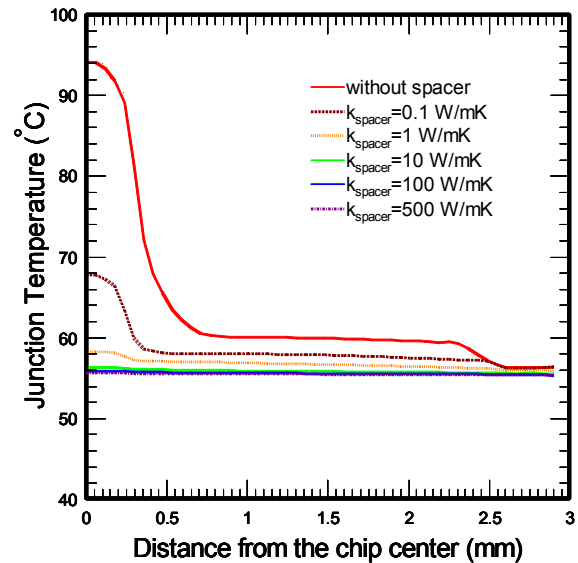


Figure 8. The temperature distribution along hottest die of 4-layer stacked IC packages with hot spot.

Conclusions

A comprehensive study of thermal simulation for 4-layer stacked IC package is presented in this paper. The three-dimensional CFD modeling has been adopted to obtain the thermal resistance and temperature distributions in 4-layer stacked IC package. Compared with the peripheral TSV/micro-bump design, the thermal resistance of the package with the full array TSV/micro-bump design can be reduced significantly. The results also show that there is no significant difference on thermal resistance by varying the bump/spacer thickness from 100 μ m to 50 μ m due to the reasons of smaller inner thermal resistance improvement. Furthermore, it is clearly to found that increasing the thermal conductivity of spacer can reduce the thermal resistance (junction temperature) of stacked IC package and increase the heat conduction in-plane direction in the range of $k_{spacer} < 10 \text{ Wm}^{-1}\text{K}^{-1}$. However, there is a negligible difference of thermal resistance for the range of $k_{spacer} > 10 \text{ Wm}^{-1}\text{K}^{-1}$. The simulation results also indicate that heat conduction through the spacer of high thermal conductivity can efficiently to reducing the maximum junction temperature in hot spot region and uniform the temperature distribution on die.

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