

Wirebondability and Solderability of NiAu electroless front side metalized Silicon wafers subjected to high temperature back end assembly process flows

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Abstract

In this work we analyze the wirebondability and solderability of different electro-less metallization stacks on Aluminum metalized Silicon wafers after exposure to subsequent high temperature back end assembly process steps. In addition, we propose a measure one can take to minimize the adverse impact such high temperature thermal budgets on solderability and wire bondability of various interconnects. In many silicon high power and high speed microelectronic semiconductor applications the need to concurrently and cost effectively implement a solderable, wirebondable and reliable topside metallization is becoming an increasingly desirable feature. This allows for the simultaneous implementation of various front side and back side interconnect solutions in the assembly process which reduce parasitic resistances, inductances and thermal resistances. These features in general enable power devices to achieve higher current ratings, higher switching speeds and improved thermal performance. The challenge associated with the implementation of these features via the use of front side electro-less front side metals is preserving its integrity during exposure to subsequent high temperature back end assembly operations such as thermal annealing and/or high temperature solder die attach. The subsequent high temperature operations have a tendency to degrade the integrity of NiAu based electro-less top metal finishes due to the diffusion of the barrier metal layer (Ni in general) to the top surface. Such mechanisms result in surface oxidization which dramatically reduces the solderability and wirebondability of the front side bond pads. In this work we experiment with different metal stacks of electro-less plated metallization over Aluminum metalized Silicon wafers and study the impact of different thermal budgets and process sequences to the solderability and wirebondability of the final surface.

Key words: electroless, wirebondability, solderability

Introduction

In the field of high power microelectronics the packaging technology is often pushed to its limits due to the application environments and operating conditions in which the devices need to function: high currents, high voltages, high temperature and high levels of power dissipation. These conditions induce high levels of mechanical, thermal and electrical stresses on the completed products.

In addition, as semiconductor performance levels increase over time, the performance capability of the packaging technology selected for final assembly becomes an increasingly larger contributor to overall performance. Thus, in general, the industry demands

the packaging technologies used in power semiconductor applications to demonstrate continuous reductions in parasitic resistances, inductances and thermal resistance while meeting the required manufacturability, cost and reliability requirements. One such application is that of power MOSFETs used in switching power converters. Power Semiconductor devices for these high current applications dictate the use of alternative packaging interconnect solutions such as that shown in Figure 1, which utilizes a mixture of interconnect methods in order to achieve the necessary performance requirements.

The illustration in Figure 1 is that of a packaged MOSFET device which utilizes both a standard wire

bonding interconnect and solder attached clip/strap interconnect. The selection of the optimum interconnect solution is determined by the role each interconnect plays in contributing to final performance. The die in this example is solder die attached, as is the clip, which provides the high current path the largest possible cross sectional area. This design results in very low parasitic resistance, reduced spreading resistance and low inductance while at the same time offering some thermal advantages allowing for improved heat flow via multiple paths. The package and implementation shown has demonstrated significant improved electrical and thermal performance characteristics over standard interconnect solutions.

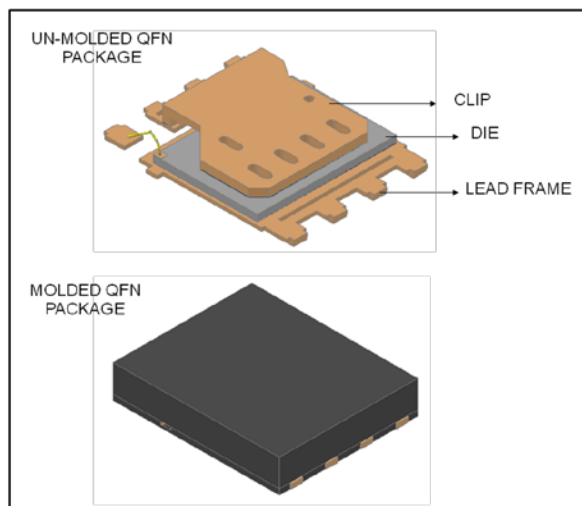


Figure 1: 3D drawing of an unmolded and molded QFN clip package

The challenge, from R&D perspective, in implementing the above mixed interconnect solution is to develop a robust and cost effective set of back end processes for thinned 8 inch Aluminum metalized Silicon wafers that have both a solderable back metal surface finish, and a top metal surface finish that simultaneously supports solderable and wirebondable interconnects. Such must be able to withstand the necessary thermal budgets used in the final assembly of the packaged device and meet the necessary reliability requirements.

The semiconductor industry today offers today various options for the front side and back side metallization of Silicon wafers such as electroplating, evaporation, sputtering and electro-less methods. The election of the optimum method depends of numerous factors such as cost, thermal budgets, performance and device sensitivity.

It has been demonstrated that the secondary x-ray from the evaporation deposition could damage the device in the active area of the wafer when evaporation is used to metalize the front side of the wafer.

One could eliminate this issue by using a sputtering process to deposit a solderable metallization on the front side Al pads. In this case one needs to use also a liftoff process to keep the solderable metal just over the pads. The problem with this option is that this technology is not readily available in most backend subcontractors, the process is not straight forward and the cost is higher than the other options.

On the other hand electroless metallization for the front side is extremely attractive because of simplicity (no photolithography steps needed) and low cost.

Based on these concepts we decided to use electroless deposition for the top solderable metallization and e-gun evaporation for the backside metallization.

In this particular implementation the backside metal is realized using a blanket evaporation of a Ti-Ni-Ag stack where Ti acts as the adhesion layer to the Silicon substrate and the Ni-Ag sandwich serves as solderable and barrier surfaces. One of the most important characteristics of this stack is the contact resistance between the silicon substrate and the metal layers. The contact resistance, along with the adhesion of the metal stack, plays a significant role in determining final MOSFET resistance and interconnects reliability [1]. One method used to ensure low contact resistance at the Ti-Si interface is to implement a post metal deposition high temperature annealing.

The top side metallization requires the deposition to be selective, and only deposited over the defined passivation openings such as those defined as pads. The method considered for the front side was an electro-less metallization technology to realize two final metal stacks: NiAu and NiPdAu.

The implementation of the above two metal deposition process steps have to be carefully integrated into subsequent high temperature back end process and assembly flows since they can easily compromise the integrity of the metal finishes. Some of the issues that incorrect sequencing and integration could create are the following:

1) Degradation of solderability of the front side and backside metallization due to oxidation.

An incorrectly implemented post back-metal deposition high temperature process step will cause diffusion of atoms from the sandwiched layers (Ni in this case) to the surface where it will oxidize in when in contact with oxygen. The oxidation of the top and bottom metallization will degrade the solderability and wire bondability of the surface.

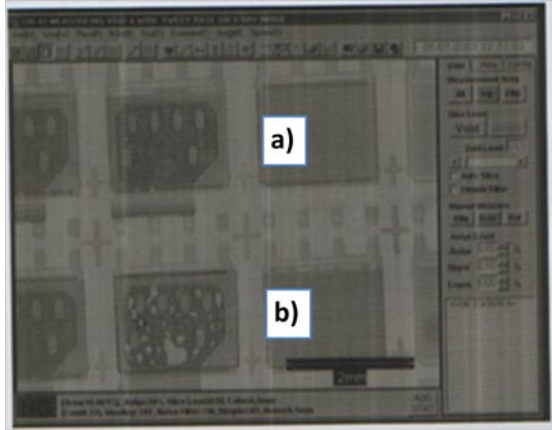


Figure 2: X-ray image showing impact of oxidation on voiding at all solderable interfaces. A) No surface oxidation showing low solder voiding. B) With Surface Oxidation showing high solder voiding.

As you can see the X-ray images of the example shown in Figure 2 the die from a wafer that has been properly exposed to subsequent high temperature process steps prior to die attach exhibits a very low level of solder voiding below 3 % while the die from a wafer that was incorrectly processed and whose surface was allowed to oxidize exhibited solder voiding levels in excess of 11%.

2) Degradation of wire bondability of the front side pads due to diffusion and oxidation of electroless Ni.

Similar mechanisms can impact the integrity of the top metallization and significantly degrade the wire bondability of electro-less NiAu finishes.

High temperature post metal deposition processes also cause diffusion in the top metallization stack. In particular the electro-less Ni diffuses to the top surface and oxidize when exposed to the atmosphere. The NiO_2 in the surface reduces the wire bondability

of the pads on the topside of the die as illustrated in Figure 3.

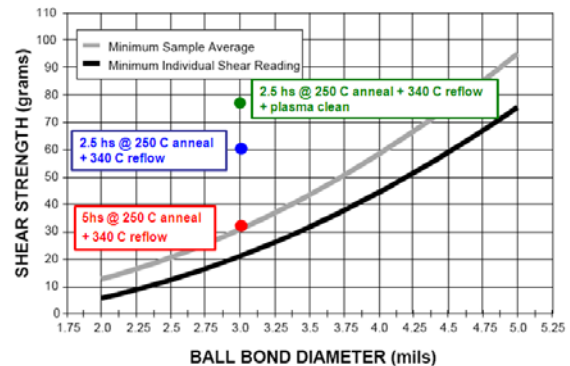


Figure 3: Shear Strength vs. Ball bond diameter for different anneal processes.

The data above exemplifies the impact of Ni diffusing to the surface and subsequently oxidizing as a result of a post metal deposition high temperature process step. The data shown corresponds to the average of 30 ball shear readings. All the wafers were subjected to the thermal conditions indicated in the graph plus a thermal profile to simulate the solder reflow process for high lead solder (max temp 340 C) that the die would see prior to the wire bond operation. We also show in the graph the curves of minimum accepted values form JEDEC spec EIA/JESD22-B116. It is clear from the measurements that post electro-less metal deposition high temperature process steps substantially degrades the shear strength of the wire bonds. For example, reducing the temperature exposure time from 5 to 2.5 hours the shear strength doubles from 31 to 62 grams. One way to improve the quality of the NiAu surface prior to wire bond is an Ar plasma cleaning step that removes the NiO_2 from the pad surface. The results show that the Ar plasma clean improved the ball shear strength by 25%.

3) Wafer warpage due to thermally induced phase transition in the electroless Ni

The electroless Ni-P film used as Under Bump Metallization (UBM) is an amorphous phase after the plating process, and tends to crystallize when exposed to high temperature post metal deposition steps. Indeed, between 350-400 C (depending on the P content) electroless Ni undergoes a phase transition from amorphous to crystalline state [2, 3, 4, and 5]. The phase transformation is accompanied by the depletion of Ni atoms and precipitation of Ni_3P from

amorphous Ni-P. This leads to a volume reduction and an important increase in the tensile stress of the Ni layer.

In Fig 4 we show the warpage of a 200 μm thick 8 inch wafer after different thermal treatments.

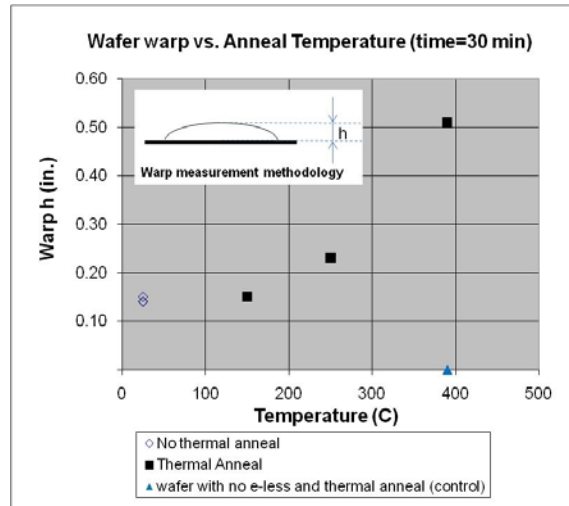


Figure 4: Wafer warpage for different thermal treatments (anneal time=30 min). All the wafers were backside grinded to 8 mils and back-metalized with a TiNiAg stack. The wafer with no electroless NiAu is a control wafer

In order to demonstrate this we exposed several wafers that had been thinned to 200 μm , backside metalized via evaporation with TiNiAg and top side metalized with NiAu using an electroless process to a thermal treatment of 30min at various temperatures. Two wafers of the group were not thermally annealed (points at room temperature in the graph). The control wafer was backside grinded and back-metalized but was not electroless plated in the front-side. As you can see from the graph in Figure 4, post metal deposition high temperature process can significantly impact wafer warpage. The control wafer show no warp indicating that the entire warp measured comes from the Ni phase transition described previously. The wafer with no thermal anneals shows an intrinsic warp as coming out of the plating bath and therefore it is attributable to the electroless NiAu process. This intrinsic warp (0.14 inches) does not constitute an issue since it is under spec for most of the assembly houses.

Recommendations

In the previous sections we explained the challenges one faces in processing double side metalized wafers through subsequent back end assembly processes utilizing mixed interconnect technologies such as top and bottom high temperature solder attach and wire bonding. As we have described before the challenges arise in the solderability of the metal surfaces, wafer warping due to Ni phase transition and wirebondability of the pads after the thermal anneal process. All of these degrade the integrity of the various interconnect interfaces.

In this section we will provide some recommendations and suggested solutions that will minimize such issues.

A) Wafer warpage:

In the case where the backside of the wafers requires a thermal treatment to reduce contact resistance the process sequence we elected to implement was to simply change the order of metallization.

We found that by providing any required thermal treatments to the wafer prior to front side electro-less NiAu plating substantially mitigated this issue. In this particular case we performed the backside wafer thinning, the blanket backside metal deposition and any necessary thermal steps prior to front side electroless metallization. This prevents the front side Nickel layer from transitioning from an amorphous to crystalline state and minimizes the chance and degree warpage.

However the challenge for this process flow is that in the electroless bath the backside of the wafer (already metalized) will plate along with the front side. To prevent the exposed back metal to plate we need to apply a protection to the backside of the wafers prior to the electroless process. The best solution we found is to apply a tape to the backside of the wafer that can withstand the harsh chemical environment of the plating baths without peeling, which would cause a complete failure.

B) Solderability and wire bondability:

It is well known that Pd is a metal that it is wire bondable [6] so the introduction of a Pd layer between the Ni and Au is a potential solution to increase the wire bondability of the top metallization. In fact, by introducing a Pd layer between the Ni and

the Au we are limiting the diffusion of Ni to the surface. Although Ni migration is reduced, atoms from the Pd layer do diffuse to the surface but as previously mentioned Pd is compatible with wire bonding operations so this does not degrade that interconnect. The issue is that Pd is not as good solderable metal as Ni or Au so by improving the wire bond operation we could be endangering the clip solder attach operation.

To evaluate this tradeoff we conducted an experiment to obtain key solderability and wire bondability parameters for several electroless plating stacks. The experiment consisted of plating wafers with three different electroless metallization: NiPdAu, Ni Au and NiPd. The wafers were exposed to a post metal deposition thermal step and assembled up to the wire bond step. Some units were assembled without the clip interconnect step to obtain the solder voiding data of the backmetal only. The rest of the units were assembled with the clip attach and the Au wire bond using the standard assembly process for these devices. The data collected on these different cells is shown in Table 1.

	NiPdAu	NiAu	NiPd
Solder voids:			
Without clip (spec 10% max)	0.29%	0.85%	0.35%
With clip (spec 10% max)	10.29% (fail)	1.12%	2.40%
Wire bond:			
wire Pull test	ok	ok	ok
Ball Shear Test (spec 80.5g min)	135 g	95 g	16.2 g (fail)

Table 1: Results of solderability and wire bondability tests to compare the performance of different electroless topside metallization.

The voiding was measured with X-ray imaging technique and the ball shear and wire pull was measured with standard equipment. Please note that when we X-ray image a part assembled with clip we measure the voiding from both interfaces: die attach and clip attach. This is also the reason why we decided to measure some units without clip so we can see the contribution from each solder joint to the total voiding number.

As you can see from the results, the NiPdAu cell shows the best ball shear test results (as expected) but the solderability is degraded. In fact the parts assembled with NiPdAu top metal do not comply with the specs (max 10% voiding) as measured with X-ray imaging. The fact that the voiding of parts without clip show less than 2% voiding indicates that

the major contributor to voiding in this case is the top metal. NiPd exhibits good solderability results but it fails in the ball shear test (16.2 grams).

Finally the units processed with just NiAu exhibit the best tradeoff between wire bondability and solderability.

Conclusions:

In this work we have presented the challenges and the solutions associated with design of a high performance, high reliability package for microelectronic power applications. These challenges are mainly based on the fact that, to obtain extremely low parasitic values, the die needs to be sandwiched between two thick Cu layers, i.e. leadframe and clip (clip QFN technology). To that end the die needs to have solderable metallization on its top and its bottom. In addition the wafers need to be annealed to minimize the metal-semiconductor contact resistance to reduce the total package resistance. The post metal deposition high temperature anneal causes several problems like diffusion and oxidation of the wafer metallization stack which degrades solderability and wirebondability. The anneal process also causes wafer warpage when Ni-based electroless metallization is used.

As a solution to these challenges we developed a process flow and a metal stack that addresses all of the above issues. We found that a modification of the process flow solved the wafer warping issue and a study of different electroless metal stacks showed that the NiAu electroless stack resulted in the best solution.

The technology we developed satisfies all the requirements from a performance and reliability point of view and qualifies as a platform that is useable for a wide portfolio of products.

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