

Enabling of Off-the-Shelf IC for Parallel Stochastic Self-Assembly

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Abstract

Parallel stochastic self-assembly techniques are promissory process alternatives replacing common pick and place methods for small devices. Companies have adopted self-assembly techniques to place and fabricate micro chips in high volume RFID devices. The objective of this study and process development was to enable the fabrication of IC chips for a parallel stochastic assembly process (PSAP) using components-off-the-shelf (COTS). Previously only custom designed IC chips or application-specific IC chips (ASIC) have been used in PSAP. A commercially available memory chip with rectangular form containing 8 I/O pads was used to test the concept in a RF micro sensor application. The chips were obtained in wafer form and the I/O pads were relocated into symmetrical arrangement by adding a redistribution layer (RDL) with vias to the original pads. A chip with simple shape, such as rectangle or square and symmetrically arranged pads will increase the PSAP yield while fully utilizing the economical benefits of the process; the chip orientation in the receptor site becomes irrelevant while its unique size and shape ensures that it settles in the correct place. This paper presents the design steps, processes, and materials used in the fabrication of redistribution layer for off-the-shelf IC components.

Key words: Self-assembly, Redistribution Layer, Components Off-the-Shelf, RFID, Micro Sensor

1. Introduction and Background

Parallel stochastic assembly methods such as fluidic self assembly (FSA) are economically beneficial when large amounts of small components are placed in designated positions [1]. FSA has been used successfully in the electronic packaging industry for placing IC chips [2]. The technical limita-

tions to assemble IC chips stochastically are due to multiple I/O pads where the correct orientation of the chip is crucial to being interconnected in automatic processes. Although vision system and additional successive processes could be used to compensate for this deficiency, it would be more economical to compensate process steps in wafer level [3]. Based on this assumption a concept has been



Figure 1. Squared chips include a 250 μm x 250 μm notch to achieve asymmetrical shape. (ASIC– designed and fabricated at CNSE).

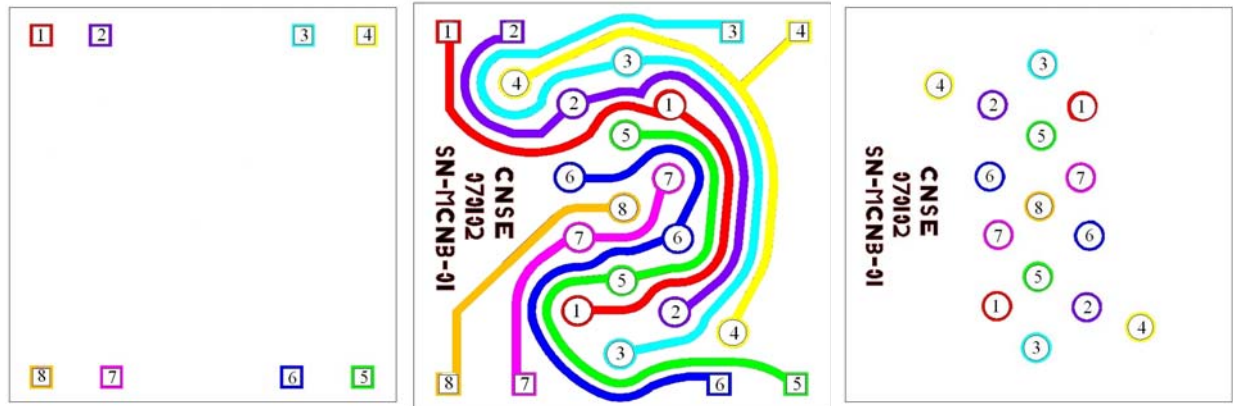


Figure 2. A rectangular COTS chip with 8 I/O pads before RDL is applied (left); Chip with RDL pattern (center); Finished symmetrical chip with RDL to be used for self-assembly (right).

developed to re-route the existing I/O pads in a symmetrical order. This would enable a chip to be always correctly aligned and interconnects could be made automatically without determining how a chip is aligned in its correct location.

2. Concept and Design

In the first experimental phase chips were designed and fabricated asymmetrical. One corner of the chip received a $250\ \mu\text{m} \times 250\ \mu\text{m}$ notch (Fig. 1). Through initial parallel stochastic assembly methods we saw a yield drop by more than 90% at the first attempt. The notch impeded enormously letting the chips locating and aligning to the designated areas. Compared to chips of squared shape, using rectangular chips decreased the yield already. In the next design a rectangular COTS chip (a memory chip from Microchip) with 8 I/O pads was chosen to design a redistribution of the I/O pads so that the chip could be aligned in any of the two possible orientation but the I/O pad would always at the same position(s) (Fig. 2). For a rectangular RDL the number of I/O pads increases from (n) to $(2n-1)$. For

the memory chip in rectangular shape a total of 15 pads needed to be designed, that the chip could be located in any of two possible alignments and having each I/O pad in the same position regardless orientation of the chip.

In the next development step the COTS chip was designed into a square shaped chip. The street width between two chips had a sufficient width since the chips purchased on the wafer level were designed to be singulated by dicing. To form the chip into base shapes to be used later in a parallel stochastic assembly process the chips were etched in the streets thus not requiring such a wide street as it would be necessary for wafer dicing.

Creating a square symmetrical I/O pad pattern proved to be difficult if a one-layer RDL approach was used. For a squared symmetrical chip the number of I/O pads would rise from (n) to $(4n-3)$ and in our case from 8 to 29 I/O pads. We developed a multi-level RDL which simplified demonstrated a 3-D model using 4 different I/O (Fig. 3 and 4). (Patent pending).

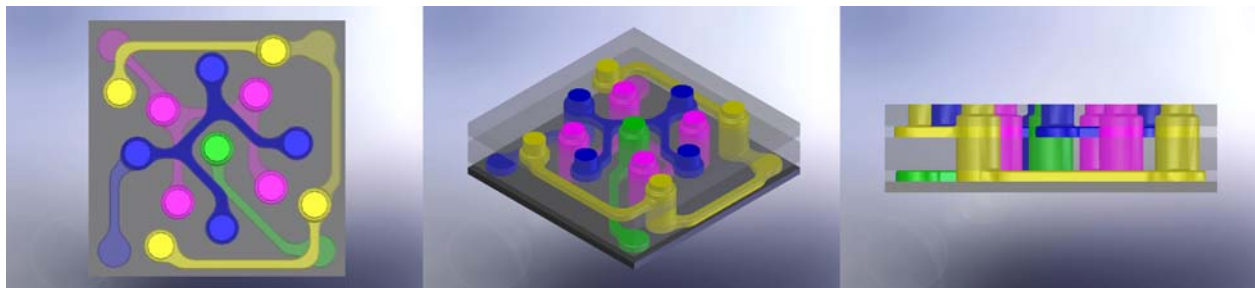


Figure 3. A model of a multi layered RDL using two dielectric layers: Top view (left), squared chip with 4 original I/O pads; 3D-view (center); Side view (right).

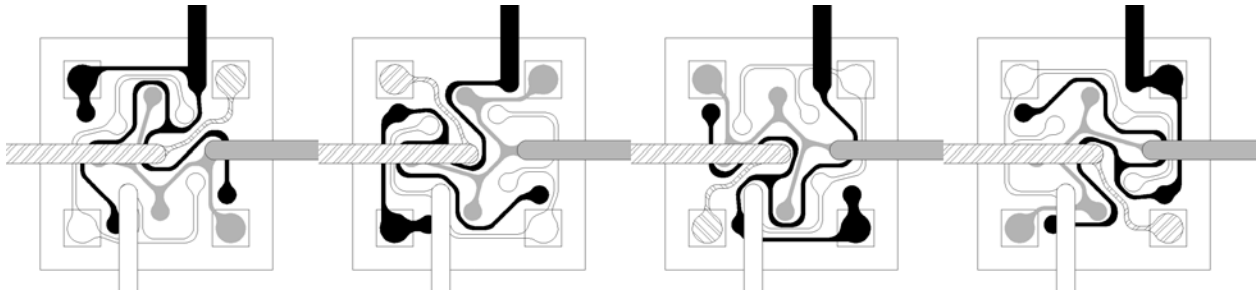


Figure 4. A square chip with RDL can align itself in any four possible direction without affecting the inter-connect process. The I/O pads are always located in the same position.

3. Materials and Methods

Processes and materials that are used in the RDL fabrication for off-the-shelf ICs are based on traditional photolithography and micro fabrication. A complete redistributed layer on an IC for the purpose of this paper will be called a system consisting of two distinct material films; one conductive material layer that is used to create the redistribution pattern and relocate the I/O pads, and an insulating layer used to separate the consecutive conductive layers.

The first step in the fabrication process was to select materials for both the conductive and insulating layers based on the processes readily available in-house. It was decided to use sputtered Aluminum (Al) as conductive layer based on its low cost and capability to be used as seed layer for elec-

troless Nickel plating if need for this occurs in the future. Sputtering is also a stable process that gives good uniformity across the wafer and takes only 40 min. to apply 1 μm thick layer of material. The patterning of the Al is done using photolithography with positive resist (i-line) as protective layer, followed by etching.

Selecting the material for the insulating layer was more challenging and multiple manufacturers of dielectric materials were considered. Several considerations taken into account were; application by spin coating (thickness $> 4 \mu\text{m}$), photo-sensitive (preferably negative tone, min. 10 μm resolution), resistant to acetone/IPA for prolonged periods of time, good dielectric strength, processing temperature not exceeding 350°C, resistance to KOH and HF during short exposures. The manufacturers were narrowed down to Sumitomo, Honey-

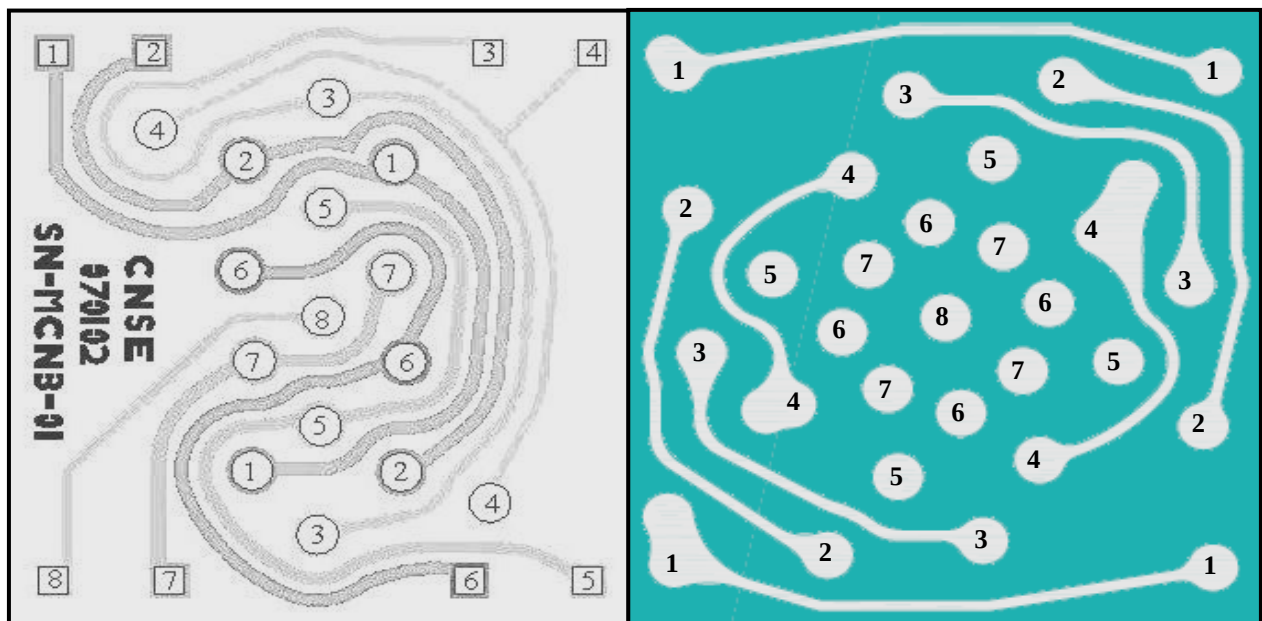


Figure 5. First design (left) with one Al layer and 15 Pads for 2-side symmetry, and newer design with two Aluminum layers and 29 pads for 4-sided symmetry (right).

well, and HD Microsystems (HDM). HD-4100, a negative tone, spin-on polyimide by HDM was selected based on the above criteria. This material can provide coat thickness (after final cure) in the 5-9 μm range, with resolution of 5 μm , dielectric constant $\epsilon = 3.2$, and final cure temperature as low as 300°C for 3 hours in nitrogen atmosphere. It can be patterned using i-line or broadband exposure with minimum energy of 250 mJ/cm² and has very wide processing window. It is also resistant to all chemicals listed previously after final cure.

An 8" silicon wafer populated with 24LC64/24AA64 memory chips by Microchip was selected for processing as pilot wafer. The 24xx64 memory chip is a rectangular chip (1508 x 1587 μm) with 8 I/O pads. The initial design was made to use one dielectric and one conductive layer for two possible orientations in the receptor cites; the eight original pads are redistributed to 15 symmetric pads (Fig. 5, *left*). Later version added a second conductive layer right after the passivation layer of the chip and used some of the street width to create a nearly square chip (1585 x 1587 μm) with four possible orientations in a receptor cite and a total of 29 pads (Fig. 5, *right*).

4. Fabrication

The methods used for fabrication include standard microfabrication/photolithography processes; spin coating (Karl Suss RC-8), exposure (Karl Suss MA-8), development, sputtering (Lesker CMS18), oven curing (Yamato DSV 600, Espec PHH-201). It is worth mentioning that based on the minimum feature size ($\sim 25 \mu\text{m}$) and the R&D nature of the study, printed flexible masks (Fineline Imaging) on Mylar were selected for the exposure process; these cost at least 8 times less than chrome on glass masks and have turn around time of less than one week.

Before any processing began, resistance measurements were taken using a microprobe on several locations across the wafer, between the ground and the other seven pads on the chip. This was done to allow comparison to the values measured after the RDL is applied.

For the initial design we started with application of a dielectric layer of spin-on polyimide, which was patterned by lithography; vias were opened to the original eight pads and streets were cleared of polyimide material (Fig. 6).

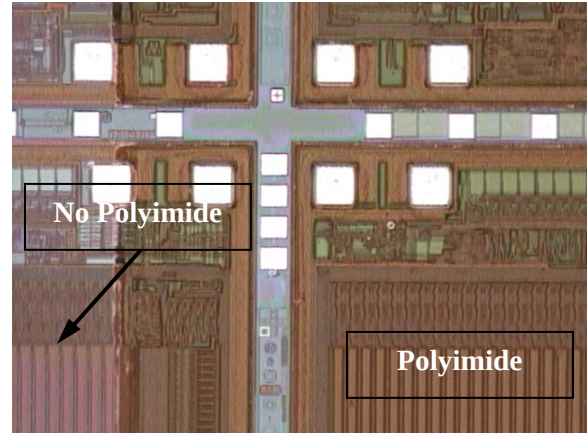


Figure 6. Polyimide covered memory chips.

In the next process, 1 μm thick Al layer was sputtered on top of the wafer, followed by spin-on application of positive resists and patterning of the resist (Fig. 7, *left*). After development the wafer was hard baked at 120 °C for 4 minutes and the unprotected aluminum was etched away (Fig. 7, *right*).

After the RDL pattern was completed, the device wafer (Microchip wafer) was bonded to a handle wafer using a KOH resistive bonding coating. Next, the bonded wafer was thinned on the device wafer side to a specified dimension; desired height of the silicon chip including the RDL thickness (a one layer, two material RDL adds about 6 μm to the total height) plus 5 to 10 μm for safety. In the next step the bonded wafer pack is etched in 2:1 KOH solution to the final chip height, followed by short (30 sec.) dip in buffered HF for cleaning. A KOH resistive layer is then deposited on both sides of the wafer using a reactive ion etcher and the de-

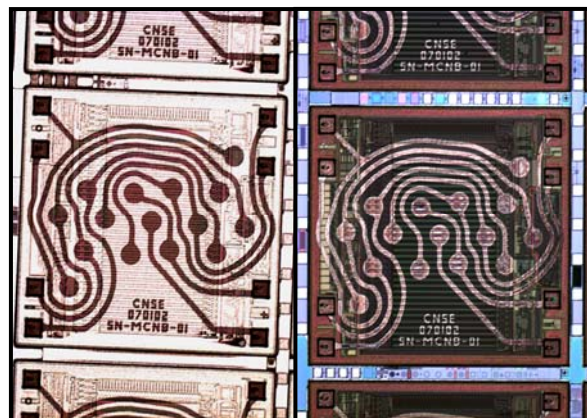


Figure 7. Patterned photoresist before Al etch (left), and patterned Al after etching (right).



Figure 8. Mask pattern used for backside patterning of device wafer to create chips with sharp and well defined corners.

vice side is patterned using positive photo resist (Fig. 8).

The unprotected areas on the backside of the device wafer are then plasma etched to remove the exposed KOH resistive layer. The photo resist is then stripped using acetone and the bonded, patterned wafer pack is placed in 4:1 KOH solution for chemical singulation and applying the natural slope of the finished chip. After the chip pattern is etched, the whole wafer pack is suspended in a solvent for a 24 hour period to release the RDL patterned chips, followed by acetone rinsing to remove any residue left from the bonding material. The released chips are stored in IPA solution under cleanroom conditions prior to assembly.

Application of a top dielectric/passivation layer was not required at this point as the ICs are etched into the chips and after they are assembled by means of a parallel stochastic method, a laminate

layer is applied over the assembled flexible substrate. The vias are opened in the laminate material using eximer laser prior to integration in a circuit (Fig. 9).

5. Results and Discussion

The chips of the pilot wafer were successfully released and tested for continuity. Figure 10 (*next page*) shows individual dies and a close view of the redistribution pattern based on the initial 2-sided symmetrical design.

No additional functionality testing has been completed so far as the blocks released were made out of an untested, damaged wafer. After RDL fabrication on a known good wafer is completed (in progress at the time of paper preparation), the chips released and assembled on a flexible substrate will undergo functionality testing and will be integrated in a wireless sensor build on a rigid PCB.

Currently RDL on two different type chips is being fabricated, one based on the two Al layer design for the Microchip memory chip and a rectangular ASIC chip ($750 \times 1500 \mu\text{m}$) which has 12 I/O pads originally (Fig. 11). The ASIC design has three Al and two dielectric layers to get 2-side symmetry with total of 23 pads. Its fabrication has been more challenging due to the smaller area and higher I/O count (two times less and 1.5 times the number of pads compared to the memory chip, correspondingly).

Several issues were encountered so far in the ASIC fabrication. First, considerable “crowning” of the polyimide material around via holes was observed (Fig. 12 - *last page*). This crowning caused problems with the patterning of the consecutive Al layers as separation or breaking

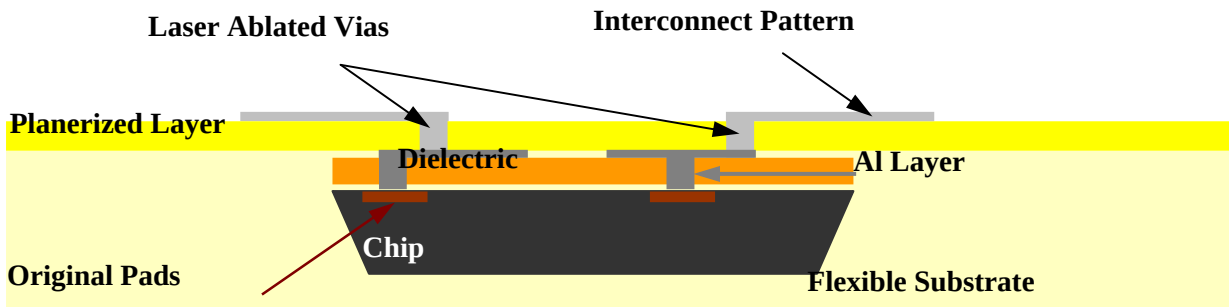


Figure 9. Cross section of a packaged RDL chip in a flexible substrate covered by planarization layer with laser ablated vias and interconnect pattern (*not to scale*).

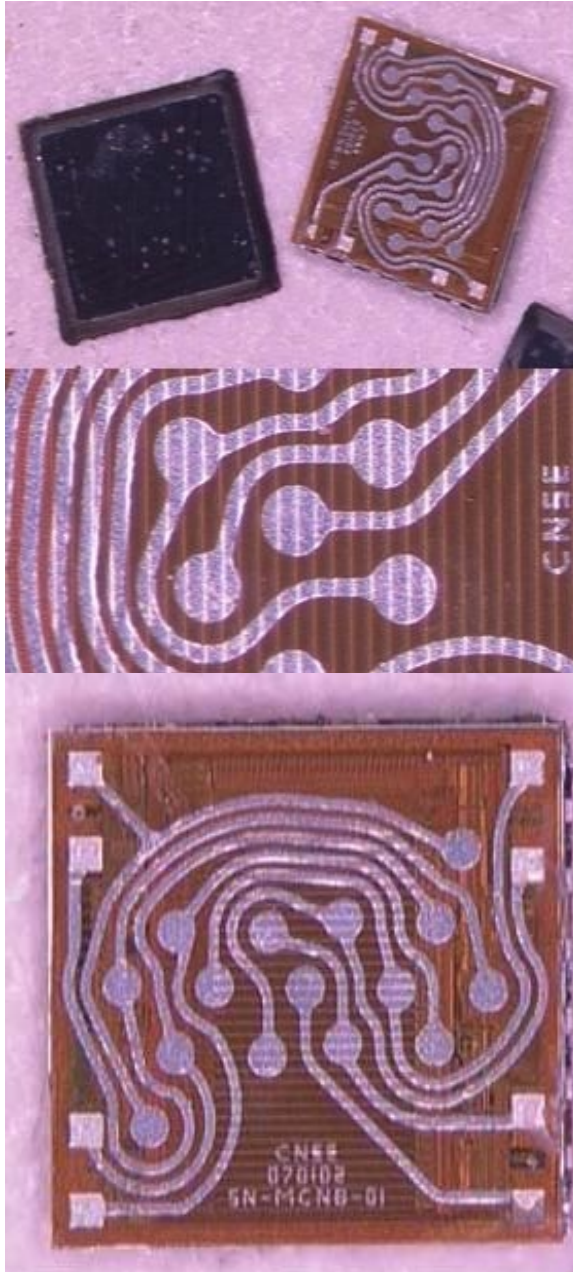


Figure 10. Released RDL patterned chips

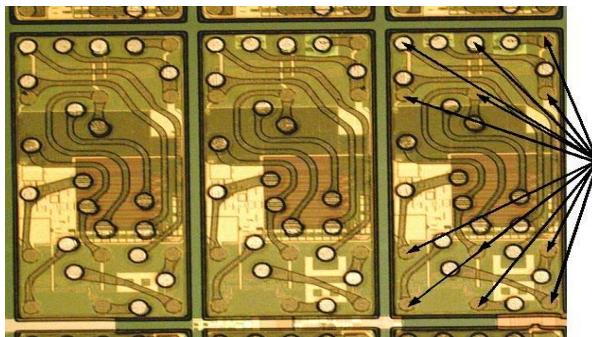


Figure 11. ASIC with first Al and Dielectric Layers applied and Patterned.

of the Al traces occurred. The problem was reduced by adjusting the polyimide exposure, development, baking time, and temperature parameters, which reduced the height of the crowning to acceptable values ($<0.4 \mu\text{m}$). Thicker layers of photoresist were also employed to better protect the traces in area where they connect with via holes. A CMP (chemical mechanical polishing) process could probably eliminate the “crowning”, but it is not currently available in house.

Another problem was out-gassing of the first polyimide layer. Due to the way the ASIC chips are situated on the wafer (“clusters” of four chips surrounded by large “empty” areas, Fig. 13), the Al masks were made that the “empty” areas were left covered with Al (to reduce etch contamination and processing time). This, however, sealed the “empty” areas, trapping gasses from the lower polyimide layers, which in turn created gas bubbles in the film and led to delaminating. To solve this problem, the masks for the Al layers were redesigned to have openings in the “empty” areas, allowing out-gassing. Also, final cure of the polyimide at the recommended 375°C will probably reduce the effect, but this has not been tested as an oven capable of reaching that temperature is not currently available in house.

6. Conclusions

The proposed method for creating two- or four-side symmetrical IC die is expected to increase the yield in a parallel stochastic self assembly process and eliminate the need for pattern recognition when interconnecting the dies to a conventional PCB circuit. The known and always identical position of I/O pads in turn will allow more conventional and cost-effective methods for circuit integration to be used, such as traditional screen printing. Despite the challenges encountered, a successful

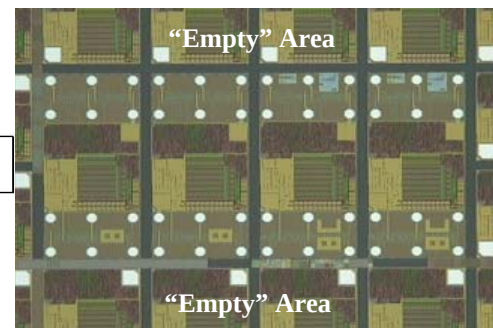


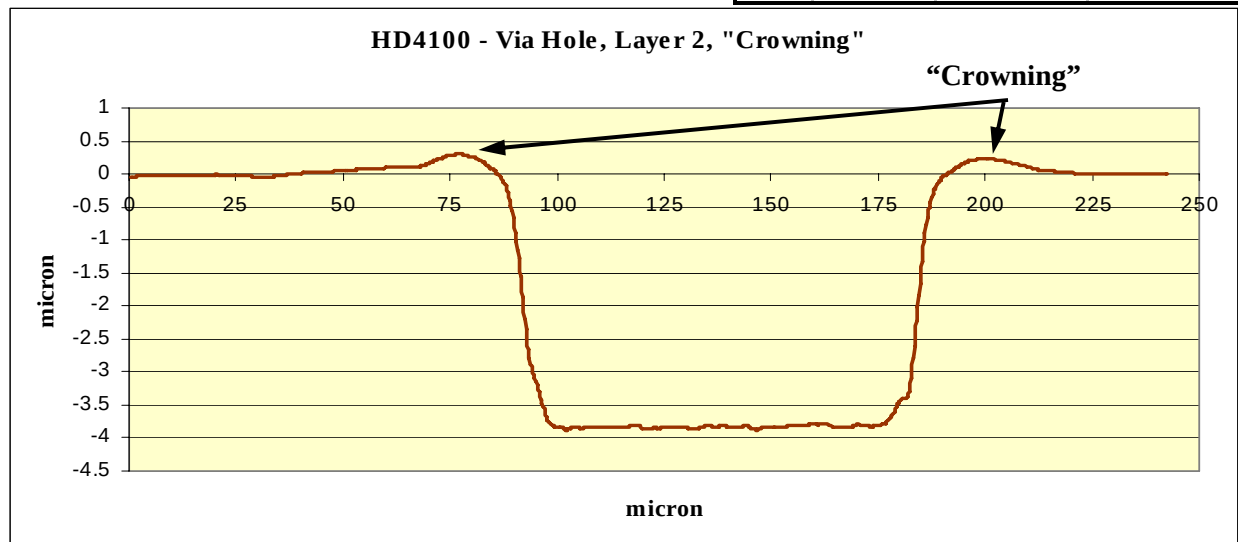
Figure 13. “Cluster” of ASIC Chips

Table 1: Resistance of released IC chips with fabricated Re-distribution Layer

Resistance measured [k Ω]						
Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Mean	St.Dev
372.5	373.3	367.5	371.3	367.5	370.4	2.76
372.3	372.8	367.7	371.4	369.8	370.8	2.07
369.5	369.8	364.8	369.2	365.1	367.7	2.50
403.9	406.4	400.2	402.2	399.0	402.3	2.94
372.4	372.3	366.7	371.3	366.9	369.9	2.88
372.4	372.3	373.7	347.3	366.7	366.5	11.06
377.0	382.4	373.3	373.7	377.0	376.7	3.65

Table 2: Resistance measured for a chip with Redistribution Layer vs. Packaged IC (24xx64 Microchip Memory Chip).

Resistance [k Ω]				
Pad 4 to:	RDL NB	Packaged IC	Difference, %	
1	370	351	5.5	
2	371	351	5.6	
3	368	349	5.4	
5	402	344	17.0	
6	370	350	5.7	
7	366	350	4.7	
8	377	355	6.1	

**Figure 12. "Crowning" effect around vias.**

RDL fabrication will greatly increase the yield and reduce the cost in die placement, interconnecting, and circuit integration of flexible substrates.

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