

Low-k Interconnect Oriented Lead Free Sn-Cu Bump Process Integration with Sn/Cu Stack Plating

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Abstract

We have developed Low-k oriented lead free Sn-Cu bump process integration with Sn/Cu stack plating. The key features are lower cost process than alloy plating, by sequential plating pure Cu and pure Sn, and suitable for low-k interconnects, with Sn-Cu bump material has high potential of stress alleviation effect. Sn-Cu bump employed sequential Cu and Sn electroplating followed flux reflows. We have found wide process latitude depended on stacked thickness ratio of Cu/Sn. Single metal plating process combination with Cu and Sn has a cost advantage. Thin Ni barrier layer thickness has achieved only 350nm with sputtering. The reliability test shows superior results of TCT B (Thermal cycle test), PCT, and HTS reliability test with low-k material interconnection, which use k=2.7 material. Sn-Cu bump has a high creep rate, therefore Sn-Cu deformed itself and alleviated the stress of thermal cycle for low-k interconnects. EM test also shows sufficient for application.

Thus, the lead free SnCu bump has a potential of most suitable candidate of low-k BEOL 65 nm and more shrinkage generation which has weaker mechanical property and greater die size.

Keywords: Lead Free, SnCu, Stack plating, Bump, Low-k interconnect

Introduction

The latest high performance LSI devices require a lot of new materials^[1], such as NiSix, metal gate, high-k insulator, SiGe, high

stress liner, Cu interconnection, low-k insulator, low-k cap insulator and so on, as well as FBEO (Far Back End Of Line) integration process needs improvement to appropriate new technologies. In

order to get high speed and density, LSI requires shrinkage and multi stack layer interconnection, although interconnect electrical resistance and capacitance has been going to be higher as shrinkage device. It was solved by lower resistance material, Aluminum interconnects to Copper, and lower dielectric insulator material, SiO₂ to F doped SiO₂ to SiCOH low density material or organic polymer material. On the other hand, mechanical properties and adhesive properties of multi layer with new material became lower than before. For instance, elastic modulus of dielectric material is CVD-SiO₂: about 50GPa, Low-k CVD-SiCOH (k=2.7): about 5GPa, almost 1/10. For packaging, an actual user environment is no change or tougher situation, despite lower mechanical properties. Therefore the burden of FBEOI integration process is increasing, it needs to improve and compensate mechanical properties. The one of solution is stress relaxation. Hi-Lead bump, typically concentration is Pb(95wt%)Sn(5wt%), work out as a stress relaxation material. Due to environmental burden reduction, it has to reduce lead concentration. Recently the alternatives which are lead free materials are implemented. It is not achieved relaxation effect as same as hi-lead material. The most common lead free material is Sn-Ag at the present time. Sn-Ag bump fabrication is adopted Sn-Ag alloy plating method. The one of reason Sn-Cu did not become common material was that Sn-Cu alloy plating was very difficult due to 0.7wt%Cu concentration control was sensitive. Sn-Ag was typical 2 - 3.5wt%.

We have selected SnCu material because the relaxation effect can be expected^{[2]-[6]}.

This paper discusses about SnCu bump for low-k generation LSI.

Experimental results

Fabrication process

Fig.1 shows Sn/Cu stack plating bump process flow sequence.

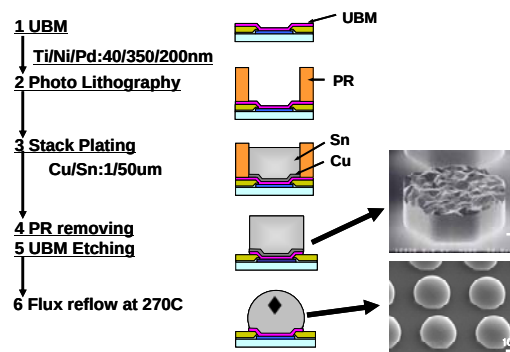


Fig.1 Sn/Cu bump process flow sequence

Firstly, UBM (Under bump metal) layer was sputtered sequential, first step was contact hole cleaning with RF (Radio Frequency) bias sputtering, 2nd step is Ti (40nm) deposition, next is Ni (350nm) deposition, final step is Pd (200nm) deposition. All sequence is no breaking vacuum condition. The Ni layer acts as barrier layer between Aluminum interconnect and Sn-Cu bump. The Pd is noble metal which is oxidized scarcely in air ambient. The Pd surface is always stable even if environmental changing as well as Gold. In addition, the Pd acts as superior plating seed layer, due to the electric standard potential of Pd²⁺ and Cu²⁺ are +0.915V and +0.335V respectively. The 2nd process is the bump photolithography process. Photo resist mask thickness is 70um and

negative type. Photo exposure light source is i-line (365nm). After photolithography process, photoresist de-scumming preconditioning, which is O_2 ashing with no bias, is implemented. The 3rd process is stack plating. Pure Copper plating thickness is 1um and then ultra low alpha pure Tin thickness is 50um. The plating machine has a multi chamber type and is able to plate both sequentially. The 4th process is photoresist removing. Fig.1 shows SEM photograph after photoresist removing process. The Tin surface seems relatively rough but it is acceptable roughness because it does not matter after ball making with flux reflow. Next, the 5th process is UBM etching process, consequently the bumps are isolate. The Pd and Ni are simultaneously removed by aqua regia with buffer solution. Although the aqua regia solution generally attacked Cu and Sn plating material, we have succeeded slight Cu/Sn damage with appropriate solution ratio and buffer concentration. After Pd/Ni removing, sequentially Ti layer is etched by alkali and peroxide combination solution. The 6th process is flux reflow. The flux is water soluble type, is implemented. The reflow temperature is 270C. After reflow the flux is removed by water. Then we have succeeded Sn-Cu solder bump as shown in Fig.1 SEM photograph.

Sn/Cu Stack plating

Sn-Cu bump employed sequential Cu and Sn electroplating followed flux reflows. The reflow process carried out alloying Cu_6Sn_5 between Cu and Sn as shown Fig.2. The Cu_6Sn_5 layer placed at the bottom of Sn-Cu bump.

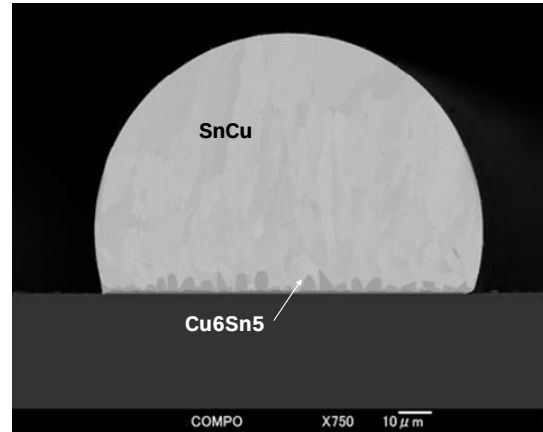


Fig.2 Cross sectional SEM photograph of SnCu bump

Fig.3 shows relationship between Sn/Cu thickness ratio and Cu concentration in Sn-Cu bump after reflow process.

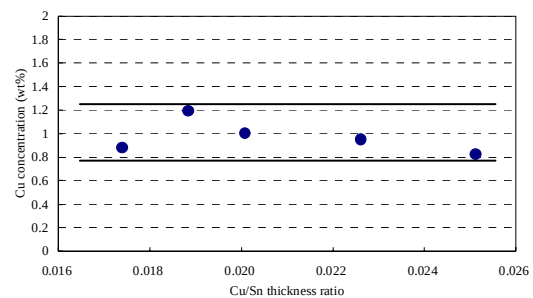


Fig.3 Cu concentration in SnCu bump with Cu/Sn thickness ratio dependent

The ratio from 0.015 (Cu/Sn=1/65um) to 0.022 (Cu/Sn=1/45um), the Cu concentration shows minimum 0.88 and maximum 1.95 wt%, it is not dependent on Cu/Sn thickness ratio. It means even if the Cu/Sn thickness ratio changes by mistake or unexpected problem, the number of Cu concentration in Sn-Cu is stable $1wt\% \pm 0.2$. If the Cu concentration changes from 0.8 to 1.2wt%, the highest melting temperature of Sn-Cu is about 250C. Then reflow temperature is not matter,

since we choose 270C reflow.

Fig.4 shows Cu, Ni and Sn distribution map of Sn-Cu bump. Fig.4 (a) shows bump whole area. Fig.4 (b) shows enlargement of bottom region.

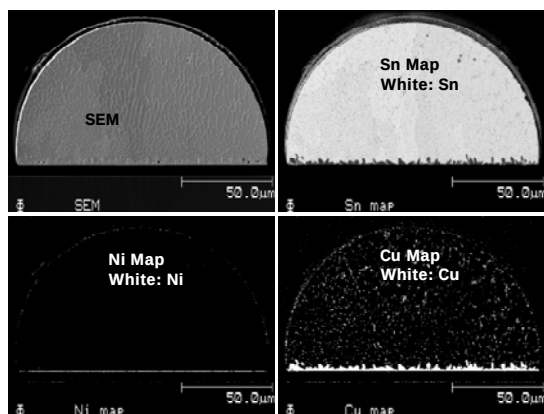
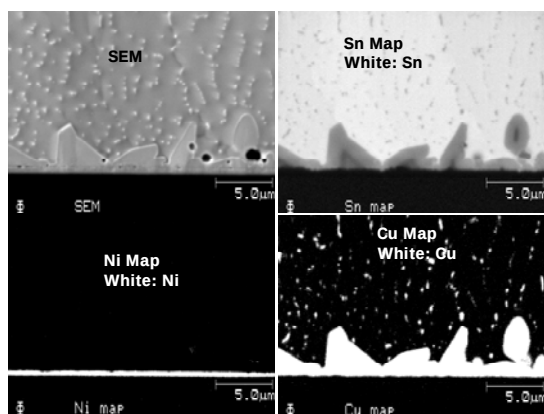


Fig.4 (a) Sn, Ni and Cu concentration MAP



Fi.4 (b) Sn, Ni and Cu concentration MAP with bottom region enlargement.

In terms of Ni diffusion, Sn-Cu bump shows Ni diffuse scarcely from under Ni layer to Sn-Cu region. In general, Sn-Ag material indicated Ni diffusion from thick under Ni layer to Sn-Ag region. In the case of Sn-Cu, since Cu_6Sn_5 acts as diffusion barrier between Ni and Sn-Cu region, Ni diffusion is inhibited and remained Ni barrier under Sn-Cu region. From the results, Ni layer is able to thin about 350nm.

Regarding Cu concentration in Sn-Cu bump region, Cu exist as Cu_6Sn_5 , precipitate along with Sn grain boundary. Over saturated Cu as Cu_6Sn_5 in pure Sn grain sweep outside and precipitate Sn grain boundaries and making Cu_6Sn_5 layer at bottom region. Cu concentration in Sn-Cu region is controlled by changing thickness of Cu_6Sn_5 bottom layer, then concentration is not great change, as shown Fig.3. Sn-Ag material could not control to stabilize Ag concentration if Ag thickness was changed^{[2]-[6]}.

One of features for Sn/Cu stack plating is cost effect. Pure Cu and Sn plating system and method has a quite simple which use conventional parallel plating, Cu and Sn plating anode, plating bath needs not change frequently because metal was supplied by anode material. For example, Sn-Ag plating system employed non-soluble anode, membrane system, two bath both anode and cathode, plating bath needs frequently changing additional metal solution since it consumed metal during plating in bath solution. The electric standard potential difference between Ag and Sn is 0.938V. Due to stable of silver content, the additives are needed additional. Our cost comparison between Sn/Cu and Sn-Ag plating estimated Sn/Cu indicated about 1/2 to 1/3 with running and material cost, in the case of plating process only.

Reliability test

The reliability test chips conditions as follows, chip size: (1) 12.5 x 14.5 mm and (2) 18.2 x 18.2 mm, Substrate size: 42.5 x 42.5 mm, core thickness: 8mm, bump pitch: 200, 150 µm

SRO (Solder Resist Opening): 100, 75 μ m. Table 1 shows the results of multiple reflow, TCT B (Thermal cycle test)(-55/125C), PCT (Pressure Cooker test)(121C/100%RH 2atm) and HTS (High Temperature Stress)(150C) reliability test. Si device generation is 65nm node with low-k material interconnection, which use k=2.7 material.

Table.1 Reliability test results (fail/total number)

Bump Pitch	Chip size (mm)	Material	Multiple reflow
150 μ m	12.5 x 14.5	SnAg	16/16 (x30)
		SnCu	0/28 (x30)
200 μ m	18.2 x 18.2	SnAg	6/6 (x20)
		SnCu	0/12 (x20)

		PCT 1000H	TCT 1000cycle	HTS 1000H @150C
150 μ m	SnAg	PreCon fail		-
	SnCu	0/14	0/224	-
200 μ m	SnAg	-	PreCon fail	Ni (5 μ m) barrier OK
	SnCu	-	0/36	Ni (350nm) barrier OK

The SnCu bump showed no fail and thin 350nm Ni layer also indicated no fail. Due to SnCu bump has a high creep rate, bump deformed itself and alleviated the stress of thermal cycle for low-k interconnects. Uchida indicated creep data as follows, Sn-Cu at 150C was A: 1.05E-10 (MPa)⁻ⁿ/hr, n: 7.6, E: 33.9Gpa, Sn-Ag was A: 1.76E-13 (MPa)⁻ⁿ/hr, n: 9.6, E: 36.0Gpa.^[4] The Sn-Ag bump showed all fail in pre-conditioning test and multiple reflow test at 270C before TCT and PCT test. The fail mode was BEOL cracking then electrical short fail occurred.

Fig.5 and 6 shows cross sectional SEM photographs of post reliability test. These indicate Sn-Cu bump has a potential of good reliability.

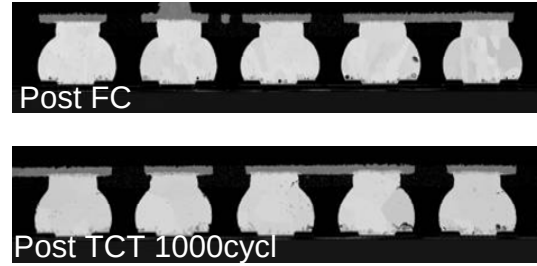


Fig.5 SEM Sn-Cu bumps conjunction photographs of post FC and TCT 1000 cycle.

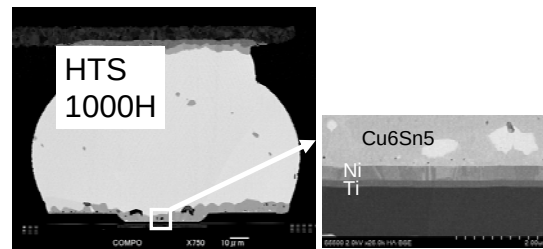


Fig.6 Post HTS 1000H Sn-Cu conjunction cross sectional SEM and enlargement of bottom region

EM (Electro-Migration) reliability test results indicated $E_a=0.76\text{eV}$, $n=-4.88$. Test conditions were temperature: 85-125C, electrical current I: 0.6-1.0 A/bump. Then, the estimated life time of failure indicated about 40 years when it applied in stress conditions were at 90C and electrical current density: 100mA/bump^[7].

Conclusion

In conclusion, the lead free SnCu bump with stack plating system has a potential of most suitable candidate of low-k BEOL 65 nm and more shrinkage generation which has weaker mechanical properties.

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